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THE SUMMARY OF Ph.D. DISSERTATION

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Title

Development and Performance Evaluation of Massively Parallel Processor JUMP-1

Abstract

A Cache Coherent Non-Uniform Memory Access machine (CC-NUMA) is one of hopeful candidates for future common high performance machines. Unlike bus-connected multiprocessors, the system performance can be enhanced scalably as to the number of processors. Moreover, parallel programs developed in small multiprocessors can be transported easily. Presently, commercial CC-NUMA machines have been developed.

JUMP-1 is a prototype of a massively parallel CC-NUMA developed by collaboration of 7 Japanese universities The major goal of this project is building an efficient cache coherent distributed shared memory on a large system with more than 1000 processors. A lot of novel techniques are introduced in the DSM of JUMP-1 for this purpose.

In order to satisfy both high degree of performance and flexibility, JUMP-1 has several distinctive structures. Interconnection network called RDT (Recursive Diagonal Torus) includes both torus and a kind of fat tree structure with recursively overlaid two-dimensional square diagonal tori structure. A dedicated processor called MBP(Memory Based Processor)-light is proposed to manage the DSM of JUMP-1. MBP-light consists of a simple dedicated core processor and hardwired controllers that handle memory systems, bus and network packets. Every cluster board which consists of processors, memory etc. has a serial link called STAFF-Link(Serial Transparent Asynchronous First-in First-out Link). Each channel of STAFF-Link is connected to an independent I/O unit, and works in parallel to obtain the scalable I/O bandwidth.

By the way, The first prototype of JUMP-1 with 4 clusters/16 processors started to work in 1999, and the system that provides 16 clusters/64 processors was available from 2000. The first and the second prototype are used for evaluation in this paper.

From the evaluation, the following result was appeared. The maximum bandwidth of RDT network is 100M Bytes/sec in the case the packets consists of 15 flits. Multicasting mechanism saves 52 cycles compared with unicasting by core processor software even when it sent only one packet, and does not require extra cycles for multicasting up to 8 packets. It also contributes to resolve the network traffic congestion. The automatic acknowledge generation logic saves 40 cycles compared with generation by the software of core processor. The automatic acknowledge packet combining mechanism achieves 2.4 times performance compared with that by the software. The Buffer-Register Architecture proposed for MBP Core improves performance with 5.64% in the home cluster and 6.27% in a remote cluster. Only a special instruction for hashing cluster address is efficient and improves the performance with 2.80%, but other special instructions are almost useless. The I/O bandwidth for reading is 2.1Mbps and the bandwidth for writing is 4.5Mbps. The whole I/O bandwidth increased linearly as the increase number of clusters and I/O units. The remote read cycles with JUMP-1's DSM system is 469 cycles (9.38usec at 50MHz) in the case that there is the valid data in the home cluster, and 850 cycles (17.00usec at 50MHz) in the case that the valid data is not in the home cluster. The execution result of matrix multiplication program shows that, the rate of speed-up is 3.72 with 4 processors system, and 6.61 with 8 processors.