（様式乙 **1-3-2**）

THE SUMMARY OF Ph.D. DISSERTATION

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Title

Short TAT Design and Manufacturing Methodologies in “System LSI” Development

Abstract

In order to develop a small size and high-performance equipment with enormous kinds of functions, it is essential to develop a “system LSI” for a wide range of uses for consumer and professional pieces of equipment. The TAT (Turn Around Time) of design and manufacturing of such LSIs must be shortened under competitive pressure for such development in today’s environment. Under such circumstances, the author directs his attention in this study to the three most important aspects for reducing the TAT: 1) hardware and software co-design in a design process; 2) high-speed data conversion from LSI design data to manufacturing data in a design/manufacturing interface process; and 3) wafer-direct EB (Electron Beam) exposure method in a manufacturing process, which allow mask-less lithography. The ultimate goal of this study is to offer the specific methods, verify the methods and allow the methods in practical use.

Chapter 1 and Chapter 2 summarize the background of this study, previous studies and the practical applications of this study.

Chapter 3 describes a systematic design methodologies in which a top-down flow design and a hardware/software co-design are simultaneously and mutually performed, and they have been applied to developing MPEG-2 video encoder LSIs. Particularly software and hardware functional partitioning in a hardware/software cooperative architecture has been systematically performed in this methodology. Proposed methodology is inferred to reduce the TAT of the design process by 10%.

Chapter 4 describes the high speed conversion method which converts LSI layout paten data into control data of a lithography system. The author proposes a conversion method which uses a hierarchical structure of LSI CAD data. The use of the data under such a structure allows the reduction of the amount of the data to be converted. When such hierarchical structure can not be used, new concepts are introduced such as restructuring of the hierarchical structure, “link mark” and “null edge” in order to resolve the difficulties.

Chapter 5 describes EB exposure characteristics studies on a wafer-direct EB exposure, which dispenses with the need for the preparation of photo masks. A series of the electron scattering simulation were conducted to obtain the required characteristics of the electron beam. As a result, it became evident that 0.5 μm LSI pattern delineation requires a combination of acceleration voltage of 30kV and a beam edge width of 0.15 μm.

Chapter 6 describes the results of the feasibility studies on a wafer-direct EB exposure system. Precision beam control is given to the three methods: 1) a dynamic focus correction method corresponding to the deflection distance; 2) deflection distortion correction method; and 3) overlay distortion correction method involving wafer distortion originating from manufacturing processes.

Chapter 7 summarizes the findings of the preceding chapters and presents the results of the studies.

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