SUMMARY OF Ph.D. DISSERTATION

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Title

A study on low-power, high-reliability and high-speed SRAM circuits

Abstract

As well as general-purpose static-random-access memory (SRAM) ICs, SRAM is used in on-chip memory modules in system-on-chip (SOC) ICs. Improving the performance of SRAM modules in the latter role is a key to improving overall IC performance. In this work, I describe circuit techniques that lower power consumption and increase the reliability and speed of SRAM.

Techniques that reduce power consumption in active mode are described in Chapter II. The first is a lithographically symmetric cell that allows lower-voltage operation. The patterns of the poly-silicon layer and the diffusion layer in the cell are very simple, which helps in achieving good electrical balance for the cell and thus allowing lower-voltage operation. Power consumption can also be lowered by varying the operating frequency and power-supply voltage with system load. To support this, the range of operating voltage must be widened. This is achieved in a voltage-adaptive timing-generation scheme. This scheme generates optimum activation timing for the sense amplifiers across the range of supply voltage.

Techniques that reduce power consumption in standby mode are described in Chapter III. The key measure here is the reduction of leakage currents. In addition to the subthreshold leakage current, the increases in the gate-oxide tunnel leakage and gate-induced drain leakage (GIDL) currents that accompany advances in MOS technology must be considered. An electric-field relaxed (EFR) scheme is proposed as a way of suppressing these leakage currents in SRAM cells. In this scheme, a 1.0-V supply replaces the 1.5-V supply to the bit lines and VSSM is raised from 0 to 0.5 V.

Techniques for reducing soft error rate (SER) caused by comic rays as a measure for higher reliability are described in Chapter IV. A rule that governs the maximum number of multi-cell errors induced by a cosmic ray strike is derived through a combination of device- and circuit-level simulation. A new error-checking-and-correction (ECC) architecture that is capable of handling such multi-cell errors caused by cosmic rays is then developed. An ECC architecture for the lithographically symmetric cell of Chapter II is also proposed.

Techniques for high-speed circuit operation are described in Chapter IV. These are applied in a two-port cache architecture that features a hierarchical bit-line architecture, consisting of local bit-line pairs and separate sets of global bit-line pairs for writing and for reading. Write operations that follow read operations are sped-up by having the write amplifier drive the global bit-line pairs for writing while the signals from cells are being transmitted to the global bit-line pairs for reading. A timing-insensitive sense amplifier that reduces read access times is also proposed. This consists of three non-latched sense amplifiers, each of which has a small voltage gain. The combination provides a sufficient voltage gain for the output signal.