SUMMARY OF Ph.D. DISSERTATION

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Title

Efficient Data-Transfer Schemes for On-Chip Interconnection Networks

Abstract

System-on-Chip (SoC) is a Large Scale Integrated circuit (LSI) that integrates various functions into a chip. SoCs have been received attentions due to the wide range of applications, ability to integrate functions, cost reduction, and performance improvement. However, according to the increase of transistor density, a methodology to design SoCs becomes very complicated and time-consuming. For ease of chip designs, SoCs are designed by reusing Intellectual Property (IP) cores that have already been designed and verified. Another approach is to use a programmable device which does not require chip fabrication. A key to success in both approaches in terms of design time, performance, and chip cost is on-chip interconnection networks, or on-chip buses and Network-on-Chips (NoCs). In this thesis, hov to design an on-chip bus and an NoC efficiently is discussed, especially taking both performance and hardware cost into account.

Firstly, novel cost- and performance-efficient implementation techniques for the on-chip bus with bus wrappers ar addressed. Four major features are included: (i) a wrapper interface for small latency cycles, (ii) a write buffer switching technique to optimize wrapper hardware cost and performance, (iii) a retry technique to connect fast and slow slaves to the same bus with small performance overhead and live lock avoidance, and (iv) a bit-width conversion technique to reduce hardware cost. Simulated results with a traffic assumed in an SoC show that the throughput is improved by 14 % and the read and write latencies are reduced by 16 % and 11 %, respectively, compared with the conventional wrapper bus. Furthermore, 50 % hardware is reduced in the proposed bus for a 5-master and 7-slave configuration in a CPU-based SoC in 0.15μm CMOS. It works at 200-MHz clock frequency and occupies 3.3-mm^2 area.

Next, a novel data transfer scheme for NoCs in programmable devices is described. A novel routing technique for achieving smaller hardware cost and higher performance is discussed. Routing information is transferred in parallel to data, which is different from the conventional packet data-transfer. This removes cycle penalty for transferring header and hardware overhead for handling packet structure. The proposed routing technique uses static analysis results of communication patterns in applications and only assigns routing labels to the pairs of communicating nodes. For reducing the required number of bits for routing information, a local label which is only valid in a channel between neighboring routers, is addressed. Local labels allow reusing a label value inside a network and results in reduction of the number of label values. The presented results show that the hardware amount for a router is reduced by 46 % from the conventional distributed routing router using global addresses.