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## Title

Hierarchical Interconnection Network of a Multiprocessor System for a Static Scheduling Technique

## Abstract

In order to maximize effective performance of large scale multiprocessors, techniques on static scheduling with sophisticated compilers have been developed. An interconnection network, that is a critical component of multiprocessors, is also a target of static scheduling.

In this paper, a hierarchical multi-stage interconnection network (MIN), R-Clos, which is both highly schedulable and scalable, is proposed. R-Clos consists of hierarchically extended Clos networks connected with extra intermediate stages. Frequent local communication between neighboring processing elements are supported with high bandwidth rearrangeable Clos networks used in a basis of R-Clos. A large-scale system can be built owing to hierarchical structure with less hardware than that of other flat MINs.

The transfer performance of R-Clos is analyzed by probabilistic simulations. The simulation results show that R-Clos achieves reasonable performance under local communication dominant traffic.

Secondary, scheduling schemes of packets transfer on R-Clos are proposed. Using this scheme at compile time, the parallelizing compiler and scheduler can arrange the packet's routes and schedule the access time to avoid any packet collisions.

Additionally, in order to keep the static scheduling under partially scheduled traffic, which includes certain unscheduled packets, a switch architecture called MGF switch is proposed. MGF switch has two sets of the transfer channel for scheduled packets and non-scheduled packets respectively. We fabricated the MGF switch on 0.35  $\mu$ m gate array. The amount of hardware of the switch chip is about one hundred thousands gates and the maximum frequency of the switch chip is about 50 MHz.

Through the instruction(clock) level simulation, the scheduling scheme performance on MGF switch is analyzed. The result of the evaluation by the simulation shows the availability of proposed network systems, the combination of R-Clos, the scheduling scheme and MGF switch architecture.