SUMMARY OF Ph.D. DISSERTATION

School	Student Identification Number	SURNAME, First name
		ONODERA, Kiyomitsu

Title

Design and Fabrication of WSiN-gate GaAs-FETs and Its Application to Millimeterwave MMICs

Abstract

The purpose of the study is to design and fabricate both active and passive devices comprehensively for use in microwave monolithic integrated circuits.

Fully ion-implanted n^+ self-aligned GaAs-MESFETs are adopted as active devices since ion-implantation technology is very attractive for its selective doping ability in a planar structure. Novel fabrication process has been developed by employing a refractory metal WSiN. It is electrically and metallurgically still more stable than WSi in high-heat treatments. In addition, WSiN sufficiently suppresses out-diffusion of Ga and As from the surface since it maintains its amorphous state after high-temperature annealing. This technology enables to form a high quality, very thin channel with high-carrier-concentration, which has achieved excellent dc and microwave performance. The relationship between measured device perforemance and the channel carrier profile is evaluated by using two dimensional device simulators. Also, to analyze device degradation and hot-carrier mechanism of the fabricated devices, the luminescence spectra at the breakdown condition is examined.

Since a buried p-layer can suppress substrate leakage current and permit thinning the effective channel thickness, it is very useful for sub-quartermicron devices. By focusing on the device elements in the equivalent circuit, the neutral p-layer effects on high-frequency performance is investigated. Moreover, new buried p-layer structure is proposed and examined on 0.1um devices.

A wide Au gate head made of a first-level interconnect is employed in order to reduce the gate resistance. ECR plasma RIE has been also performed for the formation of WSiN refractory metal gate apparently resulting in no harm to the channel. As the wide gate head results in parasitic capacitance, the relation between the gate head length and the device performance is examined. The gate resistance is also precisely calculated using the cold FET technique and Mahon and Anhold's method. A maximum stable gain decrease monotonously as the gate head length increases on account of parasitic capacitance. However, the device with appropriate the gate head exhibits an extremely low noise, which comparable to that of GaAs- or InP-based HEMT's.

Novel heterostructure MESFET's with InGaP barrier layer has been also developed. It is beneficial for GaAs MESFET's to use InGaP in order to suppress gate leakage current and reduce Schottky barrier height. Using tilted-angle n^+-implantation, two type of structure, symmetric and asymmetric, have been fabricated on the same wafer. The asymmetric structure is advantageous to improved breakdown voltage and high-power performance, while symmetric is to low-noise and high-current-gain performance.

Two types of novel microwire of a three-dimensional structure are developed for MMICs. One is a vertical microwire, which can be fabricated with a multilayer interconnection structure by folding a metal as a U-shaped wall buried in a thick polyimide insulator. The microwires are very useful to form miniature transmission lines, miniature inductors, shielding walls, and multi-functional passive elements. Another is micromachined waveguide, called a grooved conductor-backed coplanar waveguide. The waveguide has good compatibility with optical waveguides. By adopting a microshielded structure, unwanted substrate modes and resonances can be suppressed at frequencies up to 110 GHz.