SUMMARY OF Ph.D. DISSERTATION

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Title

Development of Metal Gate, Metal Source/Drain, and Strained Silicon Channel Technology for High Performance CMOSFET's

Abstract

Metal gate and high dielectric constant gate insulator technologies are desirable for MOSFET (Metal-Oxide-Semiconductor Field-Effect-Transistor) because of low gate resistance, no gate depletion, and low gate leakage current. On the other hand, Schottky barrier (metal) source/drain technology is also promising for high-performance MOSFET's because it provides shallow and low-resistivity source/drain regions with a simpler fabrication process. Accordingly, the introduction of metal gate and metal source/drain technology is a way to scale down the transistors and elevate LSI device speed and performance.

Therefore, in this study, novel technologies are proposed and developed in order to apply metal gate and metal source/drain to conventional MOSFET fabrication process.

Chapter 1 summarizes the background and previous studies.

Chapter 2 describes a novel transistor formation process (damascene metal gate process). This process is proposed in order to apply metal gates and high dielectric constant gate insulators to MOSFET fabrication, and it is demonstrated that the damascene metal gate transistors exhibit drastic improvement in transistor performance.

In chapter 3, the metal gate work function deviation (crystal orientation deviation) is found to cause the threshold voltage deviation in the damascene metal gate transistors, and the TiN work function (crystal orientation) control by chemical vapor deposition technique is found to be effective for the improvement in threshold voltage uniformity of the transistor.

In chapter 4, the combination of the dynamic threshold-voltage technology with the damascene gate transistor technology is proposed for realizing low threshold voltage and high drive current in metal gate MOSFET. And it is experimentally demonstrated that the threshold voltage for the new transistor is 0.15 V smaller than that for the conventional damascene metal gate transistor.

In chapter 5, the strain approach for improving the drive current of the Schottky Source/Drain transistor (for reducing the Schottky contact resistance) is proposed and theoretically investigated by using the non-equilibrium Green's function method and the interface dipole theory.

It is necessary to obtain the information of stress distribution in a device for developing the MOSFET with strained silicon channel. Therefore, in chapter 6, we describe a new stress simulation technology that includes the cleavage effect. And the accuracy of the calculated results is confirmed by Raman measurement.

Chapter 7 summarizes the results of this study.