

SUMMARY OF Ph.D. DISSERTATION

School	Student Identification Number	SURNAME, First name Midorikawa Takashi
<p>Title The cache coherent mechanism of switch connected multiprocessor</p>		
<p>Abstract Multistage Interconnection Networks (MINs) have been well researched as an interconnection medium between processing units (PUs) and memory modules (MMs) for medium scale multiprocessors. Unlike shared buses that allow to access only one MM at a time, MINs enable multiple accesses simultaneously. Snoop caches commonly used in shared bus connected multiprocessors are not available because of the nature of MINs, thus, they usually maintain cache coherence by the directories provided on MMs. However, this method requires not only large amount of memory spared for the directories but also extra latency caused by the accesses to slow large memory. Although several methods are proposed as solutions, for example, providing a part of cache or directories inside switching elements, they are still suffering from large memory expense, directory access latency, complicated structure of switching elements. To solve these problems, we proposed a novel MIN structure called MINDIC (MIN with Directory Cache switch). In this method, small temporary directories called directory cache(DC) are located only in switching elements that constitute the MIN, without providing directories on MMs. Since the directories are small enough to be implemented inside each switching element, there is no need of accessing external directory memories. Since the DCs must be implemented inside the switching elements, its size is limited. If the entry of the DC is full at the registration due to the lack of entry, a cache coherence problem for the cache line occurs. That is, invalidation messages for the cache line which could not be registered in the DC can't be generated. To cope with such cases, we proposed three different protocols. In our preliminary examination using a trace driven simulator, the eviction protocol achieved the best performance in the three protocols. Therefore, we evaluate the eviction protocol in detail using instruction level simulator. Our results show that MINDIC is equivalent to the architecture with full-mapped directories in execution performance.</p>		