

# SUMMARY OF Ph.D. DISSERTATION

School	Student Identification Number	SURNAME, First name  Ishikawa Ken-ichiro
<p data-bbox="167 443 231 477">Title</p> <p data-bbox="167 544 1093 577">A Study on Asynchronous Circuit using Bundled Data method</p>		
<p data-bbox="167 674 247 701">Abstract</p> <p data-bbox="178 719 1069 745">Recently, an asynchronous design using a state transition has received an attention.</p> <p data-bbox="178 772 1385 799">The asynchronous method has some advantages. In this study, the following two advantages are specially focused.</p> <ul data-bbox="167 826 1292 907" style="list-style-type: none"><li>- Each function block was processed without a synchronization of clock.</li><li>- Wasting time between an elapsed time of processing and a synchronized clock interval can be eliminated.</li></ul> <p data-bbox="167 934 678 960">In this study, two advantages below are focused.</p> <ul data-bbox="167 987 917 1068" style="list-style-type: none"><li>- Each function block processes without synchronizing.</li><li>- Each function block processes in each execution time for each process.</li></ul> <p data-bbox="167 1095 1029 1122">This study is moreover based on bundled data method in an asynchronous design.</p> <p data-bbox="167 1149 790 1176">Two major research products can be summarized as below.</p> <ol data-bbox="167 1202 1428 1494" style="list-style-type: none"><li>1. A pioneering asynchronous switch was designed, which processes all signals as an asynchronous manner, and its arbitration process and data transfer process are perfectly separated. A circuit simulation for this switch was made and it proved its 32-Gbps transfer rate. Actual switch chip and a printed circuit board for evaluating it were also implemented and confirmed the expected operation of this switch.</li><li>2. Speculative completion, which attains high-throughput calculation by changing the processing time appropriately according to each function block, was proposed by Nowick..</li></ol> <p data-bbox="167 1520 1428 1919">This study improved this speculative completion method and proposed new synchronous speculative completion that transfers a processing signal synchronized to the most dominant pipeline stage in processing time in order to enable further high-throughput calculation. If a target design does not have pipeline stage, this design might be assumed as one-stage pipeline structure for receiving the benefit of this new method. The evaluation of this method is done by applying CPU core. This evaluation proved that the throughput using this method can be extended to be 1.65 times faster than the original throughput. This synchronous speculative completion method in particular can improve the throughput when applied to a process that is activated only in limited conditions and extends the latency of its critical-path.</p> <p data-bbox="167 1946 1428 2130">This study described the bundled data method, which is the one of asynchronous circuit design method, and also described its application to a synchronized circuit for attaining high-throughput processing. These studies proved its efficiency by the actual simulation and implementations. Now, application area of the asynchronous design is limited. However, it is also expected to be widely used such as dynamic reconfigurable processors by this study.</p>		