SUMMARY OF Ph.D. DISSERTATION

School Integrated Design Engineering		SURNAME, First name TOMITA, Yasumoto

Title

A study on equalization and bidirectional transmission techniques for high-speed CMOS inter-chip communication.

Abstract: As the performance of CMOS ICs dramatically improves, the gap between the chip performance and I/O bandwidth is widening. This has made the I/O interface a primary bottleneck in many systems. To avoid this bottleneck, I/O data rates have been increasing into the multi-gigabit per second range and became to 10 Gb/s at 5 GHz. At higher date rates, however, frequency-dependent signal loss due to skin effect and dielectric losses cause inter-symbol interference, limiting the length of the transmission medium. The main objective of this dissertation is to study the equalization technique for long distance transmission such as back plane transmission, and bidirectional transmission techniques for improving the bandwidth of CMOS inter-chip communication.

Chapter 1 presents the motivation, background as the introduction of this dissertation.

Chapter 2 describes the equalization techniques. The equalizer circuit employs the feedback amplifier with two zeros by using capacitive source degeneration and inserting a pole in the feedback loop. It achieves high-bandwidth with small area and low power consumption, without using on-chip inductors. The implemented equalizer compensates for high-frequency losses ranging from 0 dB to 20 dB with a bit error rate of less than 10^{-12}.

In Chapter 3, we propose the channel response monitor to evaluate the equalizer performance. It measures the channel response including the wire and the equalizer by calculating the correlation between the error in the sampled input signal and the past decision data. A switched-capacitor correlator enables low power implementation of the monitor.

Chapter 4 shows the circuit technique for bidirectional transmission. The proposed circuit separates the incoming signal from line voltage and current without using a replica driver, which is used in conventional hybrid. It avoids the frequency characteristics and timing mismatch problem between the main and replica drivers, enabling a data rate of 20 Gb/s per differential pair. The fabricated transceiver operates at 20-Gb/s bidirectional transmission with a bit error rate of less than 10^{-12}.

Chapter 5 describes the conclusion.