SUMMARY OF Ph.D. DISSERTATION

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Title

Inductive Inter-chip Communication Interface

Abstract

In recent years, an intelligent terminal such as cellular phones and personal digital assistance spreads into the world, and a more high performance terminal is desired. A semiconductor chip which is required to be more high performance, low power, low cost, because the chip decides the terminal's performance. Conventionally, when implementing the system such as the terminal, the chip of processor, memory and discrete circuit were installed on the printed circuit board. However, there was two problems, one is that total performance is limited by a data transfer rate due to slow wiring on the board, the other is that a number of the chip on the board is limited due to the extra volume of package compared with the chip.

To solve these problems, the System on Chip (SoC) and System in Package (SiP) has been researched and developed. The SoC is the technology that all element of the system is fabricated in one chip. This technology has advantages that easy to increase the performance, because bus bandwidth is easy to increase due to large bus width and high-speed bus clock. Though, the chip using SoC technology costs high, because it requires the mixed fabrication process, such as analog, DRAM, and digital processes. In addition, its manufacturing yield becomes low compared with the SiP due to large implementation area. The SiP is the technology that more than one chips is implemented in one package. This technology allows to unifying the chips that is fabricated by different process into the one package. Moreover, the yield of the SiP becomes more higher compared with the SoC, because only known good die is used for the chips in the SiP. The wiring in the SiP is usually wire bonding or micro bump. These wiring 's bandwidth is not higher than SoC due to low clock frequency and small number of connection. In this research, to increase the bandwidth in the SiP, inductive inter-chip communication technology is proposed and investigated.

Chapter 1 is introduction. This chapter clarifies the meaning of this research by contrasting between the problem at conventional communication technology and the recent research in SiP.

In chapter 2, the idea of inductive communication technology in stacked SiP and its low power communication protocol are proposed. This technology uses on chip inductor as a communication channel. The communication is established between the inductors which are vertically aligned. Then, it is compared with capacitive communication scheme.

In chapter 3, the model of inductive coupling in stacked chip which has not been reported is proposed and investigated. Then this model is confirmed by measuring the fabricated chips. This measurement result and estimated result using proposed model agrees very well. From this result, it is found that proposed model is suitable for circuit design.

In chapter 4, the transmitter and receiver circuit is proposed. This circuit realizes the protocol which is described in chapter 2. H-Bridge circuit is applied for transmitter, a sense-amplifying flip-flop is applied for the receiver. And timing margin of transceiver circuit is discussed for low bit error rate.

In chapter 5, experiment of inter-chip communication is described. A test chip has been fabricated in 3 metal 0.35μm CMOS technology. This chip has been polished and stacked, then communication has been succeeded at 1.25Gbps communication rate with the distance of 300μm.Its power consumption is 43mW.

In chapter 6, scaling of inductive coupling communication technology is discussed based on constant magnetic field rule. This rule indicates that the bandwidth per area will be increase and energy per bit will be reduced by a factor of α^3 when the chip thickness is reduced as technology is scaled by α.

In chapter 7, conclusion is given. Results from each chapter are summarized.