SUMMARY OF Ph.D. DISSERTATION

School Integrated Design Engineering	Student Identification Number	SURNAME, First name YAMAMOTO, Tomonari

Title

Studies of Performance Enhancement in Sub-50nm CMOS Devices Using Laser Annealing Technology

Abstract

Our aim in this work is to demonstrate several new schemes of junction engineering technique for the reduction of source-drain parasitic resistance, and a novel poly-Si gate activation technique for the suppression of poly-Si gate depletion utilizing laser annealing technology. We have successfully integrated these techniques into the fabrication of sub-50nm CMOS devices, and actually achieved the performance enhancement of the devices.

In the chapter 2, we report source-drain engineering for the realization of low contact resistance between $CoSi_2$ and p^+ Si with low junction leakage current and low junction capacitance using Laser Thermal Processing (LTP) and the optimization of ion implantation conditions.

In the chapter 3, we report on the ultra-shallow junction profiles and good characteristics of sub-50nm CMOS devices with n^+/p^+ source-drain-extensions formed by LTP. By combining LTP with pre-amorphization and strong-dosage dopant-ion implantation, CMOS drive current can be improved without incurring a cost in terms of short-channel deterioration.

In this chapter 4, LTP was investigated as a gate pre-annealing technique and its advantages over RTA with regard to both gate activation and suppression of boron penetration were confirmed by evaluating the electrical characteristics of sub-40nm pMOSFETs.

In the chapter 5, we thoroughly investigated the impact of higher carrier activation using Laser Spike Annealing (LSA). We analyzed the source-drain parasitic resistance and the gate depletion suppression to demonstrate that LSA can improve on-currents while suppressing the short-channel effect in sub-40nm CMOS devices, compared to the conventional spike-RTA.

In the chapter 6, we demonstrate a new scheme of junction profile engineering technique that uses LSA: LSA is implemented prior to spike-RTA. With this technique, we can improve the performance of CMOS devices more effectively than conventional techniques.

In the chapter 7, we applied the technique described in the chapter 6 to 45nm node high performance CMOS technology. We have successfully integrated our newly developed junction engineering scheme into the leading-edge CMOS technology, and achieved a competitive performance of CMOS device.