SUMMARY OF Ph.D. DISSERTATION

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Title

A Study of High-throughput and Low-power Network-processor Architecture Exploiting Temporal Locality of Network Communication

Abstract

Network processors (NPs) are programmable devices that use many simple built-in processors to optimize packet processing on network equipment. Although next generation NPs will require even higher throughput, conventional NP architecture, in which the number of built-in processors is increased, would lead to excessive die size and power-consumption problems.

In response to these problems, I have proposed an alternative NP architecture called a "cache-based network processor" (CBNP) that realizes higher packet-processing throughput with low power consumption by using the locality of network traffic. Since data is divided into several packets and is transmitted in network, many packets that have the same header information tend to appear in a short period. The CBNP is equipped with a memory called a "process-learning cache" (PLC) and a relatively small number of built-in processors as its main logic. Only bottleneck processes such as table lookup of the first packet in every packet flow are processed by the built-in processors, and the results such as lookups are recorded in the PLC with commands for using them. The following packets that have the same header information are processed by using PLC contents without built-in processors. The CBNP also has a cache-miss handler that holds the following packets that arrive during PLC registration and then applies the contents of PLC in order to realize non-blocking PLC access.

A hardware emulator for the CBNP was developed to evaluate its packet-processing throughput with real network-traffic traces. The evaluation results demonstrate that CBNP can achieve a wire-rate packet processing when fitted with a 4K-entry PLC, 1K-entry CMH, and built-in processors that could provide about 10% of the line speed for the access network and 40% of the line speed for the core network. Moreover, according to an estimation of gate-level area and power consumption, the CBNP is expected to have an area and power consumption below half that of a conventional NP. We therefore expect that the CBNP is an applicable NP architecture for future network equipment requiring high throughput and low-power consumption.