SUMMARY OF Ph.D. DISSERTATION

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Title

A Study of Time-multiplexed Execution Models for Dynamically Reconfigurable Processors

Abstract

Field-programmable devices such as Field-Programmable Gate Arrays (FPGAs) allow us to implement any customized logic functions after chip fabrication and reuse the expensive silicon circuitry for different purposes. However, the FPGAs are generally perceived as area- and power-inefficient because they use a large number of transistors to provide high programmability. To cope with this problem, more cost- and power-aware dynamically reconfigurable processors have received attention as a flexible off-loading engine for versatile System-on-Chips (SoCs).

The dynamically reconfigurable processors have a two-dimensional array of 4-bit to 32-bit simple coarse-grained processing elements (PEs). Each PE has an internal memory to hold multiple circuit configuration data called a context, and PE operations and inter-PE connections can be dynamically reconfigured by rapidly switching contexts every clock cycle. In recent years, various architectures have been released, but a methodology or guideline to design an efficient architecture has not been established because of the wide design space compared to the FPGAs.

This dissertation describes hierarchical time-multiplexed execution models for dynamically reconfigurable processors and their evaluation results of performance, area cost, and power consumption. The goal of this study is to quantitatively evaluate the fundamental trade-offs and the area overhead associated with the time-multiplexed execution models and finally to provide a guideline for SoC designers to design area- and power-efficient architectures for a target application.

At first, the context-level time-multiplexed execution is characterized, and we propose an estimation method of performance and cost for various PE-array sizes. Evaluation result based on NEC Electronics' Dynamically Reconfigurable Processor (DRP) shows that the model can estimate the most area- and power-efficient PE-array size though there exist differences between the model and actual measurement. Next, the task-level time-multiplexed execution model, in which computational tasks can be switched on-demand, is investigated based on practical applications.

Finally, MuCCRA-1, which supports the hierarchical time-multiplexed execution models, is implemented in Rohm 180nm CMOS technology, and its performance and area overhead are evaluated. On a 5.18mm-squared die, 4 x 4 24-bit PE array, four multipliers, and four distributed memory modules are implemented. Each PE has a 64-depth context memory, and the context and task switches are controlled by efficient control mechanisms. Evaluation result demonstrates that the area overhead required for the control mechanisms of time-multiplexed execution models is only about 1.3% of the total area. In contrast, the area of a context memory in each PE amounts to 55.7% of the PE area.