SUMMARY OF Ph.D. DISSERTATION

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Title

Study of advanced plasma etching of polysilicon gate

Abstract

To manufacture advanced complementary metal oxide semiconductor (CMOS) logic chips, in the gate etching plasma process, gate length variances should be maximally controlled and anomalous erosion gate profiles caused by plasma charging should be maximally suppressed. We have mainly focused on model-based advanced process control used SO2-O2 gas mixtures plasma for a photoresist trimming in the gate etching process, and plasma charging phenomena on gate line pattern.

Chapter 1 is the introduction of this study, and describes the current statuses of sub-100nm gate fabrication using plasma, the motivation, and the subject of this study.

Chapter 2 describes structure of inductively coupled plasma gate etcher, the poly-silicon gate etch process flow for sub-100 nm gate transistors, and the effect of SO2 gas in the photoresist trimming O2 plasma. Adding SO2 gas to O2 gas trimming plasma improves the difference of isolated line pattern to dense line pattern etching loss.

Chapter 3 describes a new advanced process control (APC) technique, available to achieve no pattern-layout-dependence, for reducing lot-to-lot post etch gate linewidth variation. The process model, adapted in our APC system, is a linear relationship between etch gate linewidth bias as a function of SO2/O2 mixture ratio at a constant over etch time. It has a ±6nm of controllable range of etch gate linewidth bias with the its iso-to-dense difference within ±1nm. Using the APC technique, a 9.08 nm spread of variations in the pre etch gate linewidth with a 2.00 nm standard deviation of 1σ and a 2.49 nm spread of variation in the post etch gate linewidth with a 0.55 nm standard deviation of 1σ were obtained, and 92% of the processed lots were in the range of ±1nm from a target. We confirmed that the APC system works well. At that time, we used feedback control by the persistence prediction method using the etch gate linewidth bias for the pilot wafer from the currently processed lot, the standard deviation of the prediction error was 0.5 nm of 1σ, and the prediction error accounts mainly for the APC system error.

Chapter 4 describes in-situ measurement of plasma and surface chemistry for organic resist etching in an inductively coupled plasma in SO2-O2 gas mixture. We experimentally investigated the etch linewidth bias of photoresist pattern and its relation to the etch products and chemical compositions of the photoresist surface, as a function of gas mixture ratio between SO2 and O2. As the SO2 percentage increased, the etch linewidth bias of photoresist pattern decreased and the amount of sulfur in the higher oxidation sate of SO4 increased. We think that the sulfur acted as a passivation layer and the increase in the amount of sulfur mainly caused the decrease in the etch linewidth bias of photoresist pattern.

Chapter 5 describes the in-situ measurement of plasma charging on a dielectric line pattern formed on a Si substrate. We measured the electron and ion currents going into the Si substrate through the dielectric structure. When the pattern size decreases, the electron current is suppressed and the floating potential increases. We also measured the change in the floating potential difference between samples with different pattern sizes (namely charging voltage) as a function of electron temperature. As the electron temperature is increased from 2 eV to 4 eV by controlling gas pressures, the floating potential difference increases. This suggests that a plasma at lower electron temperature is more suitable for gate etching plasma processing.

Chapter 6 summarizes the results of the present study.