No

Thesis Abstract

				10.
Registration	□ "KOU"	□ "OTSU"	Name	Vasutan Tunbunheng
Number	No.	*Office use only		
Thesis Title				
A Study on Representation Model for Coarse-Grained Dynamically Reconfigurable Systems				
Thesis Summary				

Recently, dynamically reconfigurable architectures become popular and widely researched. It can achieve high computing performance as well as low power consumption, which is important in portable device such as MP3 players, mobile phones, portable game engines, and cameras for saving battery. Various architectures have been proposed and they require compilers to generate configuration data for evaluating the architectures at design time. Retargetability is important for a compiler or synthesis tool used for architecture exploration. If the compiler can be used for multiple target architectures, it can save the time to develop a compiler for every architecture. This kind of compiler is called "retargetable compiler". However, most of traditional retargetable compilers provide flexibility to customize the target architecture by selecting parameters and options. Thus, architecture designers still have to spend time to modify compiler code when the available options do not support the brand new architecture.

This research focuses on representation model which can be used to customize different target architectures without modifying the compiler itself. *Graph with Configuration Information (GCI)* is proposed to represent reconfigurable resources in Dynamically Reconfigurable Processor Arrays (DRPAs). The functional unit, constant unit, register, and routing resource can be represented in the graph as well as the configuration information.

A prototype compiler called Black-Diamond with GCI is now available for three different DRPAs. It translates data-flow graph from C-like front-end description, applies placement and routing by using the GCI, and generates configuration data for each element of the DRPA. Evaluation results of simple applications show that Black-Diamond can generate reasonable designs for all three different architectures. Other target architectures can be easily treated by representing many aspects of architectural property into a GCI.