Adjacent Channel Interference Mitigation Schemes for Software Defined Radio Receiver

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Abstract

Wireless communication technology such as cellular and wireless local area network (WLAN) systems have grown rapidly and generated various competing transmission formats. In the need of seamless communication across incompatible radio standards, software defined radio (SDR) concept has received much attention among researchers working in mobile and personal wireless communications. SDR is a technology that allows a single terminal to support various kinds of wireless systems and services such as mobile systems and WLANs by changing software to reconfigure the wireless terminal. In order to realize a SDR receiver, flexible receiver architecture with wideband signal receiving capability is required. However, if the receiving bandwidth is wider, the received signal components may cause interference to each other. In this study, the signal processing methods to combat the adjacent channel interference (ACI) problems in the SDR receivers are investigated and discussed.

In this dissertation, we use 2 approaches to realize the flexible receiver for SDR;

1. Low-IF signal mixing downconversion receiver architecture
2. RF sampling receiver architecture

In the low-IF receiver, received radio frequency (RF) signal is mixed down to a non-zero low or moderate intermediate frequency (IF). The low-IF receiver is superior to conventional superheterodyne receiver as the architecture does not require external filter. The low-IF receiver does not suffer much from its non-idealities, such as DC-offset and 1/f noise problems in direct-conversion receiver (DCR). In the RF sampling receiver architecture, the received signal is sampled at a RF and is processed

directly at the analog domain. The downconversion technique in the RF sampling is based on current sampling, which greatly simplifies the mixer circuit design. These architectures achieve reduction of off-chip components and enable the realization of a one-chip receiver.

This dissertation is focusing on signal processing methods to combat ACI problems in The SDR receiver. In the 2nd chapter, the interference from the mirror frequency in a multi channel low-IF receiver is discussed. In the wideband low-IF receiver, a high resolution analog-to-digital converters (ADCs) should be employed to accommodate signals with a very large dynamic range. Moreover, the ACI component may directly overlap with the desired signal if the interference is much larger than the desired signal. In the 3rd chapter, the effect of ACI due to undersampling to the multi channel low-IF receiver is investigated and discussed. The 4th chapter investigate the methods to mitigate the ACI effect due to a sample rate conversion in an RF-sampling receiver.

Chapter 1 introduces the background of the SDR and the motivation of the research.

In Chapter 2 a new ACI cancellation scheme for multi-channel signal reception with low-IF receivers is investigated through the experiment. In the low-IF receivers, the signal in the mirror frequency causes interference to the desired signal. A high resolution ADCs should be employed to accommodate signals with a very large dynamic range. Moreover, the ACI component may directly overlap with the desired signal if the interference is much larger than the desired signal. In order to reduce the required resolution of the ADCs and reduce the interference, an analog-digital signal processing technique has been investigated . This technique uses a band pass filter (BPF) for each WLAN channel. The BPFs ease the dynamic range of ADCs and enables multi-channel demodulation with low resolution ADCs. Nevertheless, the problem of the analog BPFs is that it cannot eliminate the interference completely

due to the restriction of the circuit size and the mismatch of the analog components. In the proposed analog-digital signal processing scheme, channel selection is made by analog complex band pass filter and the signal is reconstructed by Wiener filter to eliminate the interference effect in order to improve the performance.

In Chapter 3 an ACI cancellation scheme with undersampling for multi-channel reception is proposed and investigated. The main objective of Chapter 3 is to improve the system that has been proposed in Chapter 2 by reducing the ADC sample rate requirement. Undersampling technique is applied in this system in order to reduce the required sampling frequency and power consumption. However, the undersampling technique requires high performance BPFs to minimize the out-of-band signals, otherwise, the out band signal will be aliased and translated to the desired band. The effects of the adjacent channel to the undersampling technique in this scheme is examined and discussed in the chapter. In the proposed scheme, the influence of the undersampling side effect is reduced by the Wiener filter.

Chapter 4 proposes a new fractional sample rate conversion (SRC) scheme for the RF-sampling receiver architecture. This scheme is suitable for signals that are sampled at a high sample rate and converted to a lower sample rate. The objective of the scheme is to realize a high-speed and high-performance SRC scheme with low-complexity and lower power consumption. High-speed SRC scheme for high sample rate data can be realized by a direct insertion/cancellation scheme. This technique is suitable for application in the RF sampling receiver which samples data with a high oversampling ratio (OSR). However, the direct insertion/cancellation technique suffers from large aliasing and distortion as compared to the other SRC techniques. The aliasing from an adjacent channel interferes the desired signal and degrades the performance. Moreover, the aliasing from the adjacent channel interferes the desired signal. Therefore, a modified direct insertion/cancellation scheme is proposed in order to realize high performance resampling. The distortion noise or aliasing can be

reduced by applying multiple branches of parallel inserters/deleters. This proposed scheme mitigates the ACI, reduces the required complexity of an anti-aliasing filter structure, and improves the performance.

Finally, Chapter 5 summarizes the results of each chapter and conclude this thesis.

Chapter 1

General Introduction

In this chapter, first, we introduce the concepts of software defined radio (SDR). Then we present the receiver architectures that has been proposed for SDR. After that, we show some sampling concept in ADCs and sample rate conversion (SRC). Then, the issues related to the adjacent channel interference (ACI) in the receiver architecture are presented. Finally, the motivation of the research is presented in the final section. The section also explains the relationship among each chapter and the historical background of each chapter.

1.1 The Need for Reconfigurable Radio Architectures

Wireless communication is now routinely used for a large variety of applications including voice, data transfer, Internet access, audio and video streaming. Due to the demand for bandwidth and the steady improvement of semiconductor technology, the performance offered by wireless standards is improving rapidly every years, seemingly without bounds, as illustrated in Fig. 1.1. The observed and predicted evolution of the main classes of wireless standards is indicated as thick arrows (from bottom to top): wireless personal area networks (WPAN), wireless local area networks (WLAN), wireless metropolitan area networks (WMAN), and cellular networks.

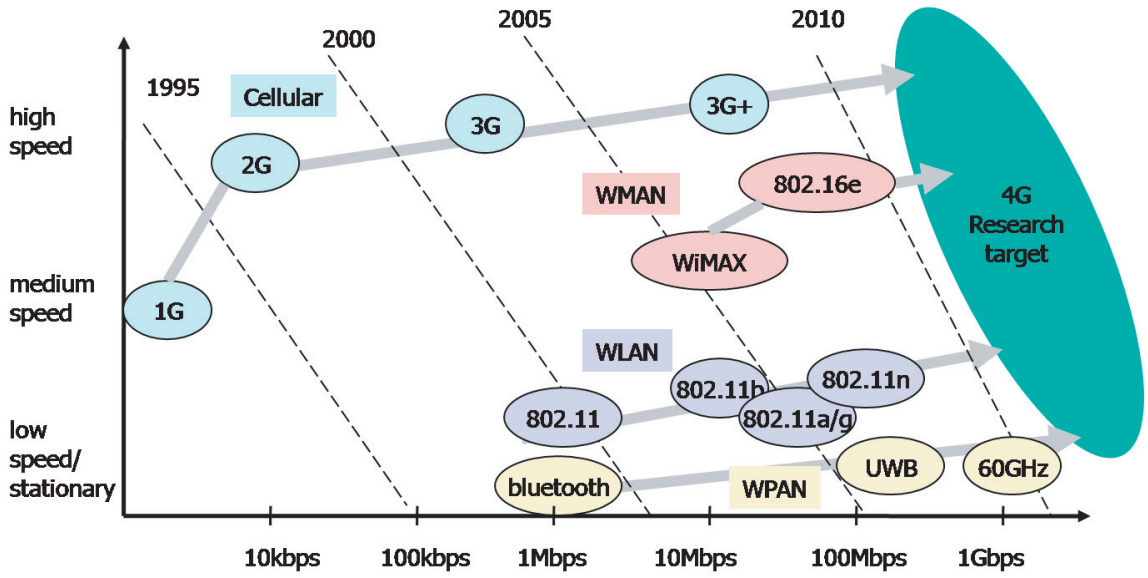

Figure 1.1: Wireless standards.

Future communications systems will have to seamlessly and opportunistically integrate these multiple radio technologies. In the future communications systems, a single handheld device that can support a large number of these wireless standards enabling ubiquitous connectivity through seamless horizontal and vertical handovers. This is supported by SDRs, which use a common hardware platform for different standards [1, 2].

1.2 Software Defined Radio

Wireless communication technology such as cellular and WLAN systems have grown rapidly and generated various competing transmission formats. In the need of seamless communication across incompatible radio standards, SDR concept has received much attention among researchers working in mobile and personal wireless communication. SDR is a technology that allows a single terminal to support various kinds of wireless systems and services such as mobile systems and WLANs by changing software to reconfigure the wireless terminal [1–3]. SDR technology enables ubiqui-

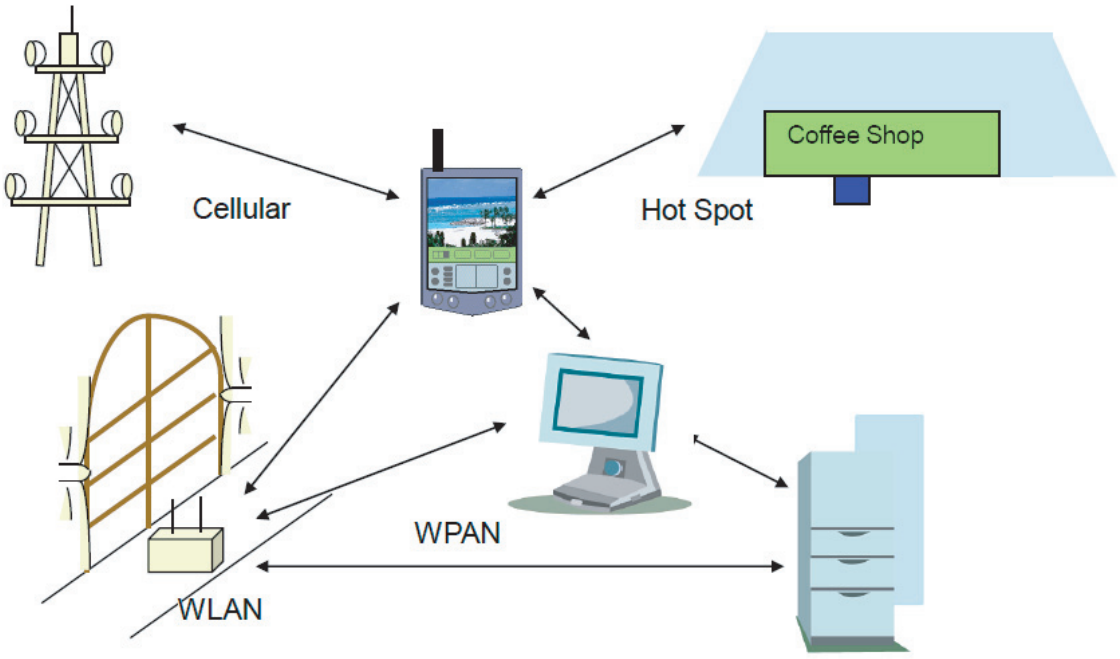

Figure 1.2: Ubiquitous wireless communications with SDR.

tous data connectivity by supporting multi-band and multi-mode wideband wireless terminal, as illustrated in Fig. 1.2. Seamless communication could be possible by selecting the wireless system that best corresponds to the communication environment and user's requirements. Desired quality of service can be maintained while improving service economy based on the data-rate and communication fee, etc.

There are several merits by using SDR technology. One terminal can be used for various wireless systems such as cellular, WLAN, WMAN, WPAN, TV, ITS, GPS, etc. New services can be provided and obtained by software version upgrade without replacing infrastructures and terminals. Therefore, there are no need to replace all terminals when new services is launched. In-service systems can be remotely maintained. The development period will be shorten because there are no longer need to develop specific chips for each system.

In order to realize the SDR terminal, radio frequency (RF) circuit that support multi-band signal, flexible baseband signal processing to support multi-band, multi-

standard and multi-mode system, and high resolution high speed analog-to-digital converter (ADC) to counter fading and ACI, are needed. The combination of the flexibility of signal processing with RF circuitry to allow software to dynamically control communications parameters such as carrier frequency, bandwidth, power levels, and data rate. In addition, the software at the heart of the systems can perform functions such as filtering signals, establishing modulation and coding schemes, and determining frequency-hopping patterns.

1.3 Receiver Architectures

The ideal concept for the SDR terminal is to attach an ADC directly to the antenna such as shown in Fig. 1.3 [1]. However, the ideal scheme is not completely realizable due to the actual technology limits; especially the need of ultra high speed ADC cannot be realized by the current technology.

Figure 1.4 shows current ADC architectures with their resolution and sampling rate. At sampling rates below 2MHz, resolution appears to be limited by thermal noise. At sampling rates ranging from 2MHz to 4GHz, resolution falls off by 1 bit for every doubling of the sampling rate. This behavior may be attributed to uncertainty in the sampling instant due to aperture jitter. For ADCs operating at multi-GHz rates, the speed of the device technology is also a limiting factor due to comparator ambiguity [4]. Many ADC architectures and integrated circuit technologies have been proposed and implemented to push back these limits. The trend toward single-chip ADCs brings lower power dissipation. However, technological progress as measured by the product of the ADC resolution (bits) times the sampling rate is slow. Even the ADC technology grows, it is still far from the requirement of the ideal SDR terminals. Therefore, trade-offs between the ideal SDR and the available technology must be made. The actual practical solution is to let the software processing stage be preceded

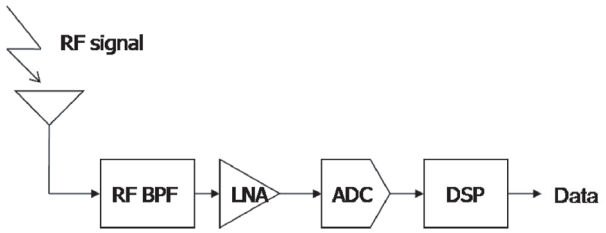

Figure 1.3: Ideal SDR concept

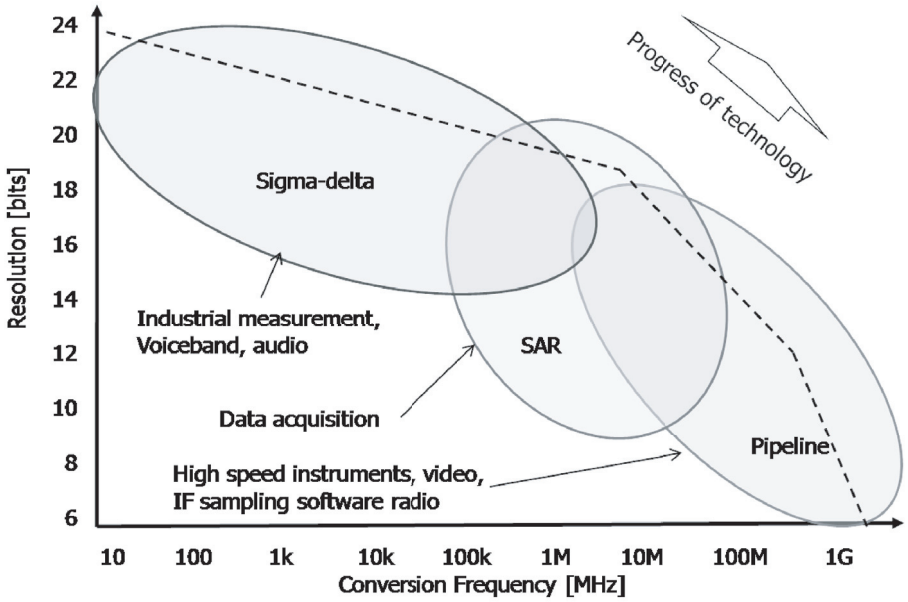

Figure 1.4: ADC architecture, application,resolution and sampling rates.

by a front-end that preconditions the input signals to give them characteristics that enable the subsequent stage to elaborate them.

1.3.1 Superheterodyne Receiver

A superheterodyne RF front end architecture is adopted to lower the frequency of the received signals to intermediate frequency (IF) values. The superheterodyne receiver, which was introduced by Armstrong in 1918 [5], has been used in radio and television receivers and transmitters in order to tune them to a particular frequency. A typical structure of the superheterodyne receiver architecture, consists of a RF filter, low noise amplifier (LNA), multiple down-conversion mixers, off-chip passive

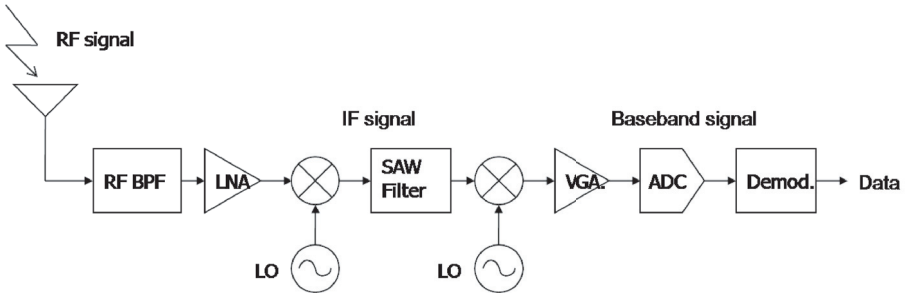

Figure 1.5: Superheterodyne receiver architecture.

image rejection filter, and variable-gain amplifier (VGA), as illustrated in Fig. 1.5.

The superheterodyne receiver downconverts the received RF signal to a fixed IF, by mixing all of the incoming signals with an internally generated waveform, using a single mixer and tunable local oscillator (LO). In the mixer stage of a receiver, the LO signal multiplies with the incoming signals, which shifts them all down in frequency. After the down-conversion mixer, a passive off-chip channel select filter attenuates the out-of-channel signals to a sufficiently low level. A VGA, which follows the IF channel-select filter, decreases the dynamic range requirements of the ADC. Then, the desired signal is downconverted to the baseband before it is converted to a digital signal by an ADC.

A super-heterodyne receiver heavily relies on expensive external, high-Q passive filter to perform the mirror signal suppression and the channel selection [6]. These high-Q filters cannot be integrated on silicon because the power consumption of active filter is proportional to the the square of its quality-factor. These filters usually realized with off-chip surface acoustic wave (SAW) filter. Although the filtering functions themselves do not consumed any power, the input and output of each off-chip filter requires impedance matching that increases the power consumption in the RF front-end. Although the off-chip filters offer sufficient image rejection and selectivity, the superheterodyne implementation of a multimode receiver with such filters will not only increase the production cost but also the physical dimension of the handset.

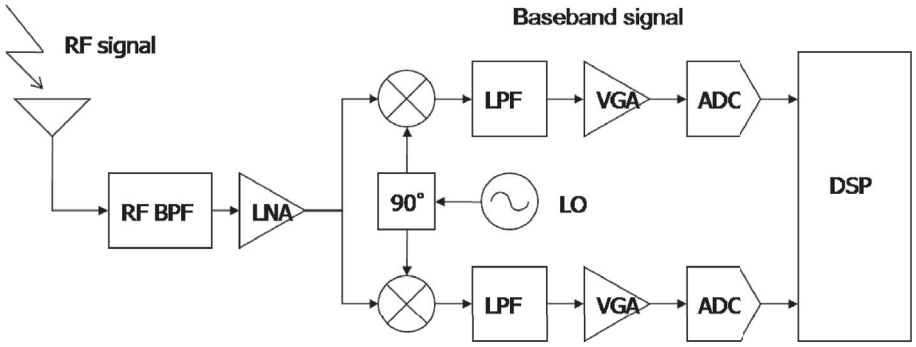

Figure 1.6: Direct conversion receiver architecture.

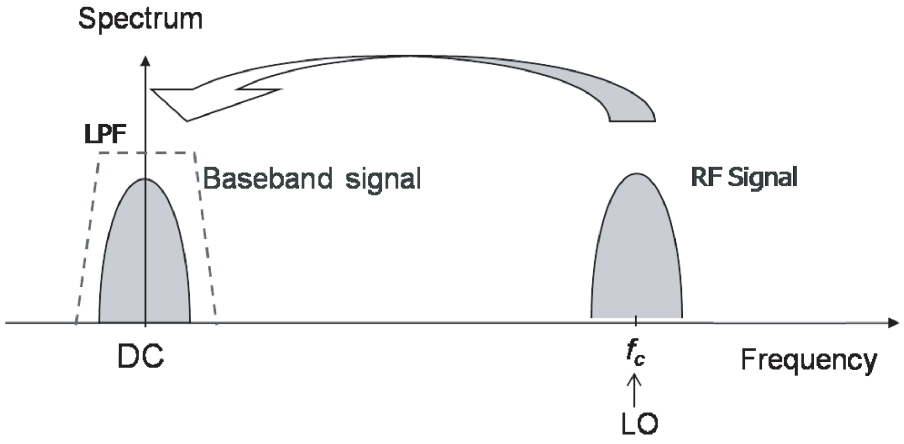

Figure 1.7: Downconversion in DCR.

Thus, superheterodyne receiver is not a practical topology for multimode receiver designs.

1.3.2 Direct Conversion Receiver

Direct conversion receiver (DCR) architecture, which has introduced the zero IF approach, supports efficient wireless terminal designs with a high level of integration [7,8]. In the DCR, the desired signal downconverted directly to baseband signal with only single conversion stage. The elimination of components and processing in IF stage had greatly lower complexity and power consumption in the DCR architecture.

The receiver, shown in Fig. 1.6 [6], consists of a RF filter, LNA, quadrature down-conversion mixers, low-pass filters (LPFs), and VGAs. The RF filter attenuates the

out-of-band signals before the LNA. The architecture uses quadrature modulation, two down-conversion mixers are required to avoid an unrecoverable loss of information. The LO signals of the two mixers have a phase shift of 90° which produces the in-phase (I) and quadrature (Q) components. There are no need for an off-chip filter in the DCR architecture, since both the mirror signal and the noise will eventually be neutralized by the recombination of the two signal paths after the quadrature down-conversion. After the downconversion mixers, the signal is at baseband where the channel selection is performed by integrated LPFs. Following, VGAs are utilized to amplify the baseband signal to a suitable level.

The downconversion is done in a single step in two signal path, instead of a cascade of mixing stages, as illustrated in Fig. 1.7. Further signal processing such as image rejection demodulation of the signal is carried out in the digital domain by a DSP. This is an attractive property, since the digital domain features a much better scalability and a great flexibility.

However, there are direct current (DC) offset and 1/f noise problems in the architecture [7, 9]. The offset arises from the self-mixing of the LO and the self-mixing of undesired interferer in the preselect filter passband. The DC offset, which appears in the middle of the downconverted signal spectrum, and may be larger than the signal itself, and much larger than thermal and 1/f noise. The DC offset will reduce the signal-to-noise ratio (SNR) at the detector input and degraded the performance. The 1/f noise or flicker noise is an intrinsic phenomenon found in semiconductor devices. the 1/f noise, which has spectral density that is inversely proportional to frequency, distort the signal that is nearer to the DC.

1.3.3 Low-IF Receiver

Low-IF receiver architecture has been proposed to avoid DC offset and 1/f noise problems in the DCR [10]. In a low-IF receiver, the RF signal is mixed down to a

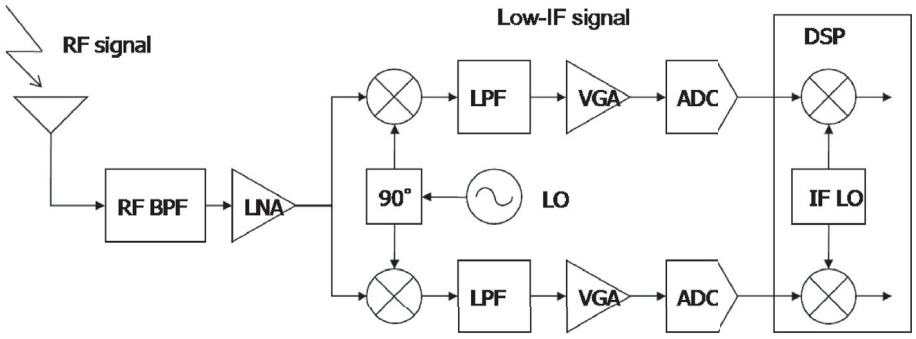

Figure 1.8: Low-IF receiver architecture.

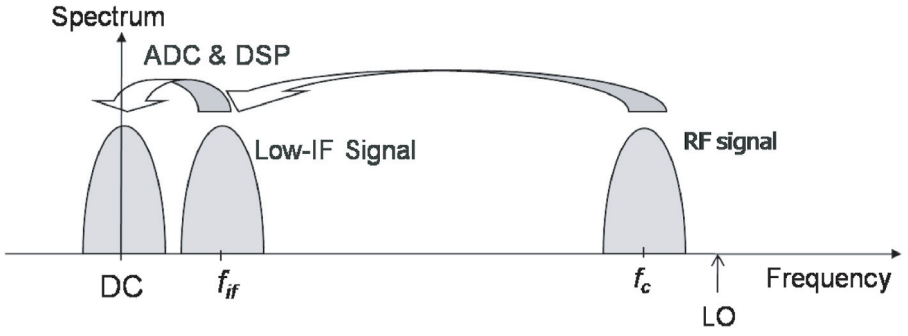

Figure 1.9: Down conversion of the received signal in low-IF receiver architecture.

non-zero low or moderate intermediate frequency, typically a few megahertz. The structure of the low-IF receiver is shown in Fig. 1.8. Received signal through antenna goes through band-pass filter. A broadband RF filter is used to prevent overloading of the mixers with strong out of band signals. The LNA amplifies the weak signal from antenna to a sufficient SNR. In low-IF receiver architecture, the received signal is down converted to the IF signal by mixing the signal with LO, such is shown in Fig. 1.9. Then the IF signal is converted to digital signal with ADCs and finally converted to the baseband signal using DSP. As the down conversion is carried out with DSP, channel selection can be done easily.

The advantages of this topology consists in the high level of integration and the lack of DC offsets as in the case of zero IF receiver. DC can be easily decoupled after

down conversion. The second IF is at low frequency and digital signal processing is possible. Low-IF receivers are not using SAW filter so that this architecture would have low cost and low power consumption as compared to super-heterodyne architecture. The low-IF receiver is much easier to make in one chip and the structure of the low-IF receiver can be much simpler than the super-heterodyne receiver.

Receiver system with the low-IF receiver architecture is described in Chapter 2 and 3.

1.3.4 RF-Sampling Receiver

Direct RF-Sampling Receiver

The RF-sampling receiver scheme has been proposed recently to replace the conventional mixer-based downconversion scheme. The direct RF sampling technique is based on current sampling, which greatly simplifies the mixer circuit design. In the RF-sampling architecture, the received signal is processed directly at the analog domain and sampled at the RF [11, 12]. Channel selection and demodulation are carried out in the digital domain [13]. This architecture achieves the reduction of off-chip components and enables the realization of a single-chip receiver. RF-sampling receiver, which supports single chip and multi-mode designs, is a promising architecture for the next generation wireless terminals to realize a flexible wireless terminals with smaller physical dimensions.

The structure of the RF-sampling architecture is shown in Fig. 1.10. The received signal is sampled at the same frequency of the carrier signal at the downconversion sampler to perform downconversion. This is followed by the decimation and filtering processes. Switched-capacitor (SC) circuits are often used to perform discrete-time operations in the analog domain [14]. Since the SC circuits sample a time-continuous input signal, no additional sample-and-hold (S/H) circuit is needed in the ADC. the SC circuits can be employed for signal sampling, downconversion, filtering, and

decimation [15].

The discrete signal is sampled at a high sample rate of the ADC. In the digital domain, digital signal processing and SRC are performed.

System model in Chapter 4 is using the RF-sampling receiver architecture.

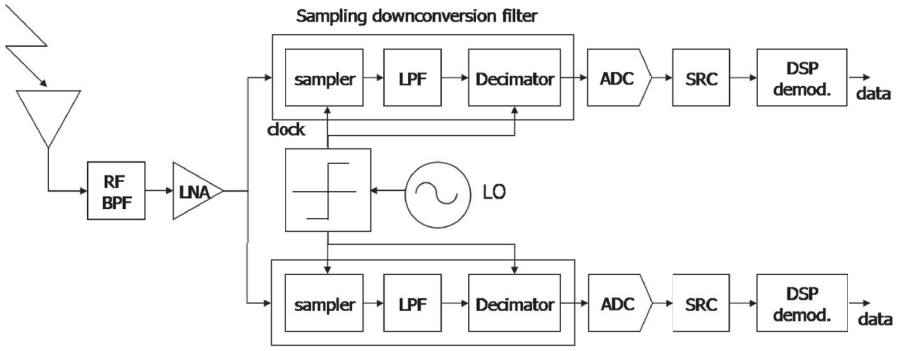

Figure 1.10: RF-sampling receiver architecture.

Discrete Time Receiver by TI

The RF-sampling receiver scheme has been presented as discrete time receiver in CMOS technology by Texas Instruments (TI) for Bluetooth radio application [16, 17]. The block diagram of the receiver is shown in Fig. 1.11. The analog front-end (AFE) comprises a continuous-time RF amplification stage followed by a discrete-time sampler and filter. The analog back-end (ABE) comprises a nonsettling IF amplifier followed by a sigma-delta ADC. The LO is generated by all-digital PLL (ADPLL).

At the AFE, the received signal is amplified in the LNA, split into / paths, and converted into current using a transconductance amplifier (TA) which are referred as a low-noise transconductance amplifier (LTNA). The input signal is sampled at the Nyquist rate of the RF carrier and follows by decimation and anti-aliasing filtering functions. This operation is performed by a multi-tap direct-sampling mixer (MTDSM). The MTDSM comprises switched capacitors that receive timing signals from the digital control unit (DCU) that generates clocks for the AFEAs. The DCU

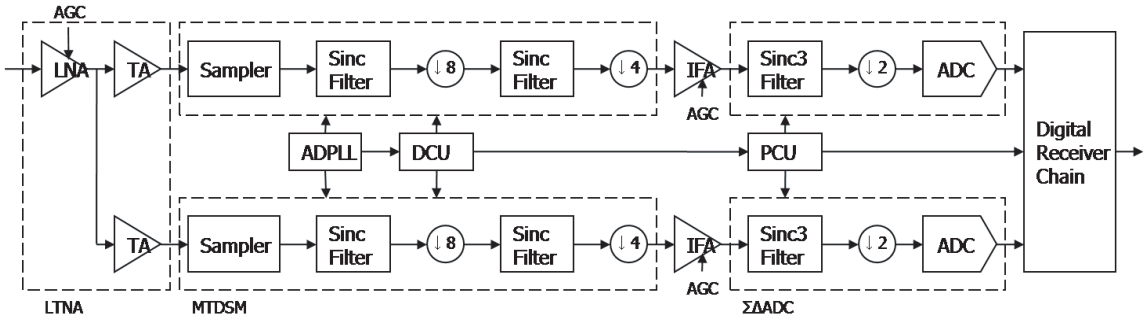

Figure 1.11: Block diagram of the DTR by TI.

generates all the clock signals for analog circuits.

At the ABE, a discrete-time IF amplifier (IFE) provides single-pole filtering in addition for anti-aliasing filtering. The IFA is implemented as a nonsettling switched capacitor amplifier with an embedded single stage IIR filtering running at a rate of LO/32. In the sigma-delta ADC, anti-aliasing filtering is performed using a third-order sinc filter, which is implanted using only capacitors and switches. The ADC operates at half the rate of the IFA for reduced power consumption.

1.4 Sampling in ADC and Sample Rate Conversion

The placement of the A/D interface is the key of SDR receiver. The ADC has to be placed closer to the antenna to realize the ideal SDR. However, current technology limits the performance of ADC, thus the ideal SDR cannot be realized for high frequency signal. As this thesis deals with sampled signals, it is necessary to understand how these signals are obtained. The analog-to-digital conversion process takes places in two steps: quantization and sampling. In signal processing, sampling is the reduction of a continuous signal to a discrete signal. A sampler is a subsystem or operator that extracts samples from continuous signal. If this signal is then discretized (i.e., converted into a sequence) and quantized along all dimensions it becomes a discrete

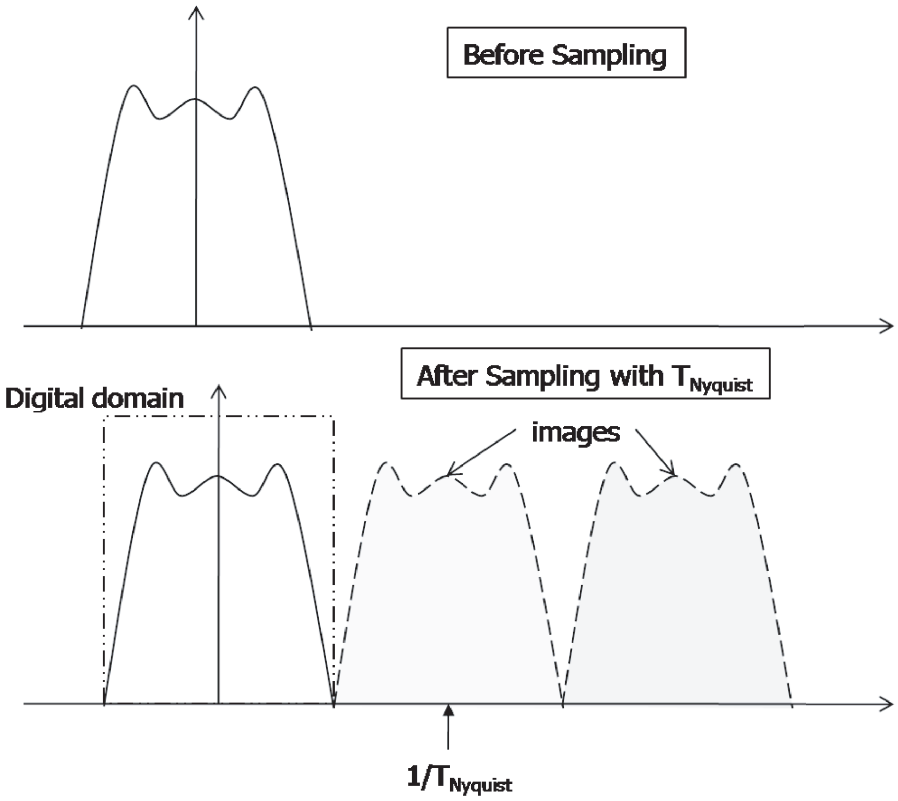

Figure 1.12: Spectral characteristics of Nyquist sampling.

signal. Sampling is performed by measuring the value of the continuous signal every T_s seconds. For instance, when a continuous signal is sampled, $x(t)$, the sampled signal $x[n]$ given by,

$$x[n] = x(nT), n = 0, 1, 2, 3, \ldots \tag{1.1}$$

The sampling frequency or sampling rate f_s is defined as the number of samples obtained in one second, or $f_s = 1/T$.

1.4.1 Nyquist Sampling

A signal which contains high frequency components is needed to be sampled at a higher rate to avoid losing information that is in the signal. In general, it is necessary to sample at twice the maximum frequency of the signal, to preserve the full information in the signal. This is known as the Nyquist rate, $f_{Nyquist}$. The Sampling

Theorem states that a signal can be exactly reproduced if it is sampled at a frequency that is greater than twice the maximum frequency in the signal [18–20]. The sufficient condition for exact reconstructability from samples at a uniform sampling rate is represent as,

$$f_s \geq f_{Nyquist}, \tag{1.2}$$

$$f_{Nyquist} = 2B, \tag{1.3}$$

where B is the one-sided baseband bandwidth of the bandlimited signal, $x(t)$

To formalize the sampling concepts, the continuous Fourier transform $X(f)$ of the continuous-time signal $x(t)$ is defined as

$$X(f) = \int_{-\infty}^{\infty} x(t)\ e^{-2\pi i f t}\ dt. \tag{1.4}$$

Sampling the signal $x(t)$ with sampling period T_s causes a repetition of the spectrum $X(f)$ at integer multiples of $1/T_s$. This effect is called imaging, the spectral copies are called images. As long as the sample rate is larger than twice the highest frequency component of $X(f)$, there is no overlap of the images, as illustrated in Fig. 1.12.

Aliasing

As the sampling frequency decreases, the image signal separation also decreases. If the sampling frequency lower than the Nyquist rate, then frequencies above Nyquist rate will be reconstructed as image signal, and appear at the frequencies below the Nyquist rate such as illustrated in Fig. 1.13. In the figure, the baseband signal is sampled at $f_s = 1/T_A$ which is lower than $f_{Nyquist}$. The resulting distortion is called aliasing; as the reconstructed image signal is an alias of the original signal, in the sense that it has the same set of sample values. Aliasing can be avoided by either increasing the sample rate or by filtering the inband high frequencies prior to sampling.

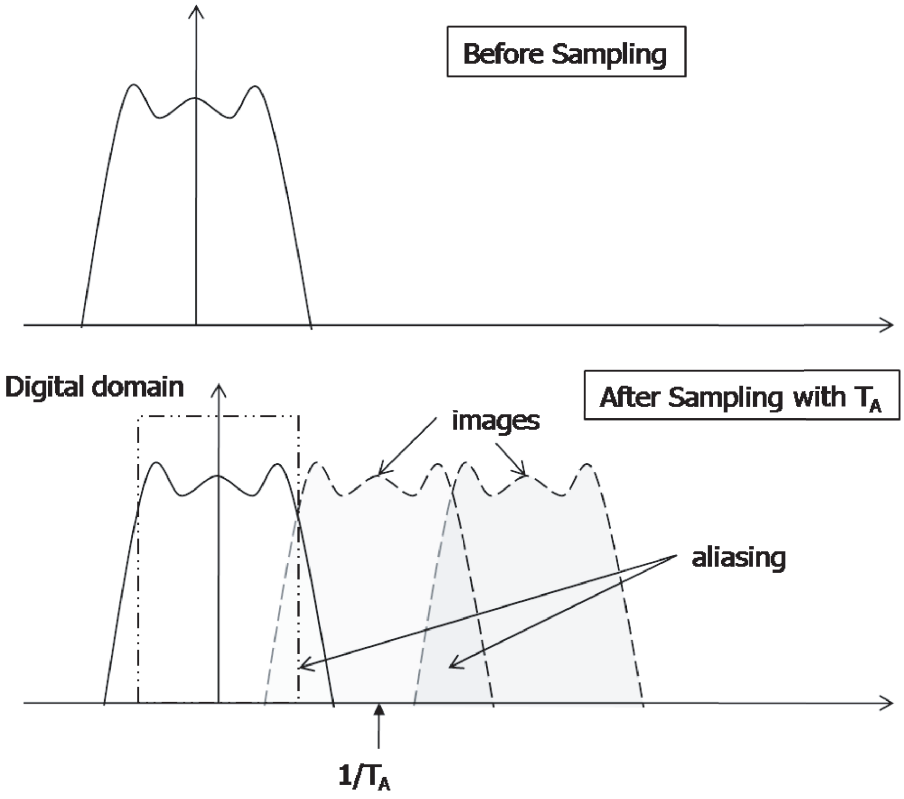

Figure 1.13: Spectral characteristics of $f_s < f_{Nyquist}$.

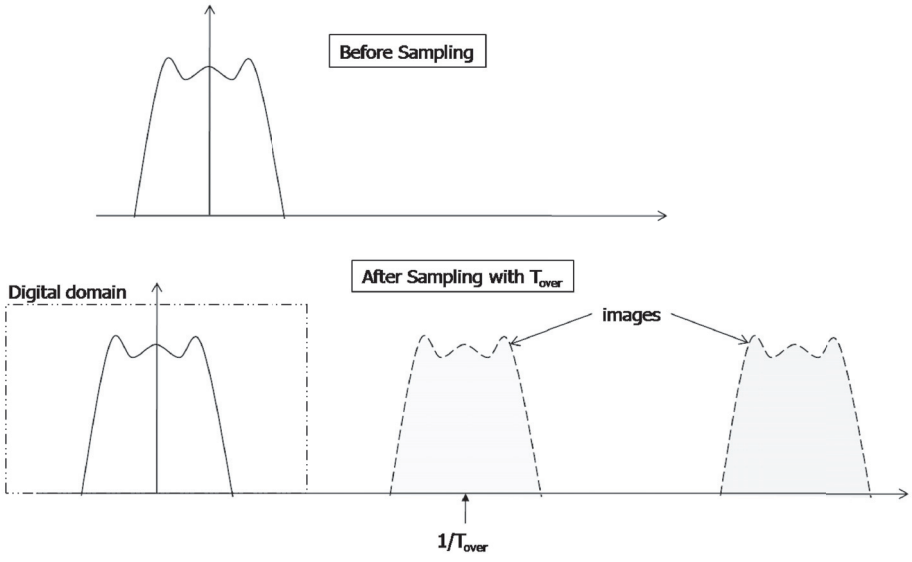

Figure 1.14: Spectral characteristics of oversampling, OSR=2.

1.4.2 Oversampling

Oversampling is the process of sampling a signal with a sampling frequency significantly higher than twice the bandwidth or highest frequency of the signal being sampled. The oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{f_{Nyquist}} \tag{1.5}$$

which means an oversampled signal is be oversampled by a factor of OSR. The spectral characteristics of a oversampled signal is shown in Fig. 1.14. In the figure, the baseband signal is sampled at $f_s = 1/T_over$ which is 2 times higher than $f_{Nyquist}$. There are wide separation between the image signals.

Oversample aids in anti-aliasing because realizable analog anti-aliasing filters are very difficult to implement with the sharp cutoff necessary to maximize use of the available bandwidth without exceeding the Nyquist limit. The anti-aliasing filter has less complexity and can be made less expensively by relaxing the requirements of the filter at the cost of a faster sampler. Once sampled, the signal can be digitally filtered and downsampled to the desired sampling frequency. In modern integrated circuit technology, digital filters are much easier to implement than comparable analog filters of high order. In practice, oversampling is implemented in order to achieve cheaper higher-resolution ADC and DAC. Oversampling can also reduce or cancel noise. If multiple samples are taken of the same quantity with a different (and uncorrelated) random noise added to each sample, then averaging N samples reduces the noise variance (or noise power) by a factor of 1/N. The SNR improves with 3.01dB per doubling the OSR, which equivalent to 1/2-bit quantizer resolution.

The sytem that is described in Chapter 4 is using oversampling.

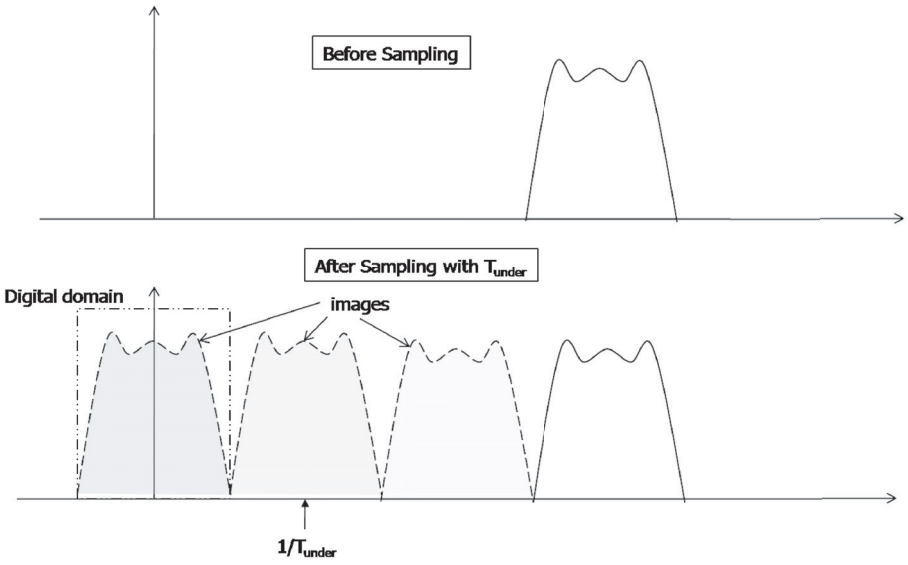

Figure 1.15: Spectral characteristics of undersampling.

1.4.3 Undersampling

If a bandlimited non-baseband high-frequency signal is samples with a lower sample rate than the Nyquist rate, such as shown in Fig. 1.15, images signal will be generated at the lower frequency. In the figure, the high frequency bandlimited signal is sampled at $f_s = 1/T_under$ which is 3 times lower than $f_{Nyquist}$. The non-baseband signal can be sampled with sampling frequency below Nyquist rate by using the undersampling technique [21]. The undersampling or bandpass sampling translates a high frequency bandpass signal to a near zero lowpass frequency such as shown in Fig. 1.16. The sampling frequency requirement is based on the signal bandwidth rather than its highest frequency. In the undersampling, the aliasing phenomenon is exploited to enable the ADC to sample the signal using a rate that intentionally aliases the high frequency signal into the operating range of the ADC.

Any out of band signal or noise must be kept to minimum because they will fold down to the desired signal band. A band pass filter (BPF) of very high Q is required to suppress the out of band signal. However, if the signal in the adjacent channel is

much larger than the desired signal, the BPF cannot eliminate the signal completely due to the restriction of the circuit size. The remaining adjacent channel signal will interfere the desired signal by folding down to the desired signal channel. As the result, the desired signal cannot be demodulated.

Jitter and phase noise of the sample clock signal can seriously degrade undersampling performance. This effect can reduce by using a high-quality crystal oscillator with simple, direct connections to the ADC. Some ADCs are specifically characterized for undersampling applications, while others are designed only for baseband sampling.

The system in Chapter 3 is implying undersampling.

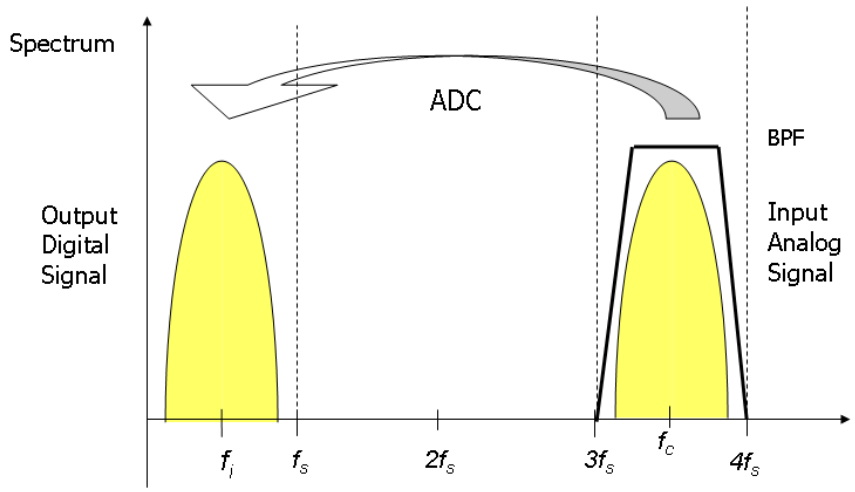

Figure 1.16: Frequency conversion with undersampling.

1.4.4 Sample Rate Conversion

In SDR terminals, the problem of SRC emerges if the sample rate of the ADC is different from the symbol, chip, or bit rate of the processed signal. Since different communication standards are based on different master clock rates, it is mainly necessary to provide different clock rates. However, a tunable sample rate of ADC is a not a best choice because high complexity analog components must be avoided.

Since a signal processor should work at the minimum possible rate, SRC has to be implanted to a SDR receiver in order to process various kinds of radio standards [3]. The problem is because the baseband processing is usually carried out at the target rate and not at an arbitrary sample rate.

The most common structure for SRC is a combination of an L-factor upsampler, an anti-aliasing filter, and an M-factor downsampler, as illustrated in Fig. 1.17. This of SRC is called rational factor SRC.The SRC by L/M-ratio is done by upsampling the input data with L and then downsampling it by M [22, 23]. The upsampling by L factor is generated by inserting $L-1$ zeros between two consecutive samples of the input signal at the upsampler. The downsampling of the filtered upsampled signal is done by the downsampler by deleting all but every Mth sample of the signal. Although this technique is very useful for investigations, it is not applicable in practice in some systems due to the possibly very high intermediate sample rate and also required large effort for the anti-aliasing filter.

Implementation of fractional-SRC by using a cascaded-integrator comb (CIC) filter can reduce the effort as the impulse response of the reconstruction filter can be realized by the comb filter [24]. However, this technique still requires the high intermediate sample rate. Time-varying polyphase structure based fractional-SRC has been proposed to avoid the high intermediate frequency. The most commonly used implementation in this kind of structure is the Farrow structure which is a combination of polynomial filtering and block processing [25, 26]. Polyphase realization for the CIC filter is also proposed in order to avoid the high intermediate sample rate [27]. However, the polyphase structure based fractional-SRC requires multiple of fractional delay filters and a lot of multiplexers which increase the complexity and power consumption.

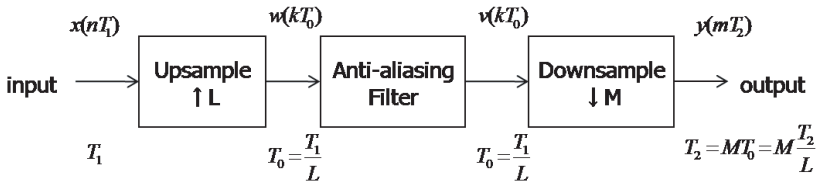

Figure 1.17: Rational Factor SRC

Direct Insertion/Cancellation SRC

A direct insertion/cancellation SRC has been proposed to realize high speed SRC with low complexity [28, 29]. This technique, which is also called non-interpolative resampling technique, does not interpolate the signal to the higher sample rate and avoid the high intermediate sample rate. This technique is suitable for application in the RF sampling receiver which samples data with a high OSR. In this technique, new samples are inserted to the data stream to increase the rate to a desired sample rate, or an amount of samples is deleted from a data stream to decrease the sample rate. In the direct insertion scheme, α samples are inserted in every block of N samples to increase the rate by $(N+\alpha)/N$. The inserted samples can simply be zeros or a repeat of last value. In the direct cancellation scheme, α samples are deleted in every block of N samples to reduce the rate by $(N-\alpha)/N$. This scheme can be realized with smaller chip size and lower power consumption as compared to the other techniques. However this scheme suffers from large distortion as compared to the other technique.

Figure 1.18 shows the conventional periodic direct insertion/cancellation scheme. The inserter/deleter block in the figure performs direct insertion/cancellation process. The insertion or cancellation step is followed by filtering process by the anti-aliasing filter. The images that have been generated after insertion/cancellation process are removed by the anti-aliasing filter, before the signal is decimated to the desired sample rate.

In the direct insertion method, where α sample is inserted by repeating the R-th

sample in every $N+\alpha$ samples period to increase the data rate by $(N+\alpha)/N$, the output signal is given by

$$y(kT_2) = x\left(\left(\left\lfloor \frac{kN+R}{N+\alpha} \right\rfloor\right) T_1\right), \tag{1.6}$$

where $x(k)$ in the k-th sample of the input sequence, T_1 is the input sampling period, and T_2 is the output sampling period. In the direct cancellation method, every R-th sample in every N samples period of the input signal sequence is deleted to reduce the data rate by $(N-\alpha)/N$. The output signal is given by

$$y(kT_2) = x\left(\left(\left\lceil \frac{kN-R+1}{N-\alpha} \right\rceil\right) T_1\right). \tag{1.7}$$

The output of the inserter/deleter also produces images every $1/NT_1$ for a conversion rate of $(N+1)/N$ and $(N-1)/N$, as illustrated in Fig. 1.19. The images are attenuated by using the anti-aliasing filter to avoid further distortion and aliasing.

The direct insertion/cancellation SRC scheme is discussed in Chapter 4.

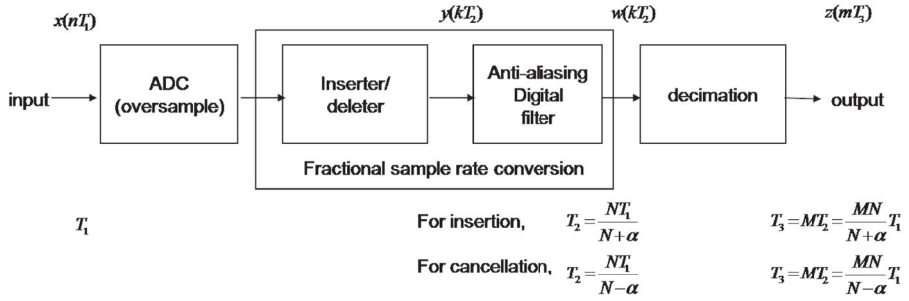

Figure 1.18: Direct insertion/cancellation based fractional-SRC.

1.5 Adjacent Channel Interference

This thesis deals with ACI problems in SDR receiver system. ACI is interference caused by extraneous power from a signal in an adjacent channel. ACI may be caused by inadequate filtering, improper tuning, or poor frequency control, in either the

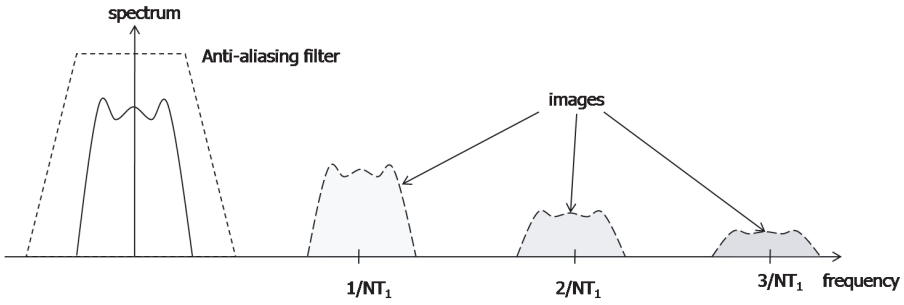

Figure 1.19: Generated images after direct insertion/cancellation.

reference channel or the interfering channel, or both. In the case of the SDR receiver, flexible receiver architecture with wideband signal receiving capability is required. However, if the receiving bandwidth is wider, the received signal components may cause interference to each other. Higher requirements of filters, ADCs, and other analog components are needed to realize a wideband receiver. Moreover, some of the adjacent channel components may overlap directly to the desired channel. This research is focusing on signal processing methods to combat ACI problems and lower the requirements in The SDR receiver.

The performance of a wireless receiver is often determined by the signal-to-interference ratio (SIR), which is defined as the ratio of the data signal to the interference signal. SIR is usually more critical to WLAN performance than the SNR. Interference resulting from signals which are adjacent in frequency to the desired signal is called ACI.

If the signal power in the adjacent channel is much larger than the desired signal, ADCs with very high dynamic range are required as shown in Fig. 1.20. This is not desirable as the large dynamic range leads to higher cost and power consumption of the ADCs.

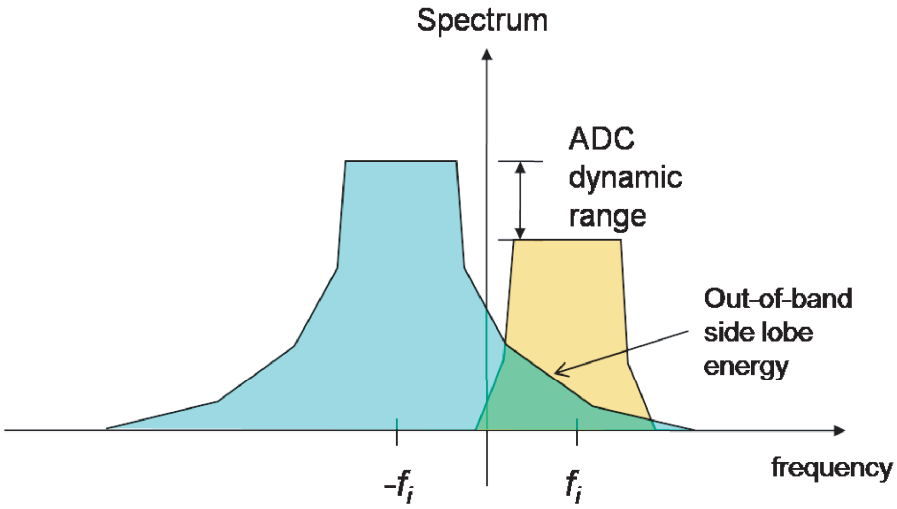

Figure 1.20: Interference due to the signal in the adjacent channel.

1.5.1 Out-of-band Side-lobe Energy

The channels that are beside one another in the frequency domain may have some spectral overlap, causing impairment and interference. Although filtering is usually done to minimize interference from the adjacent channels, this interference also generates side lobe energy that falls into the pass band of desired signal. If the adjacent channel is much larger than the desired signal, side band energy from the adjacent channel can dominate the channel's noise floor, as illustrated in Fig. 1.20.

Figure 1.21 shows the usage of 4 channels in 100MHz band with 20 MHz interval that used in WLAN IEEE802.11a. The spectrum mask standard and spectrum of amplifier output of WLAN IEEE802.11a/g is shown in Fig. 1.22 [30]. The influence of ACI is determined by adjacent channel rejection level. The adjacent channel rejection level means, the limit of interference level compare to the desired signal level that allowed in the existence of interference from adjacent channel. For example, if the transfer rate is 24Mbps, the adjacent channel rejection is 8dB. Therefore, if the desired signal is -71dBm, it is possible to receive the desired signal even there is interference of -63dBm from adjacent channel.

The interference due to the out-of-band side-lobe energy in a WLAN system is discussed in Chapter 2 and Chapter 3. An interference cancellation method to overcome the problem is also proposed in the chapters.

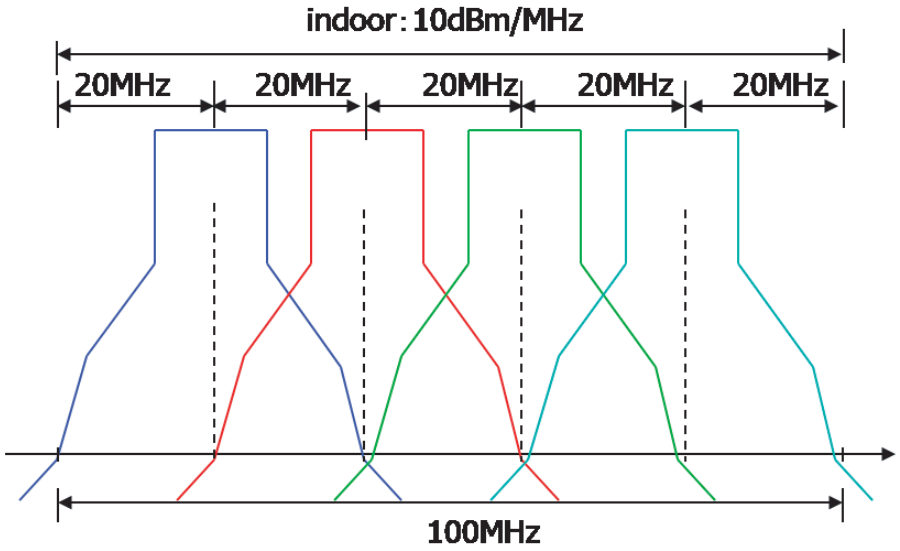

Figure 1.21: IEEE 802.11a channel spectrum.

1.5.2 ACI due to Undersampling

ACI problems also may occur when a high frequency signal is sampled at a lower sample rate as in undersampling technique. In the undersampling technique, any out of band signals or noise must be kept to a minimum because they will fold down into the output spectrum, exactly as illustrated in Fig. 1.23. In the figure, the adjacent channels are not sufficiently rejected, resulting interference from the downfolded adjacent channels. If the adjacent channel signal is significantly large, a high performance BPF with a very large Q is required to minimize the adjacent channel. Otherwise, the remaining components will aliased and translated to the desired band.

The effect of undersampling to a multi-channel reception system is discussed in

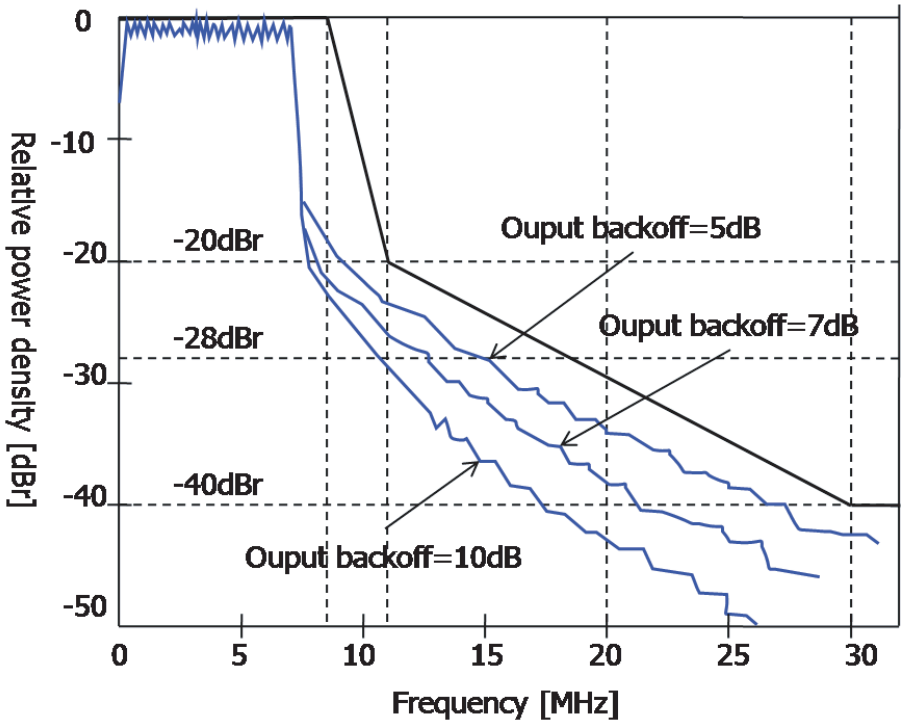

Figure 1.22: Spectrum mask standard and spectrum of amplifier output.

Chapter 3.

1.5.3 Aliasing due to Sample Rate Conversion

Image signal will be generated when the sample rate is upsampled, and the aliasing will happen when the signal is downsampled. If the adjacent channel is not completely eliminated before the SRC process, aliasing from the adjacent channel may be overlapped on the desired signal.

As stated in 1.4.4, the direct insertion/cancellation SRC suffers from high distortion and aliasing problems. Moreover, the images that generated by the adjacent channels may generated directly in the desired signal band, as illustrated in Fig. 1.24. The interference cannot be rejected by anti-aliasing filter.

The effect of the aliasing due to the SRC scheme is discussed and a method to mitigate the effect is proposed in Chapter 4.

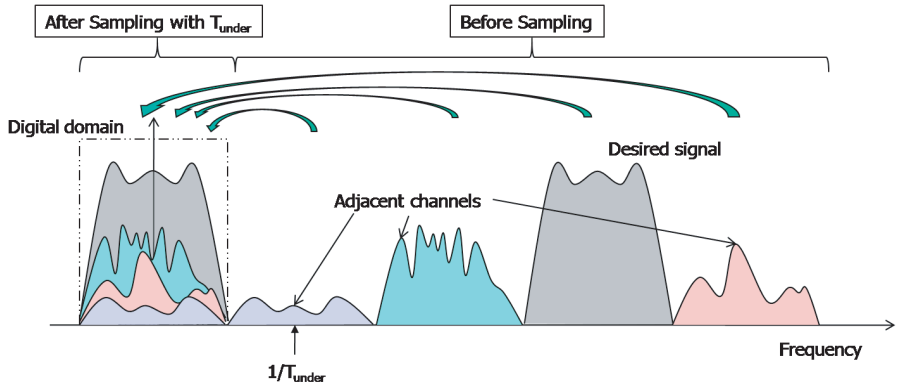

Figure 1.23: ACI due to the undersampling

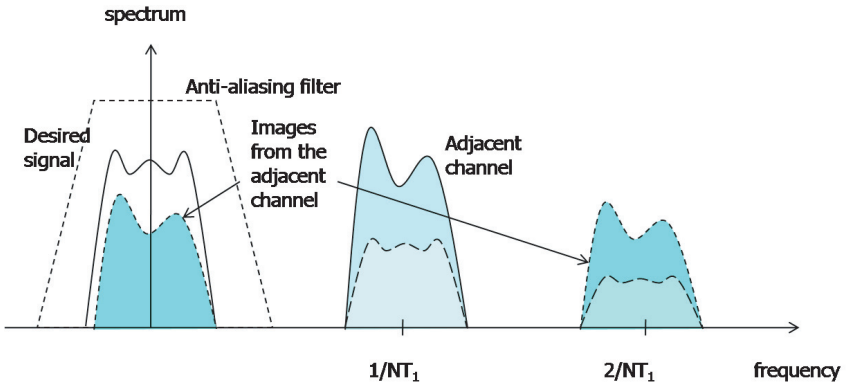

Figure 1.24: ACI due to the direct insertion/cancellation SRC.

1.6 Motivation of the Research

1.6.1 Realization of SDR receiver

This dissertation discusses the signal processing in a SDR receiver system. The ideal concept for the SDR terminal is to attach an ADC directly to the antenna, as illustrated in Fig. 1.25 [1]. However, the ideal concept is not completely realizable due to the actual technology limits. The need of ultra high speed ADC cannot be realized by the current technology. The actual practical solution is to let the software processing stage be preceded by a front-end that preconditions the input signals to give them characteristics that enable the subsequent stage to elaborate them. The signal mixing based downconversion architecture such as superheterodyne receiver,

DCR, and low-IF receiver has been proposed for SDR.

A superheterodyne RF front-end architecture is adopted to lower the frequency of the received signals to IF values. A typical structure of the superheterodyne receiver architecture is shown if Fig. 1.26. After the first downconversion mixer, a passive off-chip channel select filter attenuates the out-of-channel signals to a sufficiently low level. A VGA, which follows the IF channel-select filter, decreases the dynamic range requirements of the ADC. Then, the desired signal is downconverted to the baseband before it is converted to a digital signal by an ADC. Although off-chip filters offer sufficient image rejection and selectivity, the input and output of each off-chip filter requires impedance matching that increases the power consumption in the RF front-end. The superheterodyne implementation of a multimode receiver requires multiple filters that not only increase the production cost but also the physical dimension of the handset. Thus, superheterodyne receiver is not a practical topology for multimode receiver designs.

DCR architecture, which has introduced the zero IF approach, supports efficient wireless terminal designs with a high level of integration [7, 10]. The structure of the DCR is shown in Fig. 1.27. In the DCR, the desired signal is downconverted directly to baseband signal with only single conversion stage. Thus, the DCR had lower complexity and power consumption. Low-IF receiver architecture has been proposed to avoid DC offset problem in a DCR. In the low-IF receiver, received signal is downconverted to a IF instead of downconvert it directly to a baseband signal. The IF is set to be relatively lower than that in the conventional IF receivers. There are several merits by using low-IF receiver architecture. Low-IF receivers are not using SAW filter so that this architecture would have low cost and low power consumption as compared to super-heterodyne architecture. The low-IF receiver is much easier to make in one chip and the structure of the low-IF receiver can be much simpler than the super-heterodyne receiver.

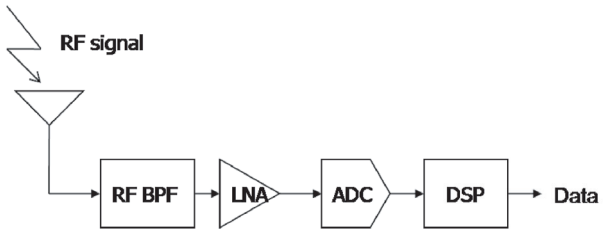

Figure 1.25: Ideal SDR concept

The RF-sampling receiver scheme has been proposed recently to replace the conventional mixer-based downconversion scheme. The direct RF sampling technique is based on current sampling, which greatly simplifies the mixer circuit design [28]. In the RF-sampling architecture, the received signal is processed directly at the analog domain and sampled at the RF [12, 16]. Channel selection and demodulation are carried out in the digital domain. This architecture achieves the reduction of off-chip components and enables the realization of a single-chip receiver. RF-sampling receiver, which supports single chip and multi-mode designs, is a promising architecture for the next generation wireless terminals to realize a flexible wireless terminals with smaller physical dimensions. The structure of the RF-sampling architecture is shown in Fig. 1.29. The received signal is sampled at the same frequency of the carrier signal at the downconversion sampler to perform downconversion. This is followed by the decimation and filtering processes. The discrete signal is sampled at a high sample rate of the ADC. In the digital domain, digital signal processing and SRC are performed. Direct insertion/cancellation SRC is proposed to process the high sample rate signal.

In this dissertation, we use 2 approaches to realize the flexible receiver for SDR;

1. Low-IF signal mixing downconversion receiver architecture
2. RF sampling receiver architecture

In order to realize a SDR receiver, flexible receiver architecture with wideband

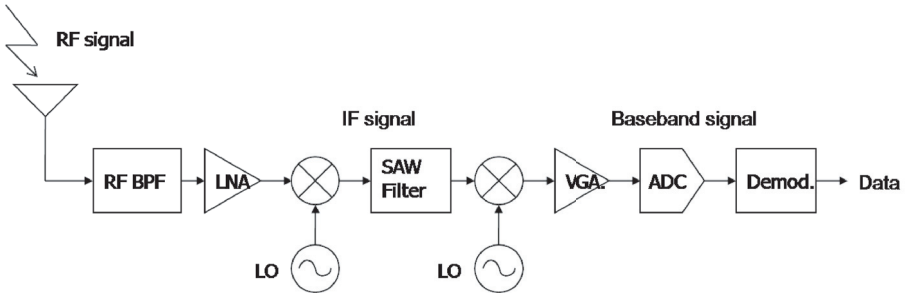

Figure 1.26: Superheterodyne receiver architecture.

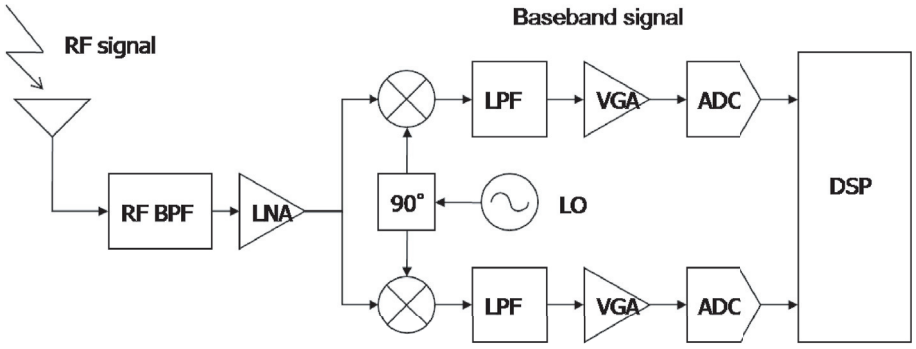

Figure 1.27: DCR architecture.

signal receiving capability is required. However, if the receiving bandwidth is wider, the received signal components may interfere each other. In this study, the signal processing methods to combat the ACI problems in the SDR receivers are investigated and discussed.

In the first receiver architecture approach, the flexible wideband receiver is discussed to be realized by utilizing the low-IF receiver with multi-channel reception capability. However, the multi-channel low-IF receiver suffers from a high interference from the adjacent channel. ADCs with a very high dynamic range are required to sample multiple of signals with a large power difference. Moreover, the out-of-band side lobe signal from the adjacent channel may be directly overlapped with the desired signal. The requirement of the high dynamic range ADC can be lowered by using complex BPF. Nevertheless, the problem of the analog BPFs is that it cannot eliminate the interference completely due to the restriction of the circuit size and

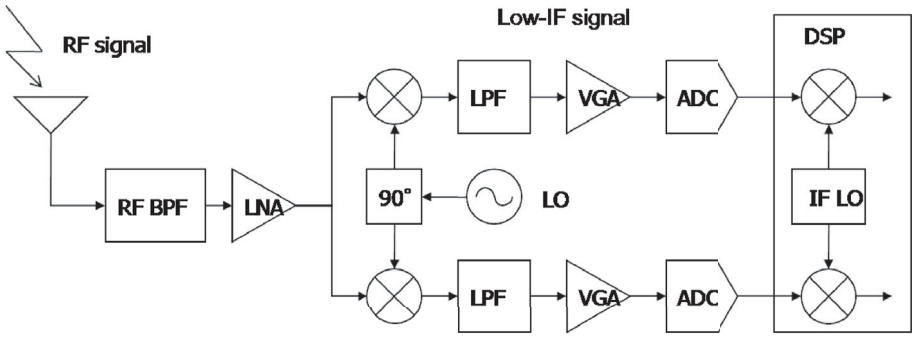

Figure 1.28: Low-IF receiver architecture.

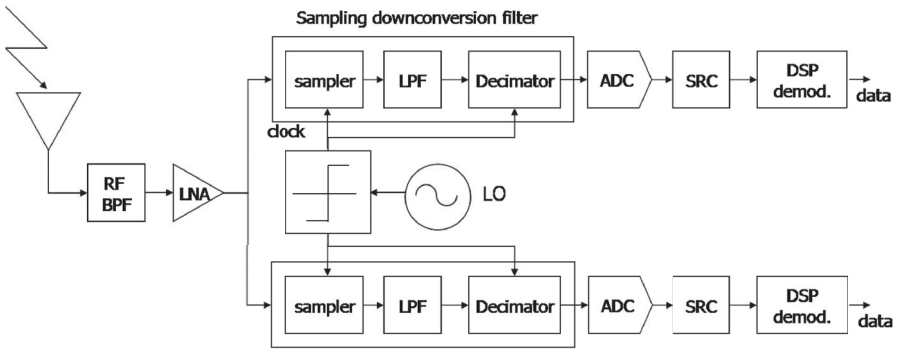

Figure 1.29: RF-sampling receiver architecture.

the mismatch of the analog components. In Chapter 2, the ACI cancellation scheme with analog filter bank has been proposed to mitigate the influence from the adjacent channel.

ACI problems also may occur when a high frequency signal is sampled at a lower sample rate as in undersampling technique. In Chapter 3, undersampling technique is applied in this system in order to lower the required sampling frequency and power consumption. In order to realize the undersampling, all the out of band signal including noise and adjacent channel has to minimize as possible to avoid the overlapping with those signals. A high performance BPF with a very large Q is required to minimize the out-of-band signals. In the chapter, the side effect of the undersampling technique to the multi-channel reception with low Q BPFs is investigated. An ACI

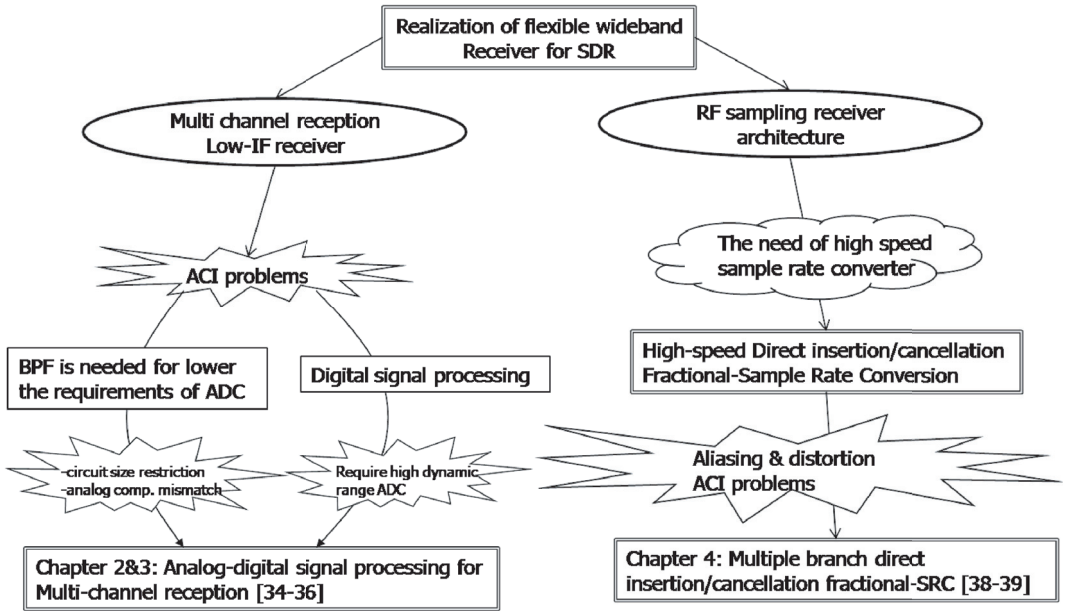

Figure 1.30: Motivation of the research.

cancellation scheme by using digital signal processing is proposed in the chapter to overcome the aliasing effect of the undersampling.

Images and aliasing which are appeared in an SRC process also bring the ACI problems as the aliasing from the adjacent channel may be overlapped on the desired signal. In the second receiver architecture approach, the ACI effects are small due to the usage of the high speed sample rate and high resolution of the ADC. However, the usage of the high speed fractional SRC introduces high aliasing to the converted signal. The image aliasing from the adjacent channel may directly be overlapped with the desired signal. Therefore, a new fractional SRC technique is investigated in Chapter 4, in order to overcome the aliasing and ACI problems and realize a high performance fractional SRC.

1.6.2 Adjacent Channel Interference Cancellation Scheme for Low-IF Receiver in Multi-Channel Reception

Chapter 2 discusses about a realization of high-speed handover for WLAN by using multi-channel reception concept. Chapter 2 proposes the method to solve the ACI

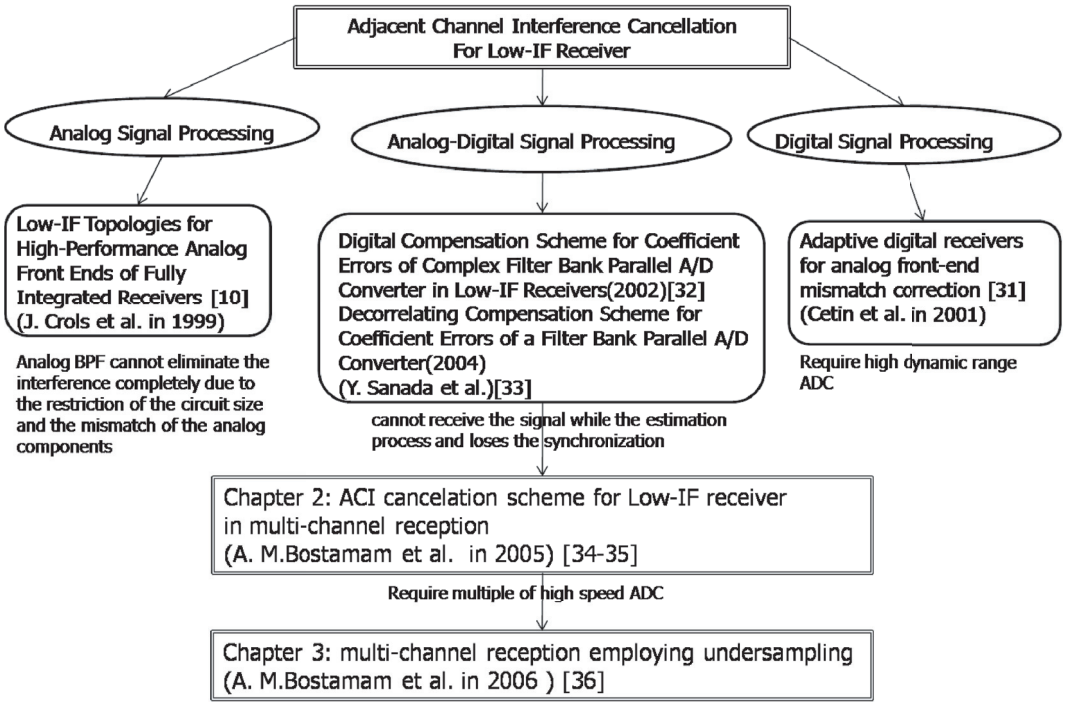

Figure 1.31: Relationship of the research about ACI cancellation in Low-IF receiver architectures.

problem due to the high dynamic range and out-of-band leakage from the adjacent channel. In the cases that the adjacent channel signal is much larger than the desired signal, high resolution ADCs have to be employed to accommodate such a signal with large dynamic range. The increase of the resolution of the ADC causes higher power consumption and higher implementation cost. Moreover the ACI component may directly overlap with the desired signal if the interference is much larger than desired signal.

The relationship of the research about ACI cancellation in Low-IF Receiver Architectures is shown in Fig. 1.31. In the previous studies, the ACI rejection or cancellation has been proposed by using analog circuits or digital signal processing. In [10], complex BPF, that can discriminate between the desired signal and the mirror signal, is proposed to be applied to the low-IF receiver. However, due to the restriction of the circuit size and the mismatch of the analog components, it is hard to realize high

Q analog filter. Several ACI cancellation technique using adaptive signal processing has been proposed [31]. However, the digital approach alone requires a very high dynamic range requirement of ADCs to be realized.

In order to reduce the required resolution of the ADCs and reduce the interference, an analog-digital signal processing technique has been investigated [32, 33]. This technique uses a BPF for each WLAN channel. The BPFs ease the dynamic range of the ADCs and makes the modulation of multi-channel possible. Nevertheless, the problem of the analog BPFs is that it cannot eliminate the interference completely due to the restriction of the circuit size and the mismatch of the analog components. Thus, combination of the analog and digital signal processing is indispensable. The problem of this scheme is that it requires estimating the characteristics of the analog filters. This system requires the signal generator in the receiver to generate known waveform for the estimation. While estimating the characteristics, the receiver can not receive the signal and loses the synchronization.

In this chapter, a new ACI cancellation scheme with the analog filter bank has been proposed [34, 35]. The proposed scheme automatically estimates the characteristics of the interference signal and cancels it from the received signal through Wiener filter. The proposed scheme can estimate the characteristics of the interference signal while it maintains the synchronization to the received signal even though the training sequence is required periodically. The results obtained from experiment show that the proposed technique enables multi-channel reception and work with the low resolution ADCs.

1.6.3 Undersampling for Adjacent Channel Interference Cancellation Scheme

The objective of Chapter 3 is to lower the requirements of ADCs in the scheme that is proposed in Chapter 2 [35]. The proposed scheme in Chapter 2 requires

multiple of high speed ADCs to prepare the filter bank. Also the low-IF receiver requires higher sampling frequency than the conventional architecture such as super-heterodyne. Thus, the ADCs in the low-IF receiver require higher power consumption than the conventional scheme.

Undersampling technique is employed in this scheme in order to lower the required sampling frequency and power consumption of the ADC [36]. In the conventional sampling technique, Nyquist rate is required to sample the received signal. Desired signal can be sampled with sampling frequency below Nyquist rate by using the undersampling technique. The undersampling translates a high frequency bandpass signal to a near zero lowpass frequency. The sampling frequency requirement is based on the signal bandwidth rather than its highest frequency. Sampling at reduced rates eases many of the ADC requirements, and decreases power consumption, thus increasing battery lifetime, and the overall receiver size. The need for very high performance programmable devices is also reduced.

Any out of band signal or noise must be kept to minimum because they will fold down to the desired signal band. A BPF of very high Q is required to suppress the out of band signal. If the signal in the adjacent channel is much larger than the desired signal, the BPF cannot eliminate the signal completely due to the restriction of the circuit size. The remaining adjacent channel signal will interfere the desired signal by folding down to the desired signal channel. As the result, the desired signal cannot be demodulated. In Chapter 3, the side effect of the undersampling technique to the multi-channel reception is investigated through the experiment. The influence of aliasing effect in the undersampling is compensated in digital domain by using the adaptive digital signal processing.

1.6.4 Fractional Sample Rate Conversion for SDR

Since different communication standards are based on different master clock rates, it is mainly necessary to provide different clock rates. Since a signal processor should work at the minimum possible rate, SRC has to be implanted to a SDR/CR receiver in order to process various kinds of radio standards [3].

The relationship of the research about Fractional SRC is shown in Fig. 1.32. The most common structure for fractional SRC is a combination of an L-factor upsampler, an anti-aliasing filter, and an M-factor downsampler. The SRC by L/M-ratio is done by upsampling the input data with L and then downsampling it by M [23, 27]. However, this technique is not applicable in practice in some systems due to the possibly very high intermediate sample rate and also required large effort for the anti-aliasing filter. Implementation of fractional-SRC by using a CIC filter can reduce the effort as the impulse response of the reconstruction filter can be realized by the comb filter [23, 24]. However, this technique still requires the high intermediate sample rate. Time-varying polyphase structure based fractional-SRC has been proposed to avoid the high intermediate frequency. The most commonly used implementation in this kind of structure is the Farrow structure which is a combination of polynomial filtering and block processing [23, 25–27]. Polyphase realization for the CIC filter is also proposed in order to avoid the high intermediate sample rate [37]. However, the polyphase structure based fractional-SRC requires multiple of fractional delay filters and a lot of multiplexers which increase the complexity and power consumption.

Chapter 4 proposes a new fractional SRC scheme based on a direct insertion/cancellation scheme. This technique is also called non-interpolative resampling technique [28, 29]. This scheme is suitable for signals that are sampled at a high sample rate and converted to a lower sample rate. The objective of the scheme is to realize a high-speed and high-performance SRC scheme with low-complexity and lower power consump-

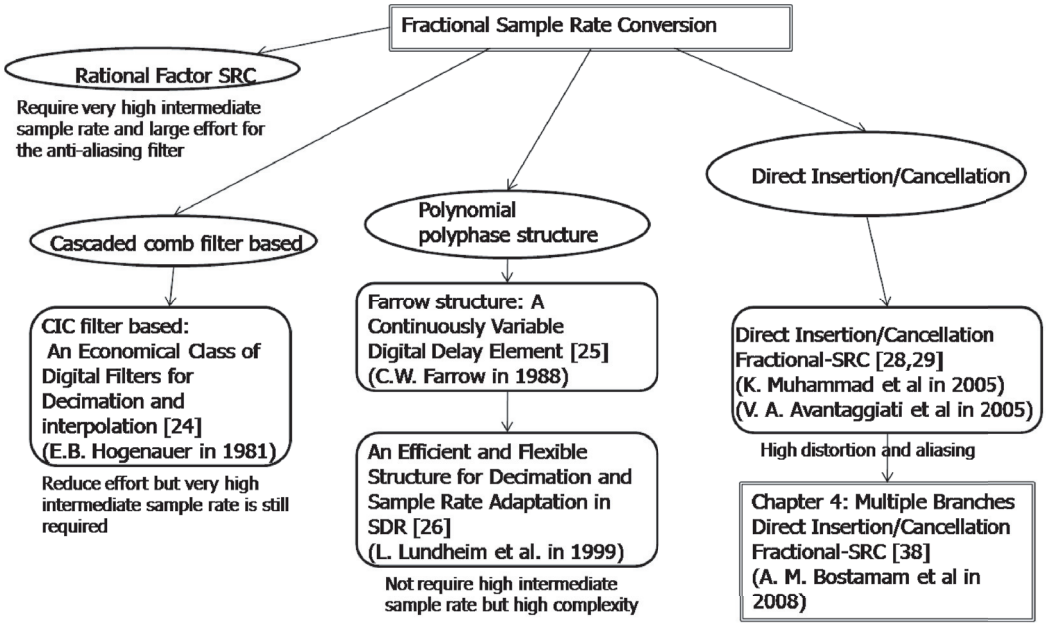

Figure 1.32: Relationship of the research on fractional SRC.

tion. High-speed SRC scheme for high sample rate data can be realize by a direct insertion/cancellation scheme. This technique is suitable for application in the RF sampling receiver which samples data with a high OSR.

However, the direct insertion/cancellation technique suffers from large aliasing and distortion as compared to the other SRC techniques [29]. The aliasing from an adjacent channel interferes the desired signal and degrades the performance. Therefore, a modified direct insertion/cancellation scheme is proposed in order to realize high performance resampling. The distortion noise or aliasing can be reduced by applying multiple sets of inserters/deleters [38, 39]. This technique reduces the required complexity of an anti-aliasing filter structure, and improves the performance of a direct insertion/cancellation based SRC system.

Chapter 2

Adjacent Channel Interference Cancellation Scheme for Low-IF Receiver in Multi-Channel Reception

In this chapter a new adjacent channel interference (ACI) cancellation scheme for multi-channel signal reception with low-IF receivers is investigated through the experiment. In the low-IF receivers, the signal in the mirror frequency causes interference to the desired signal. In the proposed analog-digital signal processing scheme, channel selection is made by analog complex band pass filter and the signal is reconstruct by Wiener filter to eliminate the interference effect in order to improve the performance. This Chapter also describes an application of multi-channel reception for quick roaming in WLANs system.

2.1 Introduction

Access points for wireless LANs have been installed in many places such as airports or hotels. Though the roaming capability has been specified in the IEEE802.11 standard, it is not able to handle a quick roaming for Voice over Internet Protocol (VoIP) applications. Therefore, multi-channel reception is required for VoIP over WLAN.

One of the receiver architecture applicable for such applications is the low-IF receiver [2, 10]. In the low-IF receiver, the IF is set to be relatively lower than that in conventional IF receivers. The low-IF receiver are not using SAW filter so that this architecture would have low cost and low power consumption compared to conventional super-heterodyne architecture. The IF signal is sampled and converted to the digital signal with analog-digital converters (ADCs). The final process of down conversion is carried out in the digital domain. This architecture is applicable for multi-channel reception as the choice of the channel can be done with digital signal processing. However, in some cases the next access point may be far away from the current one and the dynamic range between the signals from the current access point and those from the next one may be quite large. This means that high resolution ADCs have to be employed to accommodate such a signal with large dynamic range. The increase of the resolution of the ADC causes higher power consumption and higher implementation cost. Moreover, the ACI component may directly overlap with the desired signal if the interference is much larger than desired signal.

In order to reduce the required resolution of the ADCs and reduce the interference, an analog-digital signal processing technique has been investigated [32,33]. This technique uses a band pass filter (BPF) for each WLAN channel. The BPFs ease the dynamic range of the ADCs and makes the modulation of multi-channel possible. Nevertheless, the problem of the analog BPFs is that it cannot eliminate the interference completely due to the restriction of the circuit size and the mismatch of the analog components. Thus, combination of the analog and digital signal processing is indispensable. The problem of this scheme is that it requires estimating the characteristics of the analog filters. This system requires the signal generator in the receiver to generate known waveform for the estimation. While estimating the characteristics, the receiver can not receive the signal and loses the synchronization.

In this chapter, a new ACI cancellation scheme with the analog filter bank has

been proposed. The proposed scheme automatically estimates the characteristics of the interference signal and cancels it from received signal through Wiener filter. The proposed scheme can estimate the characteristics of the interference signal while it maintains the synchronization to the received signal through training sequence is required periodically. The results obtained from experiment show that the proposed technique enables multi-channel reception and work with the low resolution ADCs.

2.2 Multi-Channel Reception

2.2.1 Roaming Protocol

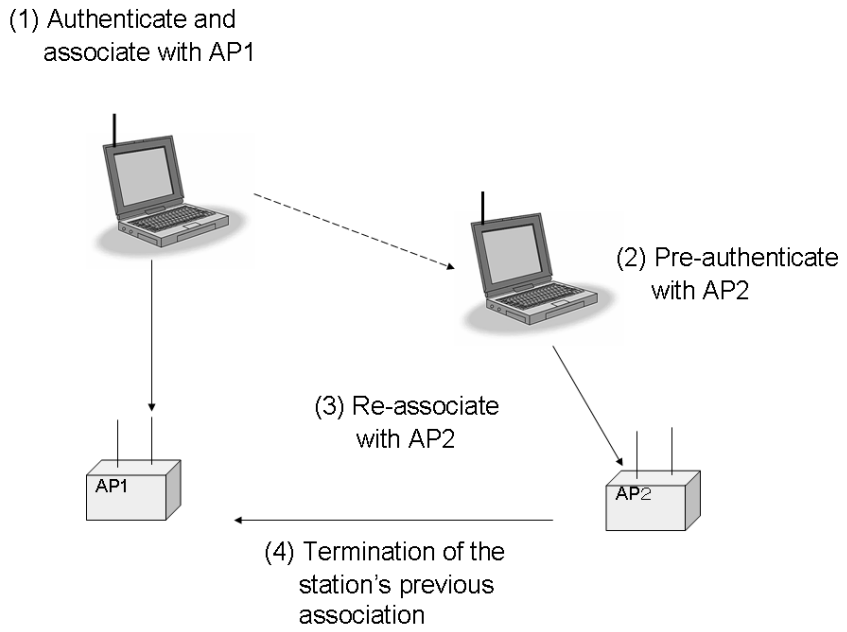

Figure 2.1: Roaming example with IEEE802.11 MAC Protocol.

The mobility of WLAN terminals among multiple base stations is specified in Extended Service Set (ESS) of IEEE802.11 MAC protocol [40]. An example of roaming capability with IEEE802.11 MAC is shown in Fig. 2.1. A handover occurs when a terminal moves beyond the radio coverage of an access point (AP), and enters cover-

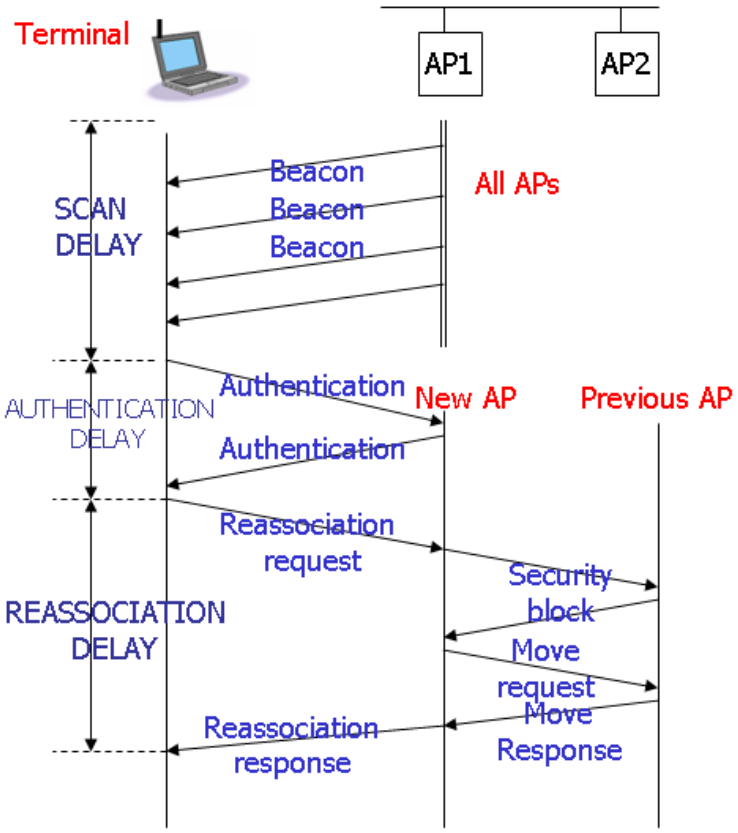

Figure 2.2: Passive scan.

age of another AP. As the terminal finds AP1, it will authenticate and associate with AP1. As the terminal moves, it may pre-authenticate with AP2. When the terminal determines that its association with AP1 is no longer desirable, it may reassociate with AP2. The reassociation causes AP2 to notify AP1 of the new location of the station, terminating the terminal's previous association with AP1. In general, the terminal can be authenticated with many different stations simultaneously. However, it may be associated with only one base station at a time. Therefore, it is not suitable for quick roaming in some applications such as VoIP over WLAN requires.

During the handover process, the terminal is not able to send or receive data traffic. In the process, management frames are exchanged between the terminal and the AP. Also the APs involved may exchange certain context information specific to

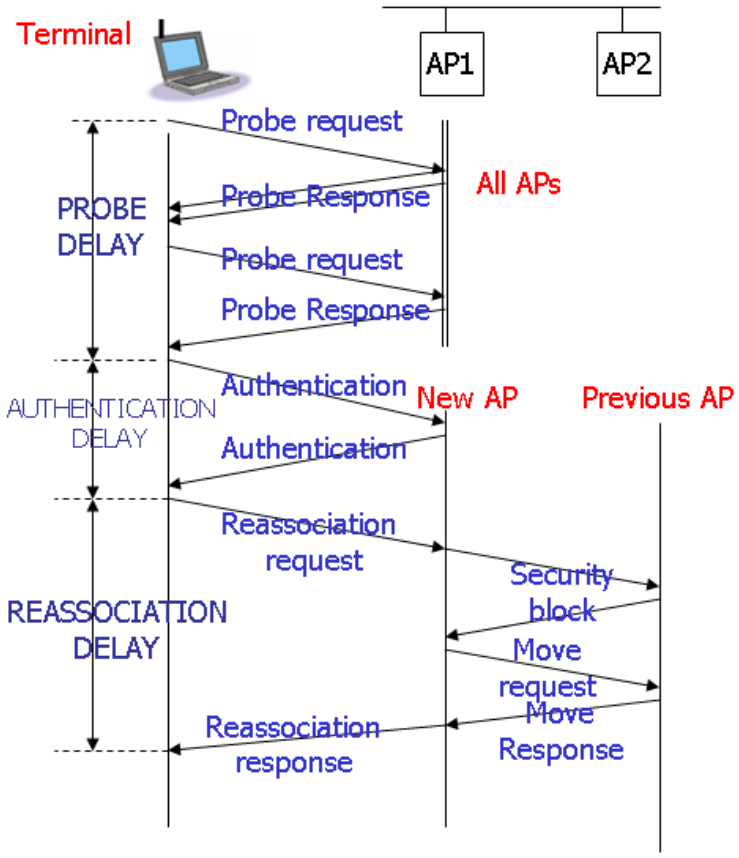

Figure 2.3: Active scan.

the station. The complete handover process can be divided into two different logical steps which lead to latency; Discovery and reauthentication.

In Discovery step, when the signal-to-noise ratio (SNR) of the signal from the current AP drops below a threshold value, it triggers the terminal to start searching for another AP. The searching for a new AP is accomplished by scanning procedure in MAC layer function. There are two scanning method defined in the standard: active scanning and passive scanning. In passive scanning (Fig. 2.2), a terminal listens for beacons from APs. These beacons are issued by all APs at a rate of 10 beacons per second. In active scanning (Fig. 2.3), the terminal sends probe request to each channel and waits for probe responses from APs on each channel. The scanning delay accounts most of the overall handover delay.

The re-authentication phase involves the transfer of credentials and other state information from the old AP. These can be achieved with inter access point protocol (IAPP). The re-authentication process typically involves an authentication and re-association to a new AP. In authentication process, a delay incurred during the exchange of the authentication frame between the terminal and the new AP. In reassociation process, a delay incurred during the exchange of re-association frames between the terminal and the new AP and also between the new AP and the previous AP.

2.2.2 Multi-Channel Reception with Low-IF Architecture

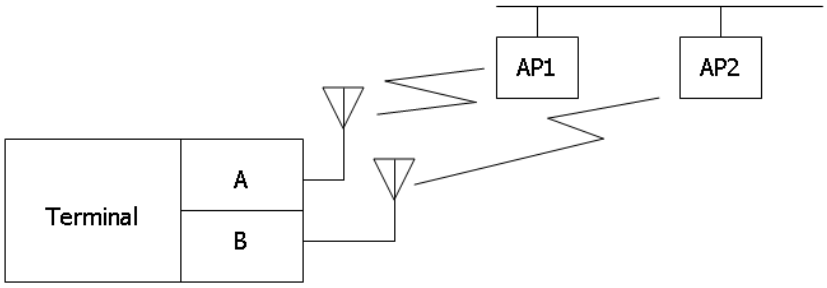

Figure 2.4: Seamless handover using two WLAN devices on a mobile node.

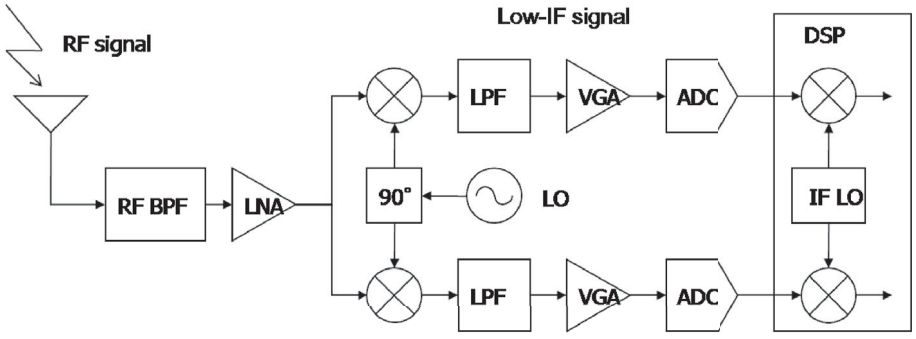

Figure 2.5: Low-IF receiver architecture.

In order to solve this problem, multi-channel reception capability is required. For example, in IEEE802.11g WLAN systems, 4 channels in 2.4 GHz band are utilized

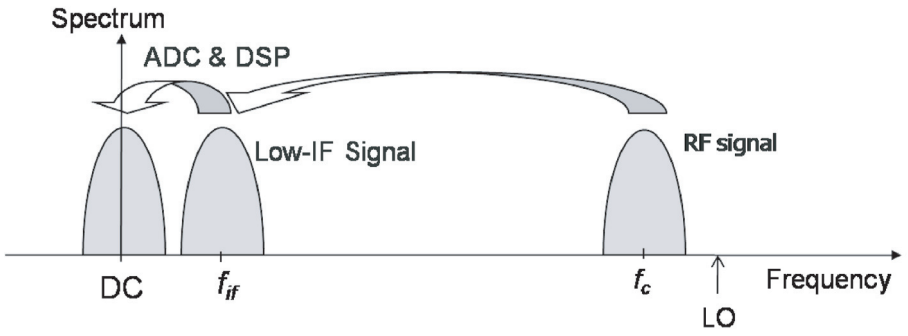

Figure 2.6: Downconversion of the received signal in low-IF receiver architecture.

to cover large area for the services. Thus, if these 4 channels can be demodulated by one receiver, the quick roaming may be possible and the mobile VoIP service over WLAN can be provided.

There are several receiver architectures applicable for multiple channel reception. The simplest architecture is to combine multiple independent receivers in one package. In [41], a method of seamless handover using two WLAN devices on a mobile node has been presented, as illustrated in Fig. 2.4. In this scheme, while one of the WLAN devices connect to an access point, the another WLAN device would perform scan process. However, this architecture has large redundancy in their circuits. Another candidate is by using the low-IF receiver. The structure of the low-IF receiver is shown in Fig. 2.5. The received signal is first down converted to the IF signal by mixing the it with local oscillator (LO) as shown in Fig. 2.6. Then the IF signal is converted to digital signal with ADCs and finally converted to the baseband signal with DSP. As the down conversion is carried out with DSP, it is possible to select one of 4 channels easily.

However, in the low-IF receivers, ADCs with very high dynamic range may required if the signal power in adjacent channel is much larger than the desired signal as shown in Fig. 2.7. In addition the desired signal may suffer from the interference from signals which are adjacent in frequency to the desired signal. This is called

adjacent channel interference (ACI). This interference occurs because the adjacent channel generates side lobe energy that falls into the pass band of the desired signal that make desired signal cannot be demodulated.

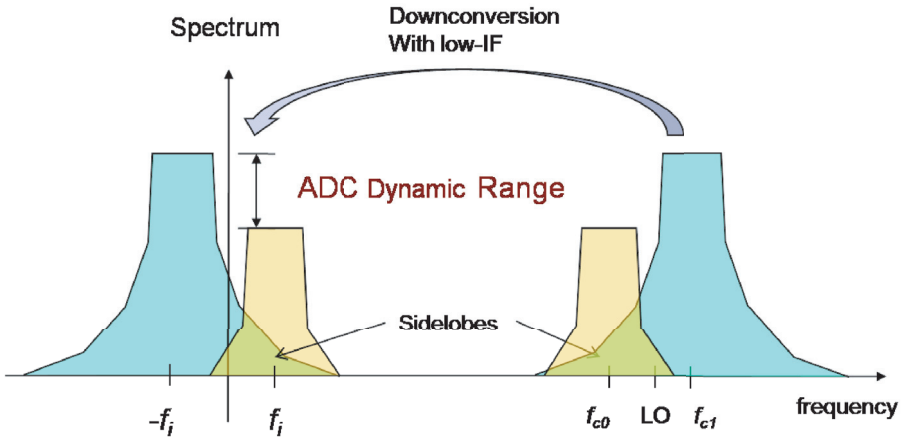

Figure 2.7: Downconversion of multi-channel and interference due to the signal in the adjacent channel.

2.3 System Model

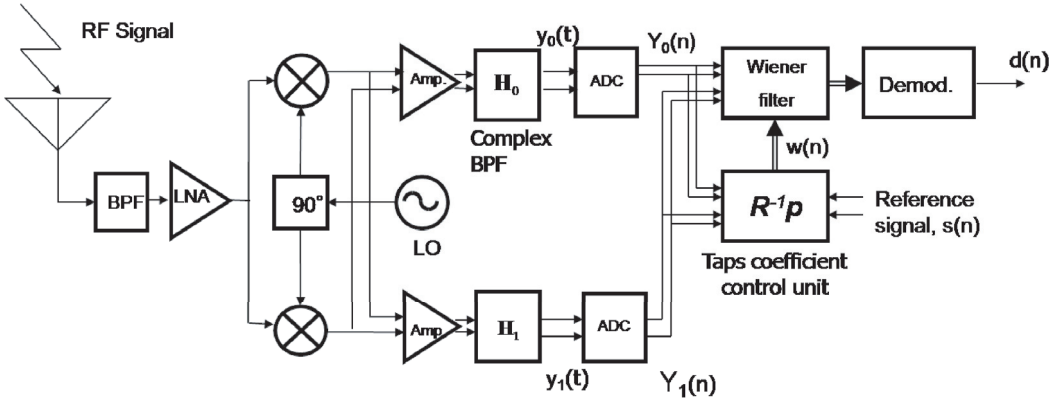

Figure 2.8: Model of the receiver with the proposed scheme.

In order to reduce the dynamic range of the ADCs and reduce the ACI, the analog-digital signal processing is utilized. The model of the receiver with the proposed

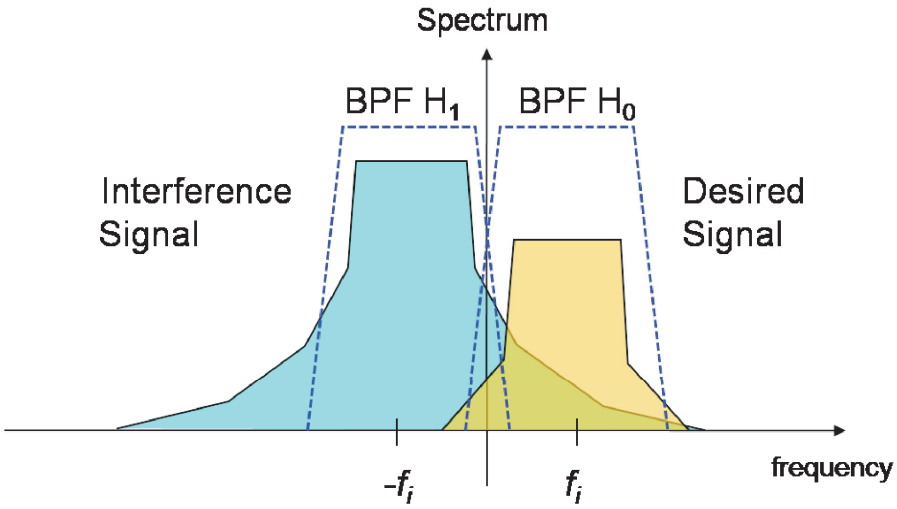

Figure 2.9: Received signal model.

scheme is shown in Fig. 2.8. In [32, 33] it has been shown that the analog filter bank can reduce the dynamic range of the ADCs. Complex analog BPFs are used in the filter bank. Complex filter is a filter that has complex-valued (I & Q) filter coefficients. Complex filters have different frequency responses in positive and negative frequency range, thus, the frequency characteristics are not symmetry as in real filters. With the complex filter it is possible to discriminate between the negative and positive frequencies and therefore, the mirror frequency will be filtered out. However, due to the restriction of the circuit size and the mismatch of the analog components, it is hard to realize high Q analog filter. Moreover the ACI may directly overlap with the desired signal if the interference is much larger than the desired signal.

Here, in addition to the analog filter bank, adaptive digital signal processing is utilized to reduce the ACI. The received signal is first goes through the RF BPF and LNA. The output of the LNA is then multiplied with the local signal and converted to the IF. With the analog filters, H_0 and H_1, the signals on the different channels are separated. However, if the power of the signal on the adjacent channel is large, it causes the interference to the desired signal. In order to reduce the ACI, the

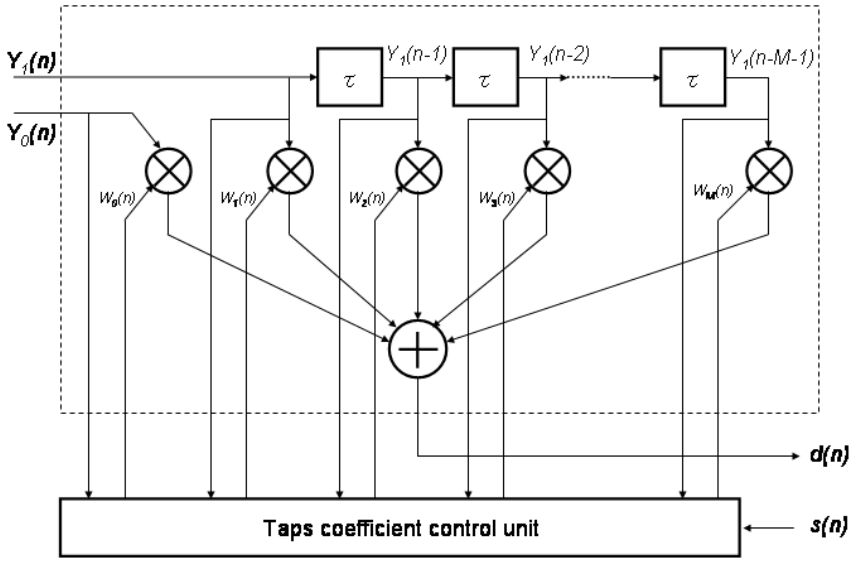

Figure 2.10: Wiener filter model.

adaptive digital signal processing, Wiener filter, is employed. However, the proposed scheme is only required when the roaming channel is an adjacent channel. When the channel is not adjacent, the receiver will demodulate the channel without the canceller process. Since the low-IF receiver requires higher sampling-frequency than conventional architecture such as super-heterodyne, undersampling technique can be applied in this system in order to lower the required sampling frequency.

Suppose that the desired signal and the interference signal are received at the same time as shown in Fig. 2.9. The downconverted received signal is expressed as

$$r(t) = d(t)\exp(j2\omega_i t) + I(t)\exp(-j\omega_i t) + n(t), \tag{2.1}$$

where $r(t)$ is the sample of the received signal at the time t, $d(t)$ is the desired signal, $I(t)$ is the signal on the adjacent channel, $\omega_i (= 2\pi f_i)$ is the intermediate frequency of the desired signal, $-\omega_i$ is the frequency of the interference signal, and n is the noise. The received signal is put into the analog filters for channel selection. This can be

expressed by

$$y_0(t) = \int_0^{(L-1)T_s} h_0(\tau) r(t-\tau) d\tau, \tag{2.2}$$

$$y_1(t) = \int_0^{(L-1)T_s} h_1(\tau) r(t-\tau) d\tau, \tag{2.3}$$

where y_m is the output of H_m analog complex band pass filter for m-th channel,$h_m(\tau)$ is the impulse response of the m-th filter. The output of the analog filters is then converted to digital signals.

$$Y_0(n) = adc\left\{y_0(\Delta t + (n-1)T_s)\right\}, \tag{2.4}$$

$$Y_1(n) = adc\left\{y_1(\Delta t + (n-1)T_s)\right\}, \tag{2.5}$$

where Y_m is the output of the ADC for m-th channel, $adc\{X(t)\}$ represents the analog-to-digital conversion of $X(t)$ at the time t

Because the interference signal is much larger than the desired signal, the interference signal is still remaining in Y_0. In training period, the signal is processed by using Wiener filter to cancel the interference signal that remains in Y_0. The model of the Wiener Filter is shown in Fig. 2.10. The input of the Wiener filter is expressed by $\overline{\boldsymbol{Y}}(n) = [Y_0(n), Y_1(n), Y_1(n-1), ..., Y_1(n-M+1)]^T$, that is combination of Y_0 and Y_1 and tap coefficient vector is given by $\boldsymbol{w}(n) = [w_0(n), w_1(n), ..., w_M(n)]^T$. Autocorrelation of input signal,$\overline{\boldsymbol{Y}}$is expressed by,

$$\boldsymbol{R} = E[\overline{\boldsymbol{Y}}(n)\overline{\boldsymbol{Y}}^H(n)] \tag{2.6}$$

and cross-correlation of input signal, $\overline{\boldsymbol{Y}}$ and reference signal, $\boldsymbol{s}$ is expressed by

$$\boldsymbol{p} = E[\overline{\boldsymbol{Y}}(n)s^*(n)]. \tag{2.7}$$

This reference signal, $\boldsymbol{s}$, is created with random sequence which is known to the receiver. The optimal tap coefficient vector $\boldsymbol{w}_{opt}$ is calculated by using this equation

$$\boldsymbol{w}_{opt} = \boldsymbol{R}^{-1}\boldsymbol{p}. \tag{2.8}$$

In the reception period, the ACI is canceled with the trained optimal coefficient and is given by,

$$d_0(n) = \boldsymbol{w}_{opt}^H(n)\overline{\boldsymbol{Y}}(n). \tag{2.9}$$

The desired signal on the IF is then demodulated and decoded in the digital domain.

2.4 Experiment System

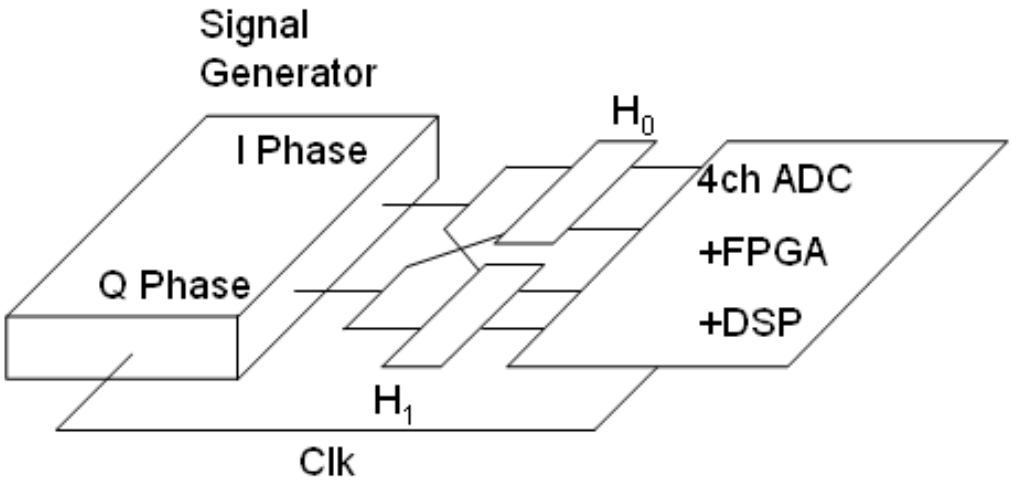

Figure 2.11: Model of the experiment system.

Table 2.1: Experiment Conditions

Signal Generator	2ch(I,Q), 14 bit 100Msps
Tx and Interference Signals	40 subcarriers OFDM, DQPSK
Demodulation	Differential Decodes
Signal bandwidth	2[MHz]
ADC	4ch, 12 bit, 10Msps
FPGA	Xilinx 1M Gate Virtex II
DSP	167MHz TMS320C6701 32bit Floating Point

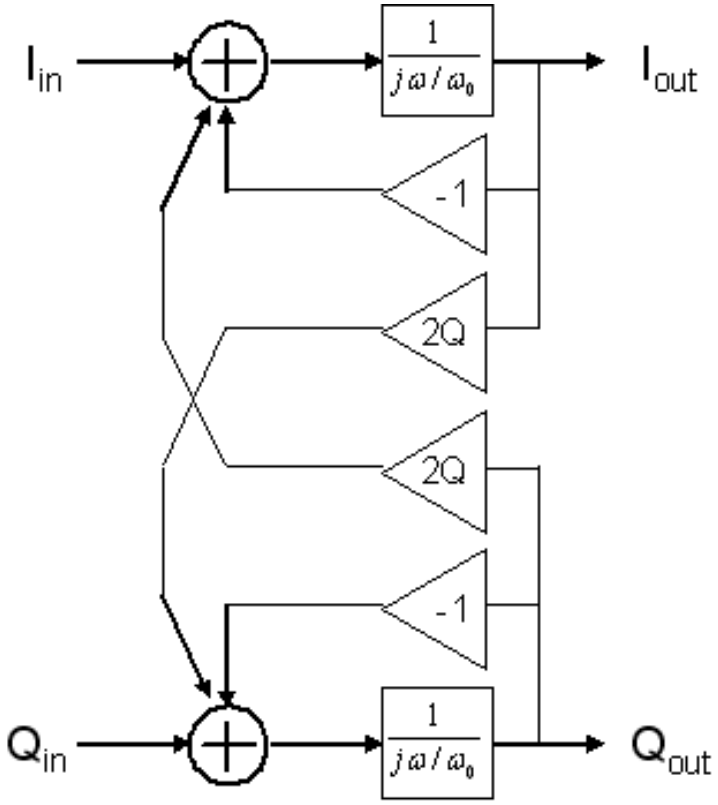

Figure 2.12: Model of the analog filter.

Figure 2.11 shows the model of the Experiment System. Table 2.1 shows the experiment conditions. In the experiment, IF signals are generated by using a dual-channel modulation signal generator. There are 4 outputs of the signal generator which 2 of them are I-phase and Q-phase of the signal, and the other 2 are the differential part of I/Q. The received IF signal data is modeled by using MATLAB program and signal generator is used to generate the IF signal. OFDM signals with variable signal-to-interference ratio (SIR) are generated to investigate performance of the proposed scheme.

The signals in the experiment are based on WLAN IEEE802.11a/g. However, due to the specification limitation of experiment equipments, the signals ware modeled with smaller scale of bandwidth and frequency spacing. In the experiment, the low-speed ADC and characteristics of the op-amp in the BPF limit the bandwidth and

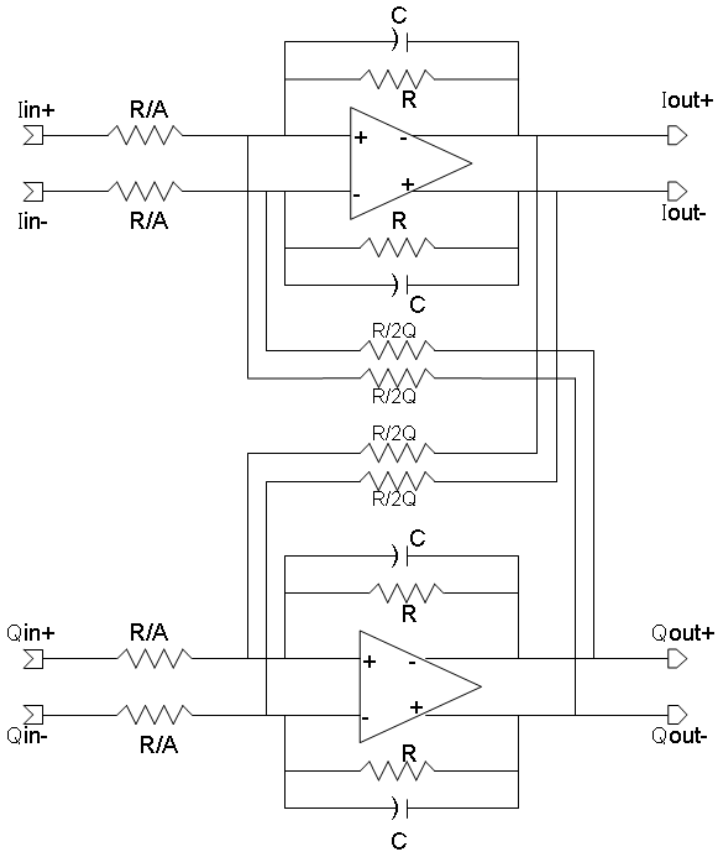

Figure 2.13: Single complex pole with active-RC filter.

frequency of the signal. Here, the bandwidth of each signal is set to 2[MHz] instead of 16.25[MHz], and channel spacing is set to 3[MHz] instead of 20[MHz]. The bandwidth of the signals are less concerned in the experiment because the purpose of the experiment is to examine the effect of analog filter response, and the nonlinearity and mismatch in analog devices to the digital signal processing. The response of the filter is estimated and the nonlinearity and mismatch in the analog devices the corrected through the adaptive signal processing.

The output of the signal generator is goes through the analog filter for channel selection. Channel selection in the proposed scheme is made by using complex analog band pass filters, H_0 and H_1. The model of the complex analog band pass filter is shown in Fig. 2.12[2]. With a complex filter it is possible to discriminate between the

negative and positive frequencies and therefore, the mirror frequency will be filtered out. H_0 allows only positive part of certain frequencies to pass and cut off negative frequency, while H_1 only allows same negative frequencies to pass. The transfer function H_0 and H_1 is given as

$$H_0(j\omega) = \left(\frac{1}{1 - 2jQ + j\omega/\omega_I}\right)^n, \tag{2.10}$$

$$H_1(j\omega) = \left(\frac{1}{1 + 2jQ + j\omega/\omega_I}\right)^n \tag{2.11}$$

where n is the number of the stages of the complex filters. ω_0 is the cut off frequency of the filter and 2Q is the relative center frequency of the complex filter. Many techniques can be used for the complex filters. In the experiment, single complex pole with active-RC filter technique is used. Figure 2.13[2] shows the circuit of the filter that used in the experiment.

Analog signal is converted to digital signal by using ADC in FPGA boards. The FPGA is programmed by using VHDL language to controls the sampling and resolution of the ADCs. In the experiment, 4 channels of ADCs are used, 2 channels are used to sample I-phase and Q-phase signals from output of H_0 filter and the other 2 channels are used to sample output from H_1 filter. Both boards are set to start sample at the same time and sampled with same sampling clock to synchronize the boards. The sampling frequency is set to 10 MHz. The input level of the received signal is adjusted to the maximum amplitude of the output of filter each. The resolution of ADCs is adjusted by changing the least significant bit (LSB) and most significant bit (MSB) of the ADCs. The maximum system resolution is 12[bits].

In the digital domain, the signal is processed with Wiener filter remove the remaining interference part. Finally the desired signal is demodulated and the performance in BER of the system is investigated.

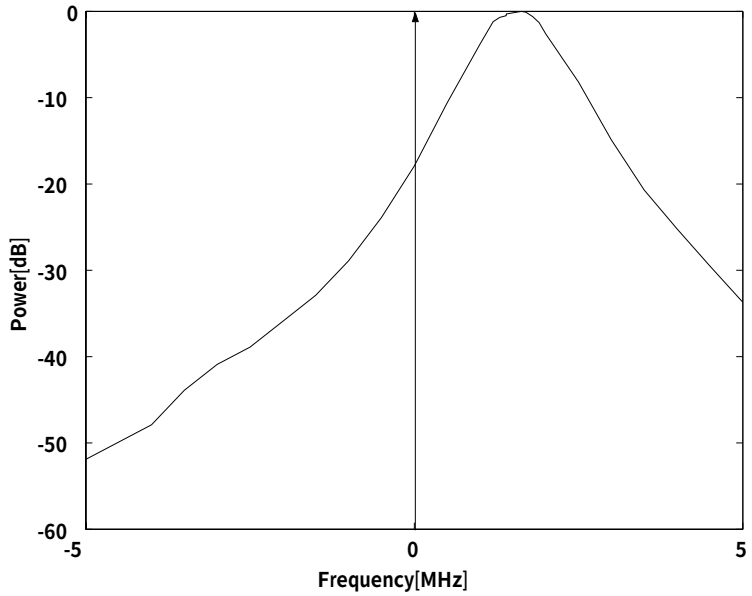

Figure 2.14: Normalize characteristic of the H_0 analog filter.

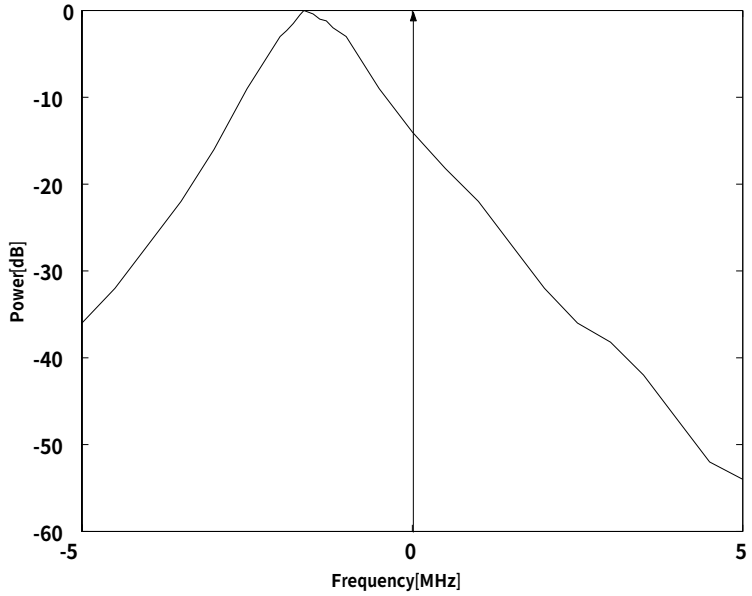

Figure 2.15: Normalize characteristic of the H_1 analog filter.

2.5 Experiment Results

Firstly, the characteristics of the analog complex band pass filter are investigated by using spectrum analyzer. Then the result from the spectrum analyzer is redrawn to

Table 2.2: Characteristics of the analog filters.

	H_0	H_1
Center Frequency	1.64[MHz]	-1.64[MHz]
Bandwidth	1.15[MHz]	1.15[MHz]
Q	1.426	1.426

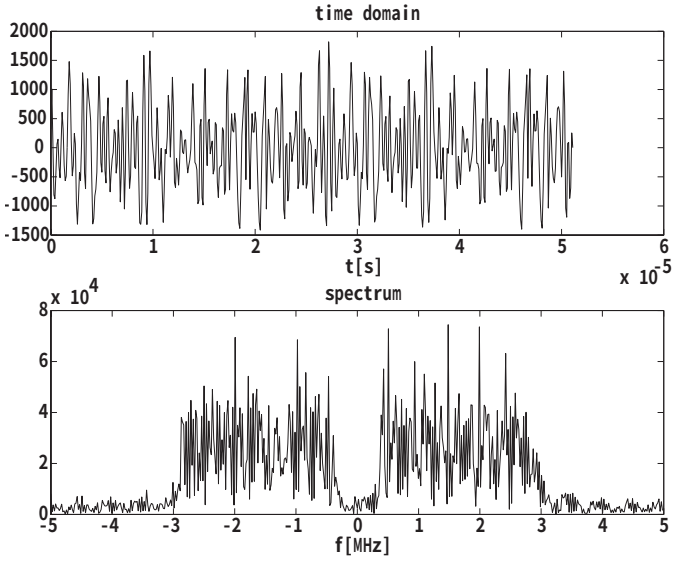

Figure 2.16: Input of the analog filters, SIR=0[dB] 64carrier QPSK/OFDM signal.

show the characteristic of the analog complex filters and the characteristic is shown in Fig. 2.14 for H_0 and Fig. 2.15 for H_1. The characteristics of the analog complex band pass filter are shown in Table 2.2. From these results, the center frequency of the H_0, ω_0 is 1.64[MHz] with bandwidth of 1.15[MHz] and the center frequency of the H_1, ω_1 is -1.64[MHz] with bandwidth of 1.15[MHz].

Spectrum analyzer cannot separate positive frequency and negative frequency, thus, to investigate positive and negative frequency, the output of the filter is analyzed with computer program. Figures. 2.16-2.19 show computer analysis of input and output of analog filter for 40-subcarriers DQPSK/OFDM signal. Signal with 0[dB] of SIR would have about the same power spectrum for both positive and negative

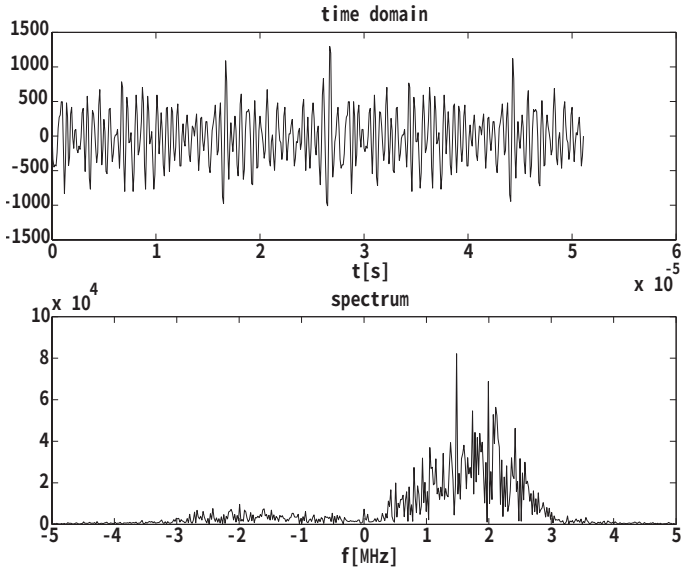

Figure 2.17: Output of H_0, SIR=0[dB] 64carrier QPSK/OFDM signal.

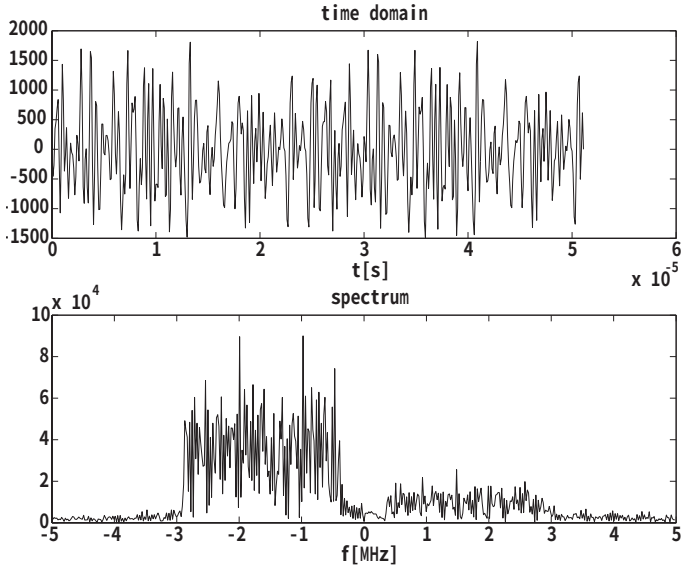

Figure 2.18: Input of the analog filters, SIR=-12[dB] 64carrier QPSK/OFDM signal.

frequency such as shown in Fig. 2.16. When the signal is filtered by the H_0 analog filter, only the positive part of the signal remain such as shown in Fig. 2.17. This means the filter only let the positive frequency pass through and select only the desired channel. However, when SIR is -12[dB] such as in Fig. 2.18, Interference

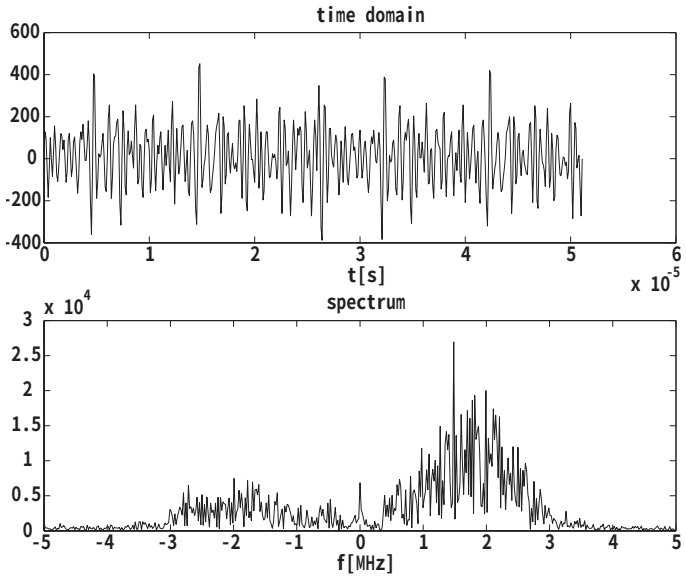

Figure 2.19: Output of H_0, SIR=-12[dB] 64carrier QPSK/OFDM signal.

part would have much larger power than the desired signal. When the signal is pass through H_0 the negative frequency of the signal is still remaining in a small power as in Fig. 2.19.

When interference power is much larger than desired signal, negative frequency part would still remain in Y_0 although it had filtered by H_0 as shown in Fig. 2.20(a). Meanwhile, only negative frequency part left in Y_1 which is output of H_1 as shown in Fig. 2.20(b). When the signal is processed with Wiener filter, the output of the filter (Fig. 2.20(d)) is seemed similar to reference signal (Fig. 2.20(c)) which only includes desired signal. In other words, the proposed scheme effectively cancels the interference. However when SIR is about -24[dB], the output of the Wiener filter is still not similar to the reference signal.

Figure 2.21 shows BER versus number of coefficient for Wiener filter with different SIR. The Wiener filter cannot approximate the characteristic of the interference if the number of coefficient is too small. The performance of the Wiener filter is converging when the number of coefficient is enough. However, if the number of coefficient is

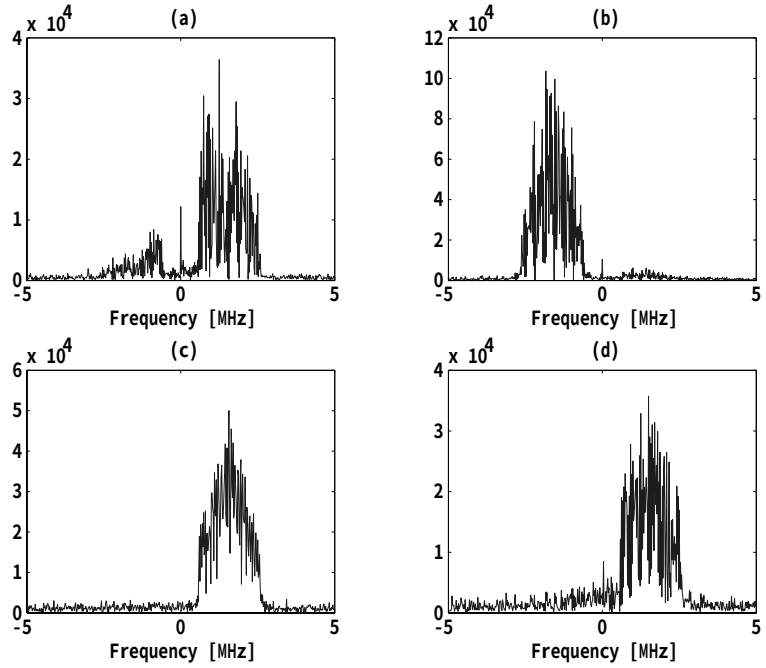

Figure 2.20: SIR=-12[dB],SNR=20[dB],Spectrum of (a)Y_0 (b)Y_1 (c)Reference signal,s, (d)Output of Wiener filter,d

too large, much more noise components, such as thermal noise, quantization noise, and other floor noises, will be included while approximates the interference. Due to the noises, the non-related coefficients are falsely estimated. This will make the performance worse. In Fig. 2.21, the performance seems to be converging when the number of coefficient is between 10 and 50. In this experiment, the number of coefficient is set to 20. The coefficient training process take about 1 OFDM symbol period to converge. In the case of WLAN system, the training process can be done during preamble period. Figure 2.22 shows the estimated coefficients after 2 OFDM symbol period.

Figure 2.23 shows BER versus SIR with and without the adaptive digital signal processing in the proposed receiver architecture. In this figure, 'no side lobe energy' means that the signal on the adjacent channel does not have the side lobe energy and no interference occurs. When the SIR is less then -18[dB] the Wiener filter seems

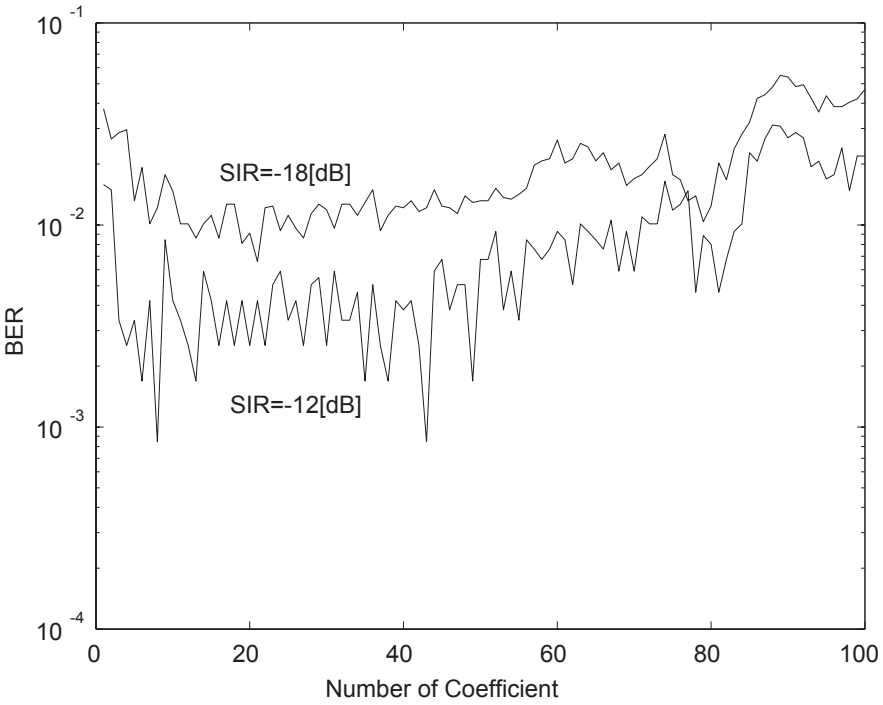

Figure 2.21: BER vs. Number of coefficient, SNR=10[dB].

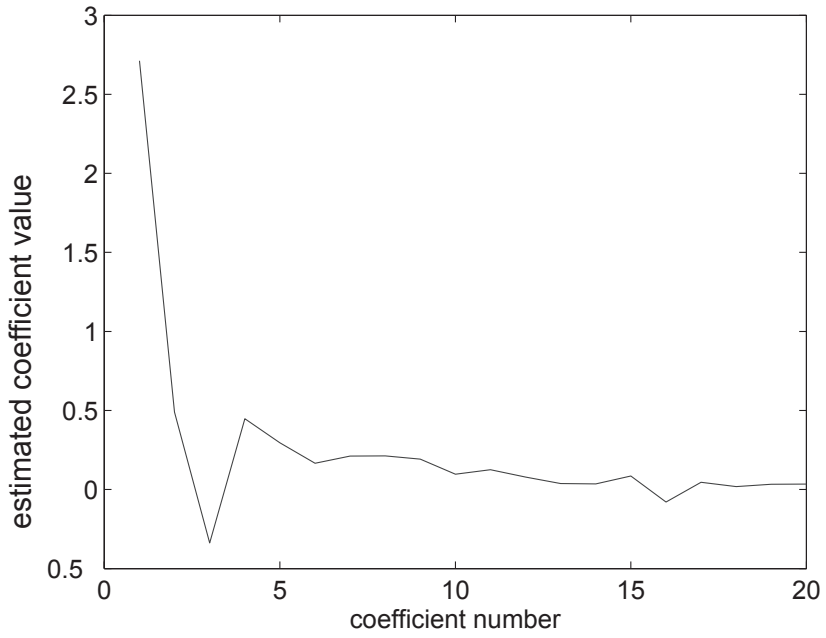

Figure 2.22: Estimated coefficients.

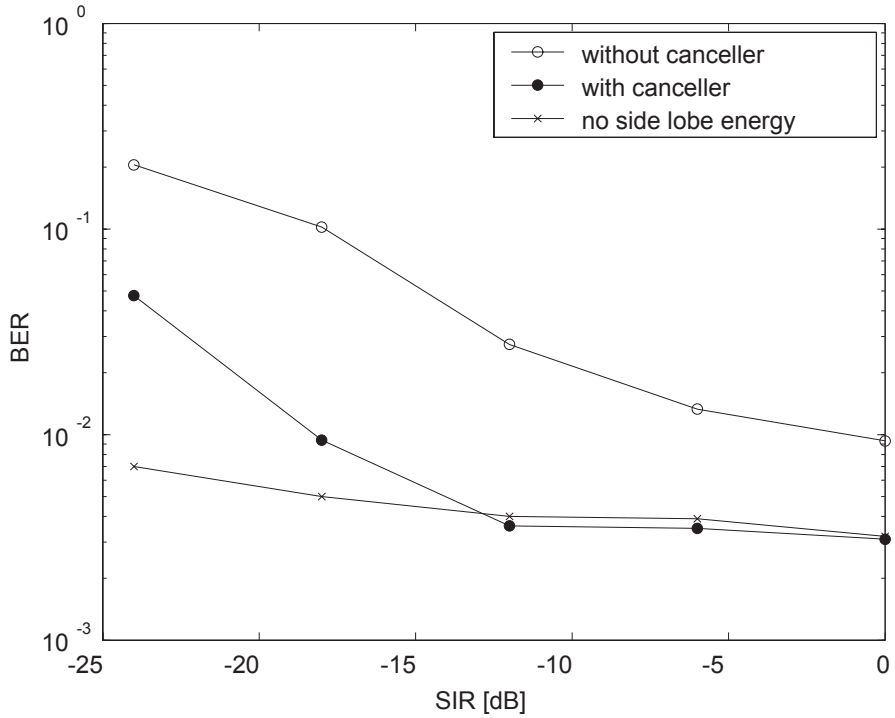

Figure 2.23: BER vs. SIR, SNR=10[dB], resolution [8bits].

effectively cancel the interference and improves the BER performance. However, when the SIR is -24[dB], there is no much difference in performance. If the adjacent channel signal level is very high, the quantization error of the signal is also high. This will make the canceller hard to approximate the characteristics of the interference signal. As the result, the interference can not be eliminated completely and the performance degraded. From the figure, it can concluded that the effect of ACI can be reduced by about 18[dB] when the BER is 10^{-2}.

Figure 2.24 shows BER versus SNR when SIR is fixed. There is not much difference in BER performance when the SNR is varied for the signal without interference cancellation. The Wiener filter work better in low power of noise however it still can work effectively in high power of noise.

Figure 2.25 shows BER versus the resolution of ADCs when SIR is set to -12[dB]. If the resolution of ADCs is 6[bits]-8[bits], the Wiener filter effectively improve the

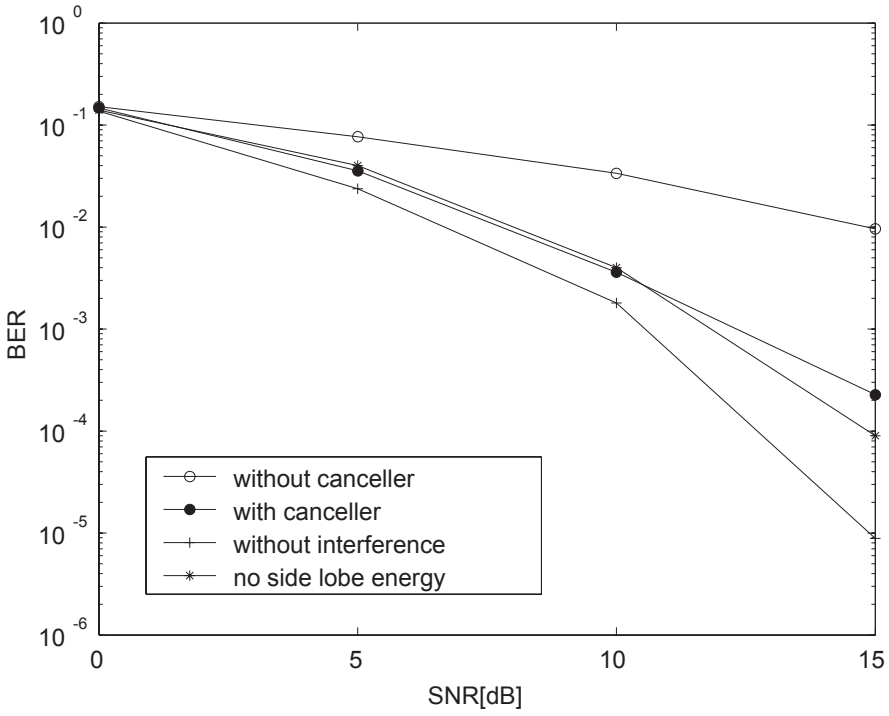

Figure 2.24: BER vs. SNR, SIR=-12[dB], resolution 8[bits].

BER performance. When higher resolution then 6[bits] are used for SIR=-12[dB], the improvement is very small. However when the ADC is 4[bits], there is not much difference in the BER performance between the filtered signal and not filtered signal. The reason is that the reconstructed signal through the adaptive signal processing includes the error due to the quantization noise. From the result, it is clear that 6[bits] is enough for resolution when the SIR is lower then -12[dB] and SNR=10[dB].

Figures. 2.24 and 2.25 show that the BER with canceller becomes close to that of no sidelobe energy and it does not become close to the case without interference. This because the canceller cannot estimate the interference components perfectly due to the quantization errors. The false coefficients estimation also happened in the case of no sidelobe energy which degraded the performance. Another reason is because of the IQ imbalance phenomena in the analog components. Due to the IQ imbalance in the analog components especially the complex BPF, the images from the mirror

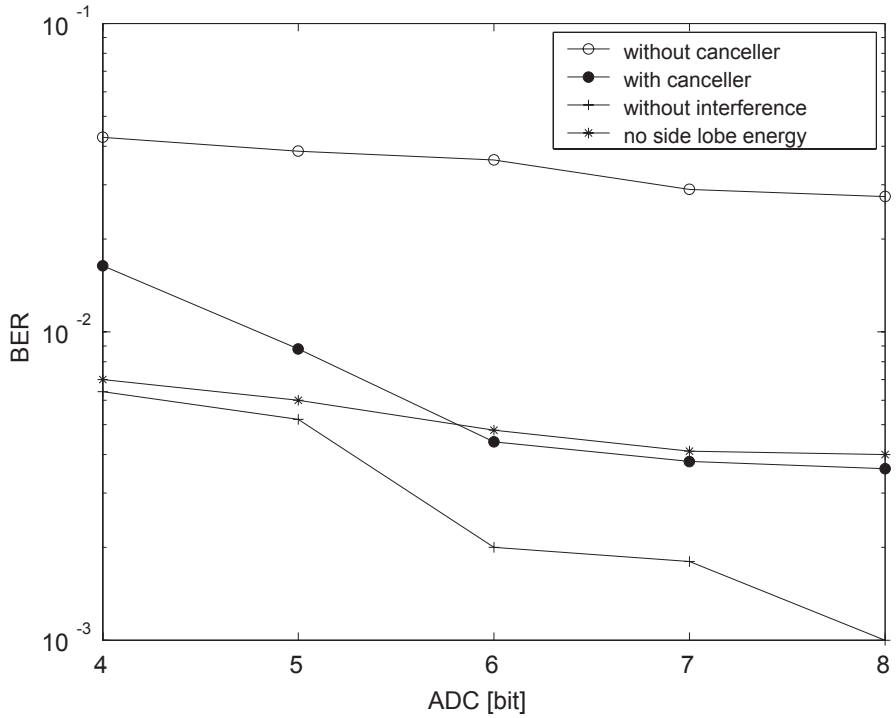

Figure 2.25: BER vs. Resolution of ADC, SIR=-12[dB], SNR=10[dB].

signal reconstructed in the desired signal band. The images can be cancelled with simple modification of the Wiener filter i.e. by inputting conjugated interferer signal for estimation and cancellation.

2.6 Conclusion

In this chapter, the ACI cancellation scheme with analog filter bank for multi-channel reception has been proposed. From experiment results, it has been shown that the proposed scheme can mitigate the influence from the adjacent channel and enables multi-channel reception with relatively low resolution of ADCs with the adaptive digital signal processing. Therefore, the propose scheme can be applied to VoIP services with WLANs. From the results, the proposed scheme effectively cancels the interference and improved the BER performance when the resolution of ADCs is 6[bits] and more, and the SIR is less then -18[dB]. The effect of ACI can be reduced

by about 18[dB] for BER=10^{-2}.

Chapter 3

Undersampling in Multi-channel Reception Scheme

In this chapter an adjacent channel interference (ACI) cancellation scheme with undersampling for multi-channel reception is proposed and investigated. Low-IF receiver architecture is used in the multi-channel reception scheme. In this system, signal in the adjacent channel causes interference to the desired signal. The ACI cancellation scheme with analog filter bank has been proposed to mitigate the influence from the adjacent channel in Chapter 2. Undersampling technique is applied in this system in order to lower the required sampling frequency and power consumption. The effects of the adjacent channel to the undersampling technique in this scheme is examined and discussed.

3.1 Introduction

Recently, cellular and wireless local area network (WLAN) systems have grown rapidly and generated various competing transmission formats. In the need of seamless communication across incompatible radio standards, the SDR concept has received much attention among researchers working in wireless communication. SDR is a new technology that allows a single terminal to support various kinds of wireless systems and services such as mobile systems and WLANs by changing software to

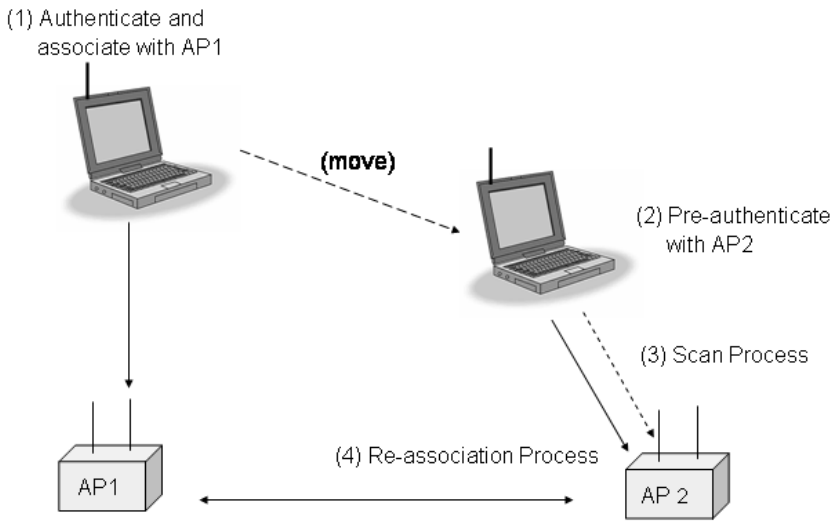

Figure 3.1: Roaming example with IEEE802.11 MAC Protocol.

reconfigure the wireless terminal.

A variety of architectures have been proposed to realize the SDR [1–3, 7, 10, 42]. In direct conversion receiver (DCR), the desired signal mixed directly to baseband signal [10]. However, local oscillator (LO) to RF leakage can result in a large dc offset. In low-IF receiver, received signal is not directly down converted to baseband signal; therefore, this architecture may not suffer from DC-offset problem [32].

In the low-IF receiver, the IF is set to be relatively lower than that in the conventional IF receivers. There are several merits by using low-IF receiver architecture. Low-IF receivers are not using SAW filter so that this architecture would have low cost and low power consumption as compared to super-heterodyne architecture. The low-IF receiver is much easier to make in 1 chip and the structure of the low-IF receiver can be much simpler than the super-heterodyne receiver.

The low-IF receiver architecture can be applied to the multi-channel receiver system [34, 35]. Multi-channel receiver is a system that can receive and process multiple channels simultaneously. Multi-channel receiver may be applied to wireless systems

such as WLAN for quick roaming. However in such applications, the adjacent channel may causes interference to the desired signal. The ACI component may directly overlap with the desired signal if the interference is much larger than the desired signal. The system performance degraded due to the out-of-band leakage of adjacent channel signal and, also, the large interference reduces effective resolution of ADCs to the desired signal. Thus, high resolution ADCs have to be employed. The increase of the resolution of the ADC causes higher power consumption and higher implementation cost.

In order to mitigate the influence from the ACI, a new ACI cancellation scheme with the analog filter bank has been proposed [35]. This scheme automatically estimates the characteristics of the interference signal and cancels it from the received signal through Wiener filter. The performance of the proposed scheme in the influence of ACI from the adjacent channel which is in the mirror frequency of the desired signal has been investigated and discussed. However, the proposed scheme requires multiple ADCs. Also the low-IF receiver requires higher sampling frequency than the conventional architecture such as super-heterodyne. Thus, the power consumption of the ADCs may be a problem. Undersampling technique is then applied in this system in order to lower the required sampling frequency and ADC power consumption. In this chapter, side effect of the undersampling technique to the multi-channel reception is investigated through the experiment. The influence of aliasing effect in the undersampling is reduced in digital domain by using adaptive digital signal processing.

3.2 Multi-Channel Reception

3.2.1 Roaming Protocol

The mobility of WLAN terminals among multiple base stations is specified in Extended Service Set (ESS) of IEEE802.11 MAC protocol [40]. An example of roaming capability with IEEE802.11 MAC is shown in Fig. 3.1. As the terminal finds AP1, it will authenticate and associate with AP1. As the terminal moves, it may pre-authenticate with AP2. When signal quality from the current AP drops below a threshold value, a terminal is triggered to start handover procedure. The terminal has to search for a new AP which is accomplished by scanning procedure in MAC layer function. Scanning can be accomplished either in passive or active mode. In active scan mode, probe request frames on each channel are used to detect wireless activity. In passive scanning, the terminal listens for beacons from APs occasionally to find candidate APs. Generally, these beacons are issued by all APs at a rate of 10 beacons per second. The scanning delay accounts most of the overall handover delay which takes more than 100 ms. As the terminal finds AP2, it may re-associate with AP2. In the re-association process, a delay incurred during the exchange of re-association frames between the terminal and the new AP and also between the AP1 and the AP2 which takes a few milliseconds.

Due to the latency problem, it is not suitable for quick roaming in some applications such as VoIP over WLAN requires. It is recommended that overall latency does not exceed 50 ms to realize VoIP over wireless LAN [43].

3.2.2 Multi-Channel Reception with Low-IF Architecture

In order to solve the latency problem in roaming process, multi-channel reception capability is required. For example, In IEEE802.11g WLAN systems, 4 channels in 2.4 GHz band are utilized to cover large area for the services. Thus, if these 4

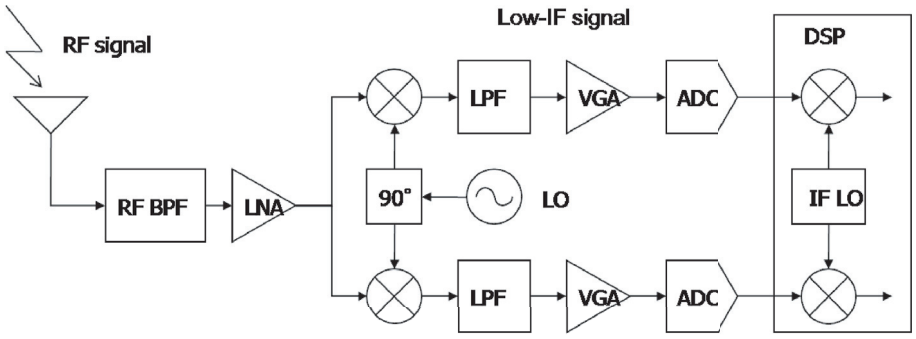

Figure 3.2: Low-IF receiver architecture.

channels can be demodulated by one receiver, the quick roaming may be possible and the mobile VoIP service over WLAN can be provided.

Multi-channel reception receiver can demodulate signals in multiple channels simultaneously. By using multi-channel reception, a receiver would perform scan process while connecting and receiving information data to an access point. Therefore, the scanning delay in handover process can be eliminated by utilizing multi-channel reception. There are several receiver architectures applicable for multiple channel reception. The simplest architecture is to combine 4 independent receivers in one package. While one of the receivers connects to an access point, the other receivers would perform scan process. A seamless handover system using 2 set of WLAN device on a mobile node applying this concept has been proposed [41]. However, this architecture has large redundancy in their circuits and it is not efficient since multiple set of RF circuit are required.

Another candidate is to use the low-IF receiver. Multi-channel reception can be realized easily by utilizing a low-IF receiver since multiple channels can be down converted to IF signal at once. The structure of the low-IF receiver is shown in Fig. 3.2. The received signal is first down converted to the IF signal. Then the IF signal is converted to the digital signal with the ADCs and finally converted to the baseband signal with the DSP. As the final down conversion is carried out with the

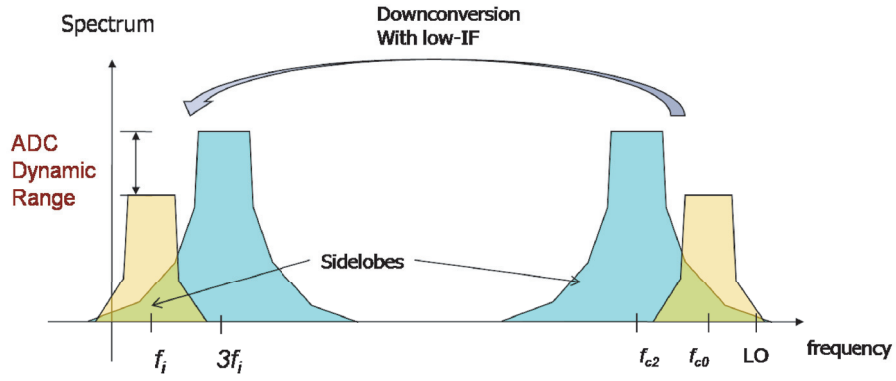

Figure 3.3: Downconversion of multi-channel and interference due to the signal in the adjacent channel.

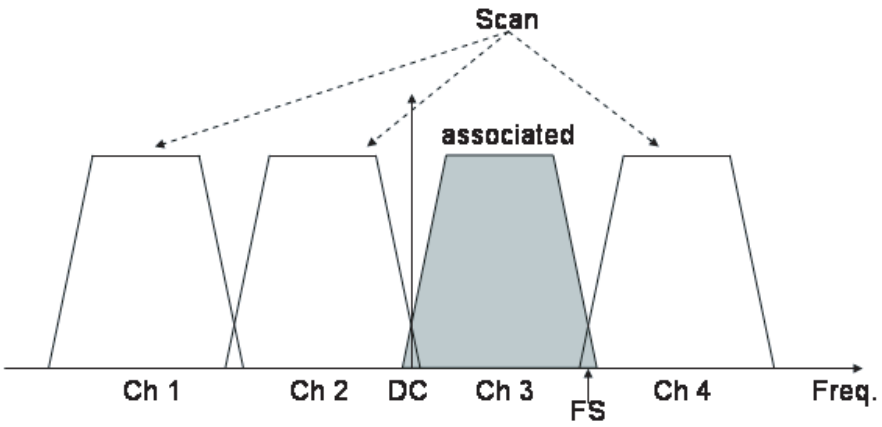

Figure 3.4: 4 bands of WLAN after downconversion with low-IF receiver.

DSP, it is possible to select one of 4 channels easily. The channels in WLAN after the down conversion can be processed separately. Therefore, multiple channels can be received and demodulated simultaneously with a low-IF receiver.

3.2.3 Adjacent Channel Interference (ACI)

In the low-IF receivers, ADCs with very high dynamic range may be required if the signal power in the adjacent channel is much larger than the desired signal as shown in Fig. 3.3. "Fs" in the figure means sampling frequency. Moreover, the desired signal may suffer from the interference signals which are adjacent in frequency to

the desired signal. This is called ACI. This interference occurs because the adjacent channel generates side lobe energy that falls into the pass band of the desired signal. The side lobe energy degraded the performance of the desired signal.

Figure 3.4 shows 4 WLAN channels after down conversion. As a receiver is associated with channel 3, the receiver may perform scanning process to search other available channel. The signals from channel 2 and 4 which are adjacent of channel 3 may interfere the desired signal. The effect of inference from channel 2 which is in the mirror frequency of the desired signal and its cancellation performance has been discussed in [35]. This chapter discusses the inference effect of the adjacent channel which is at the higher frequency band (channel 4 in Fig. 3.4) and its cancellation performance.

3.2.4 ACI Cancellation with Undersampling

Undersampling technique is applied in this scheme in order to lower the required sampling frequency and power consumption of the ADC. In the conventional sampling technique, Nyquist rate is required to sample the received signal. Desired signal can be sampled with sampling frequency below Nyquist rate by using the undersampling technique. The undersampling translates a high frequency bandpass signal to a near zero lowpass frequency. The sampling frequency requirement is based on the signal bandwidth rather than its highest frequency.

Any out of band signal or noise must be kept to minimum because they will fold down to the desired signal band. A band pass filter (BPF) of very high Q is required to suppress the out of band signal. If the signal in the adjacent channel is much larger than the desired signal, the BPF cannot eliminate the signal completely due to the restriction of the circuit size. The remaining adjacent channel signal will interfere the desired signal by folding down to the desired signal channel. As the result, the desired signal cannot be demodulated.

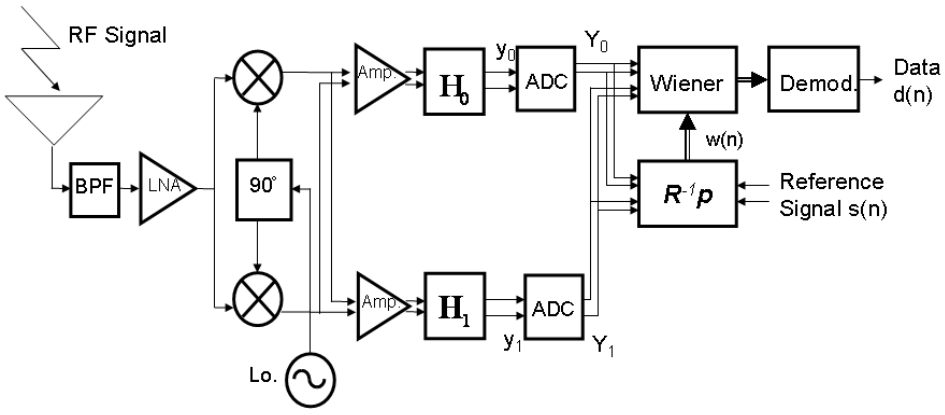

Figure 3.5: Model of the receiver with the proposed scheme.

3.3 System Model

Analog-digital signal processing is utilized to reduce the dynamic range of the ADCs and reduce the ACI. In [32, 33] it has been shown that the analog filter bank can reduce the dynamic range of the ADCs. However, due to the restriction of the circuit size and the mismatch of the analog components, it is hard to realize high Q analog filter. In addition to the analog filter bank, adaptive digital signal processing for ACI cancellation scheme is utilized to reduce the ACI [35].

The model of the receiver with the proposed scheme is shown in Fig. 3.5. The received signal first goes through the RF BPF and LNA. The output of the LNA is then multiplied with the local signal and converted to the IF. The signals on the different channels are separated by two analog complex BPFs with variable center frequency function, H_m, where integer $m(0 \leqq m < 3)$ is the channel number. The filter would have switchable function to 4 difference bands. The center frequency of the filters is adjusted depending on the current channel and the roaming channel. However, variable center frequency filter with high Q may be hard to realize [10]. A filter with these specifications cannot be integrated and realized with discrete components. These filters are expensive and vulnerable. The other way is to use a

multi-channel filter bank instead of variable center frequency BPF. For the WLAN channels shown in Fig. 3.4, 4 channels filter bank are required. The filter bank can be realized on chip with OTA-C technique though it may required relatively large chip area as compared to a single IF filter [44, 45].

When a higher frequency signal is received, the signal is down folded to the lower frequency with the undersampling technique. The interference due to the adjacent channel that is down folded to the desired signal channel is eliminated by Wiener filter.

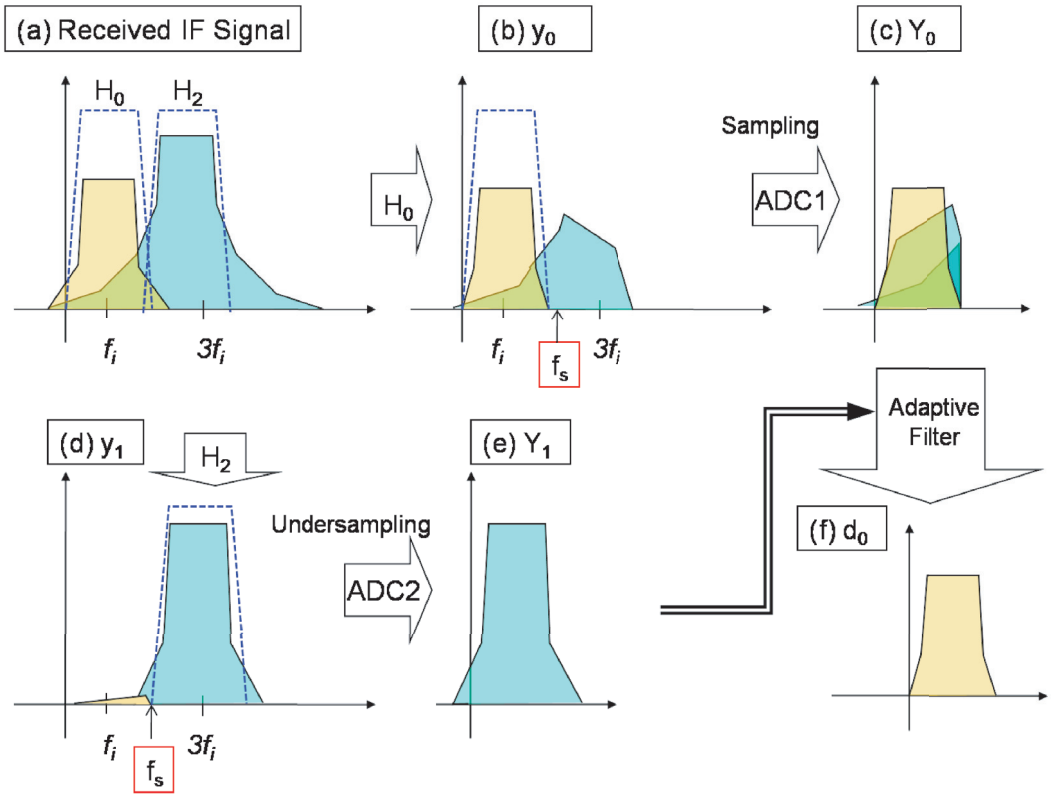

Figure 3.6: Signal model.

Suppose that the desired signal and the adjacent channel signal are received at the same time as shown in Fig. 3.6(a). The center frequency of the adjacent channel signal is set to 3 times higher than the desired signal. The received signal is expressed

as

$$r(t) = d(t)\exp(j\omega_i t) + I(t)\exp(3j\omega_i t) + n(t) \tag{3.1}$$

where $r(t)$ is the sample of the received signal at the time t, $d(t)$ is the desired signal, $I(t)$ is the signal on the adjacent channel, $\omega_i = 2\pi f_i$ is the intermediate frequency of the desired signal, $3\omega_i$ is the frequency of the adjacent channel signal, and $n(t)$ is the noise. The received signal is put into the analog filters for channel selection. This can be expressed by

$$y_m(t) = \int_0^{(L-1)T_s} h_m(\tau) r(t-\tau) d\tau, \tag{3.2}$$

where y_m is the output of H_m analog complex BPF for m-th channel, L is the length of the signal, and $h_m(\tau)$ is the impulse response of the H_m filter. The transfer function of the filters are given as

$$H_m(j\omega) = \left(\frac{1}{1 - 2jQ_m + j\omega/\omega_0}\right)^n, \tag{3.3}$$

where n is the number of the stages of the complex filters. ω_0 is the cut off frequency of the filter and $2Q_m$ is the relative center frequency of the complex filter on the m-th channel. The center frequency of H_0 and H_2 is set to the desired signal and the adjacent channel signal respectively. Therefore, $2Q_m$ is set to ω_I and $3\omega_I$ for the desired signal and the adjacent channel signal. The output of H_0 and H_2 is shown in Fig. 3.6(b) and (d). The output of the analog filters is then converted to digital signals.

$$Y_m(n) = adc\left\{y_m(\Delta t + (n-1)T_s)\right\}, \tag{3.4}$$

where Y_m is the output of the ADC for m-th channel, Δt is time delay, $adc\{X(t)\}$ represents the analog-to-digital conversion of $X(t)$ at the time t and T_s is the sampling interval. The sampling frequency of the ADCs is set lower than the frequency of channel 2. As the effect of undersampling, the remained adjacent channel frequency of H_0 output will be down folded to the desired signal channel such as in Fig. 3.6(c).

The adjacent channel signal of H_1 output will be down folded to the lower frequency such as in Fig 3.6(e).

In the training period, the signal is processed by using Wiener filter to cancel the interference signal that remained in Y_0. The input of the Wiener filter is expressed by $\overline{\boldsymbol{Y}}(n) = [Y_0(n), Y_1(n), Y_1(n-1), ..., Y_1(n-M+1)]^T$ that is the combination of Y_0 and Y_1, and the tap coefficient vector is given by $\boldsymbol{w}(n) = [w_0(n), w_1(n), ..., w_M(n)]^T$. Autocorrelation of input signal, $\overline{\boldsymbol{Y}}$, is expressed by,

$$\boldsymbol{R} = E[\overline{\boldsymbol{Y}}(n)\overline{\boldsymbol{Y}}^H(n)], \tag{3.5}$$

and cross-correlation of input signal, $\overline{\boldsymbol{Y}}$, and reference signal, $\boldsymbol{s}$, is expressed by

$$\boldsymbol{p} = E[\overline{\boldsymbol{Y}}(n)\boldsymbol{s}^*(n)]. \tag{3.6}$$

This reference signal, $\boldsymbol{s}$, is created with random sequence which is known to the receiver. The optimal tap coefficient vector, $\boldsymbol{w}_{opt}$, is calculated by using this equation,

$$\boldsymbol{w}_{opt} = \boldsymbol{R}^{-1}\boldsymbol{p}. \tag{3.7}$$

In the reception period, the ACI is canceled with the trained optimal coefficient and is given by,

$$d_0(n) = \boldsymbol{w}_{opt}^H(n)\overline{\boldsymbol{Y}}(n). \tag{3.8}$$

From the Wiener filter process, the desired signal without interference part is obtained such as shown in Fig 3.6(f). The desired signal on the IF is then demodulated and decoded in the digital domain.

3.4 Experiment Results

3.4.1 Experiment System

Figure 3.7 shows the model of the experiment system. The experiment conditions are shown in Table 1. In the experiment, IF signal is generated by using a dual-channel

Table 3.1: Experiment Conditions.

Tx and Interference Signals	64 Carrier OFDM, DQPSK
Demodulation	Differential Decoding
Signal bandwidth	2[MHz]
Signal Generator	2ch(I,Q), 14 bit 100Msps
Noise Generator	4ch input, 4ch output, 12 bit 10Msps
ADC	4ch, 12 bit, 10Msps
FPGA	Xilinx 1M Gate Virtex II
DSP	167MHz TMS320C6701 32bit Floating Point

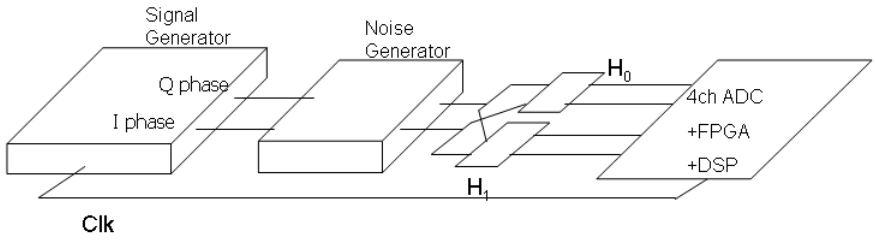

Figure 3.7: Model of the experiment system.

modulation AMIQ signal generator. There are 4 outputs of the signal generator which 2 of them are I-phase and Q-phase of the signal, and the other 2 are the differential output of I and Q. The signalfs data files are made by MATLAB program and signal generator is used to generate the IF signals. OFDM signals with different signal to interference ratio (SIR) are generated to investigate the performance of the proposed scheme. Gaussian noise is added to the IF signals by using FS-2221 Option Waveform Generator. 4 channels of input and 4 channels of output are used in the experiment. The sampling frequency of the generator is set to 10[MHz]. The noise level is varied from SNR=0[dB] to SNR=10[dB].

The received signals model in the experiment are based on WLAN IEEE802.11a/g. However, due to the specification limitation of experiment equipments, the signals

ware modeled with smaller scale of bandwidth and frequency spacing. The low-speed ADC and characteristics of the op-amp in the BPF limit the bandwidth and frequency of the signal. Here, the bandwidth of each signal is set to 2[MHz] instead of 16.25[MHz], and channel spacing is set to 3[MHz] instead of 20[MHz].

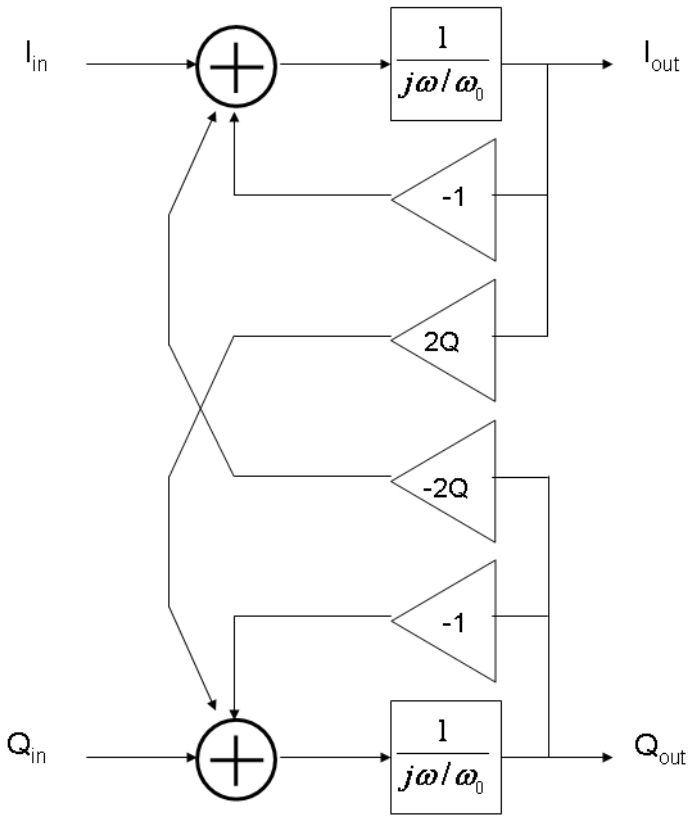

Figure 3.8: Model of the analog filter.

Then the signals go through complex band-pass analog filters, H_0 and H_2 for channel selection. Channel selection in the proposed scheme is made by using complex analog band pass filters, H_0 and H_2. The model of the complex analog band pass filter is shown in Fig. 3.8. With a complex filter it is possible to discriminate between the negative and positive frequencies and therefore, the mirror frequency will be filtered out. The center frequency of H_2 is set 3 times larger then H_0. The transfer function

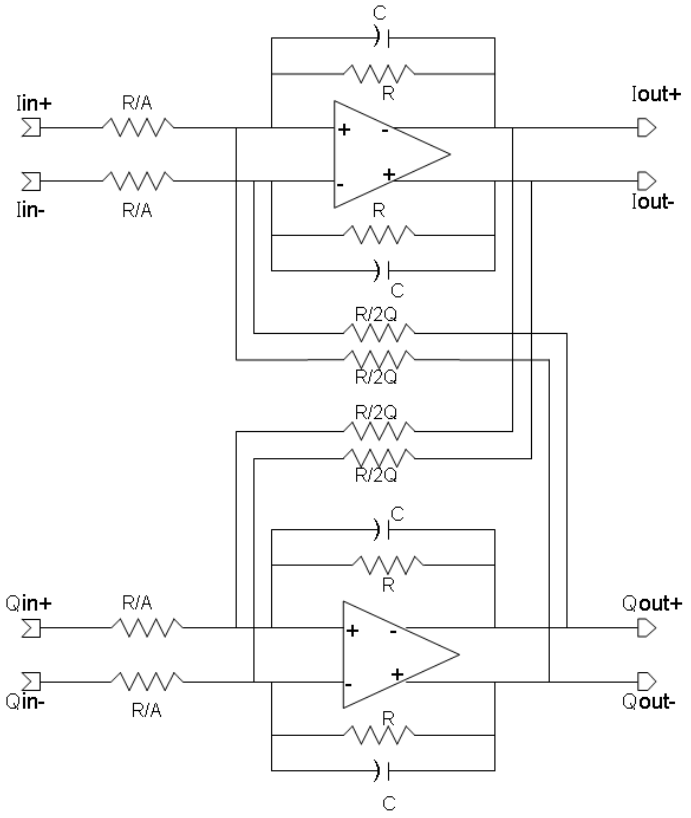

Figure 3.9: Single complex pole with active-RC filter.

H_0 and H_2 is given as

$$H_0(j\omega) = \left(\frac{1}{1 - 2jQ_0 + \omega/\omega_0}\right)^n, \tag{3.9}$$

$$H_2(j\omega) = \left(\frac{1}{1 - 2jQ_2 + \omega/\omega_0}\right)^n, \tag{3.10}$$

where $2jQ_0 = \omega_I$ and $2jQ_2 = 3\omega_I$. The complex filter are built using active-RC technique as shown in [10]. Figure 3.9 shows the circuit of the filter that used in the experiment.

Analog signal is converted to digital signal by using ADC with FPGA board. The FPGA is programmed by using VHDL language to controls the sampling of the A/Ds. In the experiment, 4 channels of ADCs are used, 2 channels are used to sample I-phase and Q-phase signals from output of H_0 filter and the other 2 channels are

used to sample output from H_2 filter. Both boards are set to start sample at the same time and sampled with same sampling clock to synchronize the boards. The sampling frequency, $f_s = 1/T_s$ is set to 10 MHz. The sampling frequency is changed to 5[MHz] and 2.5[MHz] to investigate the performance of the undersampling. The input level of the received signal is adjusted to the maximum amplitude of the output of each filter.

In the digital domain, the signal is processed with Wiener filter to remove the ACI. Finally the desired signal is demodulated and the performance in the BER of the system is investigated.

3.4.2 Characteristics of the Analog Complex Filters

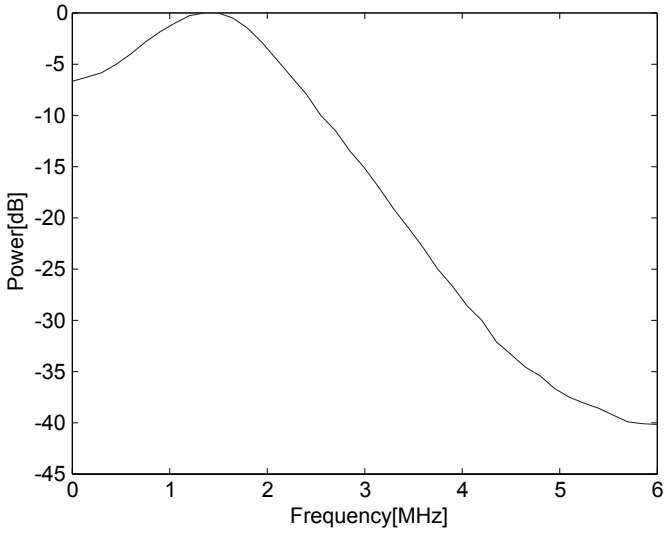

Figure 3.10: Normalized characteristic of the H_0 analog filter.

Firstly, the characteristics of the analog complex BPFs are investigated by using spectrum analyzer. The characteristic of the analog complex BPFs is shown in Fig. 3.10 for H_0 and Fig. 3.11 for H_2. The center frequency, the bandwidth, and the Q of the filters are shown in Table 3.2.

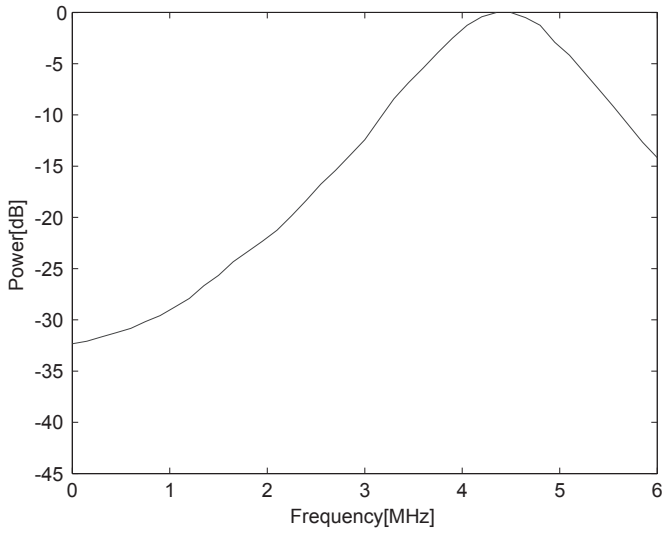

Figure 3.11: Normalized characteristic of the H_2 analog filter.

Table 3.2: Characteristics of the analog filters.

	H_0	H_2
Center Frequency	1.42[MHz]	4.45[MHz]
Bandwidth	1.22[MHz]	1.15[MHz]
Q	1.16	3.87

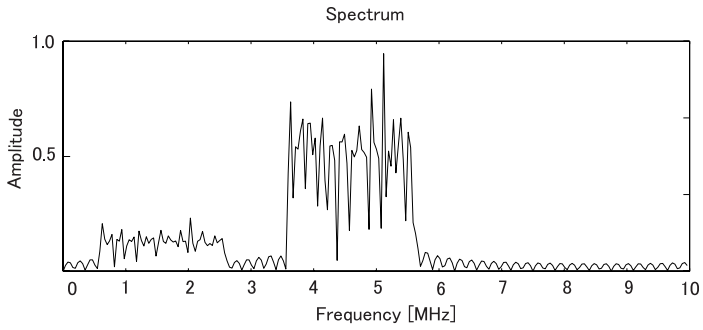

Figure 3.12: Received signal, SIR=-12[dB].

In the experiment, 2 channels are used to examine the undersampling effect to this system. Center frequency of the desired signal channel is set to 1.5[MHz] and center frequency of the adjacent channel is set to 4.5[MHz]. The bandwidth of the signals

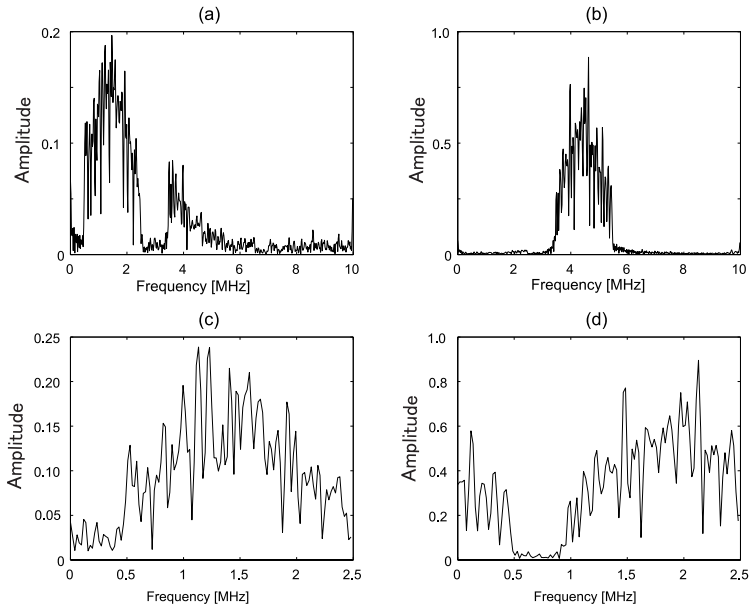

Figure 3.13: (a) Output of H_0 BPF, f_s=10[MHz] (b) Output of H_2 BPF, f_s=10[MHz] (c) Output of H_0 BPF, f_s=2.5[MHz] (d) Output of H_2 BPF, f_s=2.5[MHz].

is set to 2[MHz]. Spectrum of the received signal when the SIR=-12[dB] is shown in Fig. 3.12. When the received signal is filtered by analog complex BPF, H_0, the adjacent channel is reduced as shown in Fig. 3.13(a). When the sampling frequency is set to 2.5[MHz] such as shown in Fig. 3.13(c), the remained adjacent channel will be down folded to the desired channel and degrades the performance.

3.4.3 BER Performance

In order to verify the experiment system, signal without adjacent channel or interference has been examined. The BER performance is shown in Fig. 3.14. The performance of the system is almost the same as the theory when the sampling frequency is 10[MHz], however, it is degraded a little compared to the theoretical performance as the SNR increase. This is because of noise floor, system noise, and filter noise. When the sampling frequency is set to 2.5[MHz], the performance is degraded a little more. This is because the outband side lobe energy of the signal is down folded to

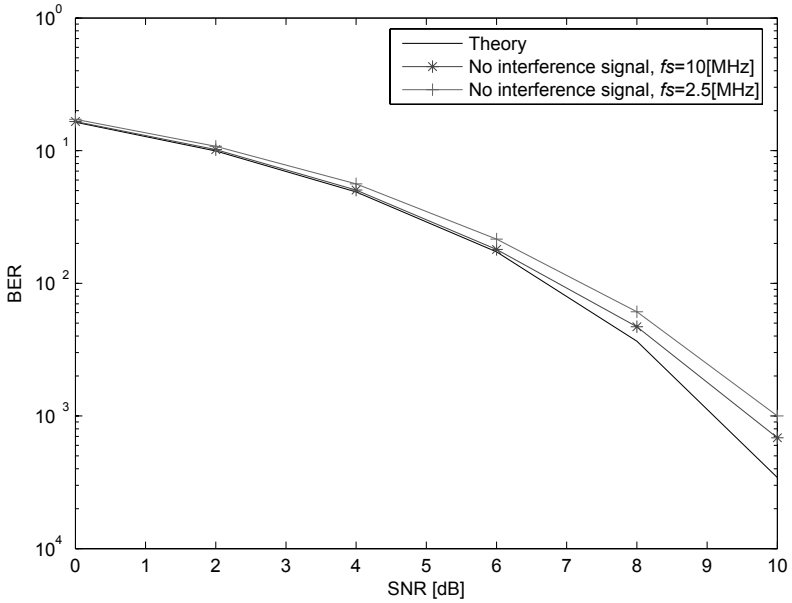

Figure 3.14: Signal without interference, resolution of ADC = 8[bits].

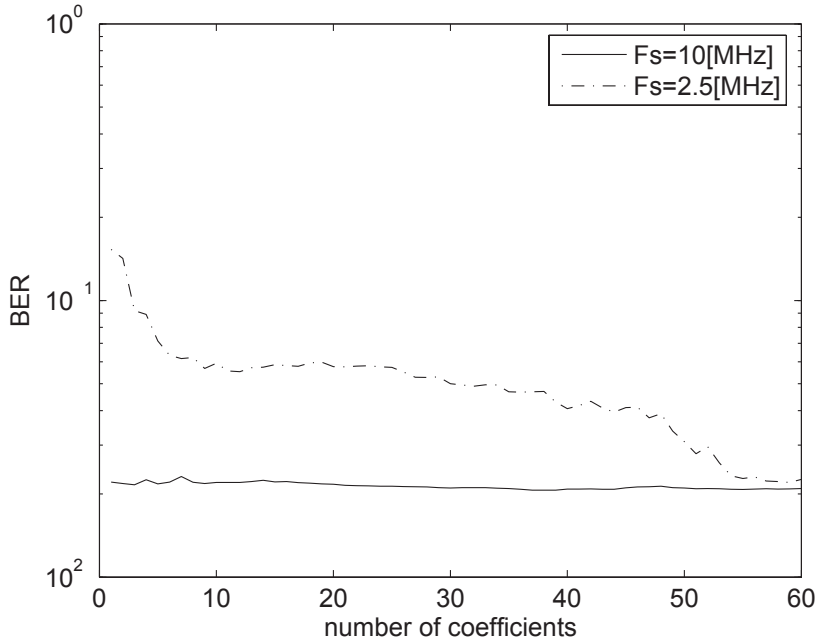

Figure 3.15: BER vs. the number of coefficients, SIR=-18[dB], SNR=6[dB] , resolution of ADC = 8[bits].

its own channel and also the outband noise that is not completely filtered is folded to the desired signal channel.

Figure 3.15 shows the BER versus the number of coefficients for Wiener filter when SIR=-18[dB] and SNR=6[dB]. When the sampling frequency is 10[MHz], it is possible to get good result with a small number of coefficients. When the sampling frequency is 2.5[MHz] a good performance of the BER can only be obtained when the number of coefficients is more than 55. Therefore, 10 is selected as the number of coefficient for f_s=10[MHz] and 55 is selected as the number coefficient for f_s=2.5[MHz] in this experiment.

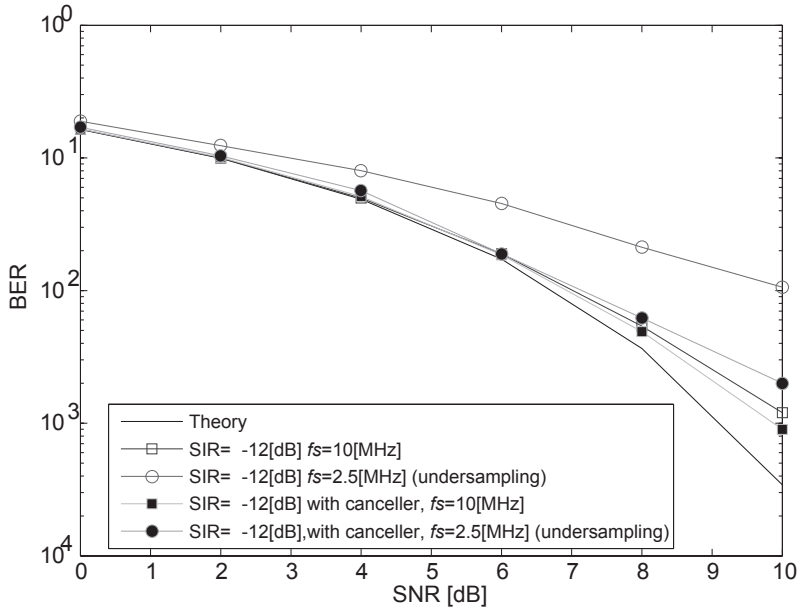

Figure 3.16: BER vs. SNR, SIR=-12[dB], resolution of ADC = 8[bits].

Figure 3.16 shows the BER performance versus SNR when the SIR=-12[dB]. The "canceller" in the figure indicates the result when ACI cancellation with Wiener filter is used. When the sampling frequency is set to 10[MHz], the performance degraded a little due to the ACI. The performance improved when the canceller is utilized in the system. The BER performance degraded for about 2[dB] as compared to f_s=10[MHz]

when the sampling frequency is set to 2.5[MHz] and undersampling is used. The result shows a great improvement of the BER performance when the canceller is utilized in the system.

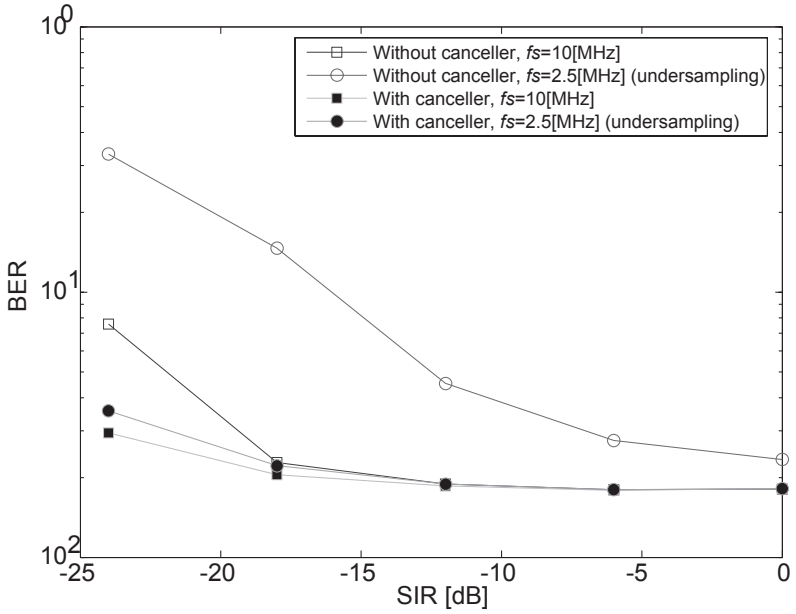

Figure 3.17: BER vs. SIR, SNR=6[dB], resolution of ADC = 8[bits].

Figure 3.17 shows the result of BER performance when the sampling frequency is 10[MHz] and 2.5[MHz]. For F_s=10[MHz], the performance starts degraded when the SIR is below -12[dB]. This is because side lobe of ACI interferes the desired signal and the performance improves by applying Wiener filter. When undersampling technique is applied by reducing the sampling frequency to 2.5[MHz], the performance degraded larger as the SIR increase. This is because other than the side lobe of the ACI, then remained main lobe of adjacent channel is down folded to the desired channel. When the Wiener filter is applied, the remained adjacent channel component is cancelled, and the performance improved. From the figure, it is concluded that the influence of the ACI can be reduced by about 20[dB] when BER=3×10^{-2}.

3.5 Conclusion

In this chapter, the ACI cancellation scheme for multi-channel reception with undersampling is proposed. In the proposed scheme, training sequence is required periodically to estimate the characteristics of interference signal. The interference signal is then cancelled from received signal through Wiener filter. From the experiment results, it has been shown that the proposed scheme can mitigate the influence from the adjacent channel. It has been also proven that the undersampling technique can be applied in this scheme. The proposed scheme enables multi-channel reception with relatively low resolution and sampling frequency of ADCs with the adaptive digital signal processing.

Though the experiment, it is shown that the proposed scheme can reduce the influence of the interference from adjacent channel by about 20[dB] when BER=3×10^{-2}, and it is proven that undersampling can achieve the same performance as that Nyquist sampling. The sampling frequency can be lowered from 10[MHz](in reference [10]) to 2.5[MHz] when undersampling is applied. Therefore, high speed handover over WLAN for VoIP can be achieved with the proposed scheme.

Comparison between Chapter 2 and Chapter 3

Both Chapter 2 and Chapter 3 discusses about a realization of high-speed handover for WLAN by using multi-channel reception concept. Chapter 2 proposes the method to solve the ACI problem due to the high dynamic range and out-of-band leakage from the adjacent channel. The proposed scheme in Chapter 2 requires multiple of high speed ADCs to prepare the filter bank for all channels. Also the low-IF receiver requires higher sampling frequency than the conventional architecture such as super-heterodyne. Thus, the ADCs in the low-IF receiver require higher power consumption than the conventional scheme.

Undersampling technique is employed in Chapter 3 in order to lower the required sampling frequency and power consumption of the ADC. The undersampling translates the high frequency bandpass signal to a near zero lowpass frequency. The sampling frequency requirement is based on the signal bandwidth rather than its highest frequency. Sampling at reduced rates eases many of the ADC requirements, and decreases power consumption, thus increasing battery lifetime, and the overall receiver size. The need for very high performance programmable devices is also reduced.

For instant, usually 4 channels are used to cover a large area in a WLAN system. In the case of Nyquist sampling, at least 40MHz sampling frequency of dual-channel ADCs are required in order to receive higher frequency channel. On the other hand, in the system that is described in Chapter 3, only 20MHz sampling frequency of dual-channel ADCs are required to receive any channel despite the channel frequency.

There are some demerits of utilizing undersampling. In order to utilize undersampling, any out of band signal or noise must be kept to minimum because they will fold down to the desired signal band. A BPF of very high Q is required to suppress the out of band signal. If the signal in the adjacent channel is much larger than the desired signal, the BPF cannot eliminate the signal completely due to the restriction

of the circuit size. The remaining adjacent channel signal components interferes the desired signal by folding down to the desired signal channel. The influence of aliasing effect in the undersampling is compensated in digital domain by using the adaptive digital signal processing. Thus, the requirements of the digital signal processing in Chapter 3 system are slightly higher than Chapter 2. The system in Chapter 2 only needs 10 coefficients filter, while the system in Chapter 3 needs approximately 50 coefficients filter to operate effectively.

The system in Chapter 3 is more sensitive to jitter and phase noise. Jitter and phase noise of the sample clock signal can seriously degrade undersampling performance. This effect can reduce by using a high-quality crystal oscillator with simple, direct connections to the ADC. Some ADCs are specifically characterized for undersampling applications, while others are designed only for baseband sampling.

Referring to the results in Section 3.4.3, the performance of the system with undersampling is slightly lower than the system with Nyquist sampling. The adaptive signal processing greatly improves the performance of the system with undersampling, however, it is still slightly lower than those with Nyquist sampling. Therefore, there are some trade-offs between the performance and the power consumption. The system in Chapter 2 can be applied for higher performance with higher power consumption applications while the system in Chapter 3 can be applied for lower power consumption with slightly lower performance applications.

Chapter 4

Direct Insertion/Cancellation method based Fractional Sample Rate Conversion for Software Defined Radio

In this chapter, a new fractional sample rate conversion (SRC) scheme based on a direct insertion/cancellation scheme is proposed. This scheme is suitable for signals that are sampled at a high sample rate and converted to a lower sample rate. The direct insertion/cancellation scheme may achieve low-complexity and lower power consumption as compared to the other SRC techniques. However, the direct insertion/cancellation technique suffers from large aliasing and distortion. The aliasing from an adjacent channel interferes the desired signal and degrades the performance. Therefore, a modified direct insertion/cancellation scheme is proposed in order to realize high performance resampling.

4.1 Introduction

Recently, cognitive radio (CR), which automatically changes its communication variables in response to network environment and user demands, has been introduced as the next step in radio systems' evolution. Due to the need of seamless communication for CR, a software defined radio (SDR) concept has received much attention

among researchers working in wireless communication. SDR is a technology that allows a single terminal to support various kinds of wireless systems and services such as mobile systems and wireless LANs by changing software to reconfigure the wireless terminal.

A variety of architectures have been proposed to realize the SDR [1–3,7,10,42]. In a direct conversion receiver (DCR), a desired signal is mixed directly to a baseband signal [7]. An RF sampling receiver scheme has been proposed recently to replace the DCR scheme. In the RF sampling receiver architecture, the received signal is processed directly at the analog domain and is sampled at a radio frequency (RF) [12, 16]. Channel selection and demodulation are carried out in the digital domain. These architectures achieve reduction of off-chip components and enable the realization of a one-chip receiver.

Since different communication standards are based on different master clock rates, it is mainly necessary to provide different clock rates. Since a signal processor should work at the minimum possible rate, SRC has to be implanted to a SDR/CR receiver in order to process various kinds of radio standards [3].

The most common structure for fractional SRC is a combination of an L-factor upsampler, an anti-aliasing filter, and an M-factor downsampler. The SRC by L/M-ratio is done by upsampling the input data with L and then downsampling it by M [23, 27]. However, this technique is not applicable in practice in some systems due to the possibly very high intermediate sample rate and also required large effort for the anti-aliasing filter. Implementation of fractional-SRC by using a cascaded-integrator comb (CIC) filter can reduce the effort as the impulse response of the reconstruction filter can be realized by the comb filter [24]. However, this technique still requires the high intermediate sample rate. Time-varying polyphase structure based fractional-SRC has been proposed to avoid the high intermediate frequency. The most commonly used implementation in this kind of structure is the Farrow

structure which is a combination of polynomial filtering and block processing [25]. Polyphase realization for the CIC filter is also proposed in order to avoid the high intermediate sample rate [27]. However, the polyphase structure based fractional-SRC requires multiple of fractional delay filters and a lot of multiplexers which increase the complexity and power consumption.

In this chapter, a new SRC technique is proposed based on the direct insertion/cancellation scheme. This technique is also called non-interpolative resampling technique [28, 29]. This technique is suitable for application in the RF sampling receiver which samples data with a high oversampling ratio (OSR). In non-interpolative resampling technique, new samples are inserted to the data stream to increase the rate to a desired sample rate, or an amount of samples is deleted from a data stream to decrease the sample rate. In the direct insertion scheme, α samples are inserted in every block of N samples to increase the rate by $(N + \alpha)/N$. In the direct cancellation scheme, α samples are deleted in every block of N samples to reduce the rate by $(N - \alpha)/N$. This scheme realizes small chip size with low cost and power consumption. However this scheme suffers from large distortion as compared to the other SRC techniques. The aliasing from an adjacent channel interferes the desired signal and degrades the performance. For simplicity, this thesis is focusing at $\alpha = 1$ as $(N + 1)/N$ and $(N - 1)/N$ generates nearer aliasing interval as compared to the other rates. The aliasing that is nearer to the desired signal interferes the desired signal more than those that are far away from the desired signal.

In order to reduce the distortion noise that was imposed after the insertion/cancellation a new technique is introduced. The distortion noise or aliasing can be reduced by applying multiple sets of inserters/deleters. This technique reduces the required complexity of an anti-aliasing filter structure, and improves the performance of a direct insertion/cancellation based SRC system.

In this thesis, a 2.4GHz signal is used as the received signal example. The 2.4GHz

signal is sampled at the RF frequency at the downconversion sampler. The discrete signal is then decimated 8 times to 300MHz sample rate before converted to the digital signal. The signal has to downsample to 40MHz for support of IEEE802.11n [46]. Therefore, the sample rate of the ADC output signal has to be converted to a multiple of 40MHz that are 360 and 240MHz.

4.2 Conventional Direct Insertion/Cancellation SRC Method

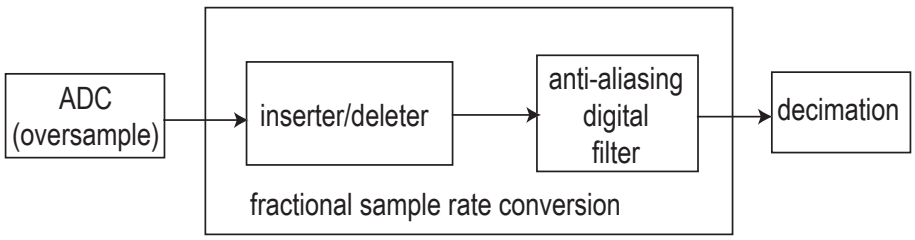

Figure 4.1: Direct insertion/cancellation based fractional-SRC.

In the non-interpolative resampling technique, new samples are inserted to the data stream to increase the rate to a desired data rate, or an amount of samples is deleted from a data stream to decrease the data rate. The common method to insert new samples in this technique is to insert a new sample after every block of N samples to increase the rate by the ratio $(N+1)/N$. The inserted samples can simply be zeros or a repeat of last value. In this thesis, the repetition of the last value is used as the inserted sample. Similarly, a data is deleted or skipped every N samples to decrease data rate by the ratio $(N-1)/N$. The insertion or cancellation step is followed by filtering process by the anti-aliasing filter. The images that have been generated after insertion/cancellation process are removed by the anti-aliasing filter.

High oversampling ratio (OSR) is required in this technique. Figure 4.1 shows the conventional periodic direct insertion/cancellation scheme. The inserter/deleter

block in the figure performs direct insertion/cancellation process. This scheme realizes smaller chip size and lower power consumption as compared to the other techniques. However this scheme suffers from large distortion as compared to an interpolative technique.

In the direct insertion method, where a new sample is inserted by repeating the R-th sample in every $N+1$ samples period to increase the data rate by $(N+1)/N$, the output signal is given by

$$y(kT_2) = x\left(\left(\left\lfloor \frac{kN+R}{N+1} \right\rfloor\right) T_1\right), \tag{4.1}$$

where $x(k)$ in the k-th sample of the input sequence, T_1 is the input sampling period, and T_2 is the output sampling period. In the direct cancellation method, every R-th sample in every N samples period of the input signal sequence is deleted to reduce the data rate by $(N-1)/N$. The output signal is given by

$$y(kT_2) = x\left(\left(\left\lceil \frac{kN-R+1}{N-1} \right\rceil\right) T_1\right). \tag{4.2}$$

For example, a data is inserted every 5 samples to convert f_{s1} =300MHz sample rate to f_{s2} =360MHz. The timing of the 5th sample of 300MHz signal is the same timing with the 6th sample of 360MHz signal. Therefore, the 6th sample of 360MHz output signal of the data has to be corrected to fit the 5th sample of 300MHz input sample. The input signal sequence,

$$\mathbf{x} = [x_0, x_1, x_2, x_3, x_4, \cdots], \tag{4.3}$$

is converted to the output signal,

$$\mathbf{y} = [x_0, x_1, x_2, x_3, x_4, x_4 \cdots]. \tag{4.4}$$

In this example, the samples $[x_{5p-1}]$ are repeated, where each sample is repeated every p-th insertion period.

As a sample rate reduction example, a data is deleted every 5 samples to convert f_{s1} =300MHz sample rate to f_{s2} =240MHz. If the input signal matrix is the same with (3), the output signal matrix is

$$\mathbf{y} = [x_0, x_1, x_2, x_3, x_5 \cdots]\,. \tag{4.5}$$

In this example, the samples $[x_{5p-1}]$ are skipped, where each sample is skipped every p-th cancellation period.

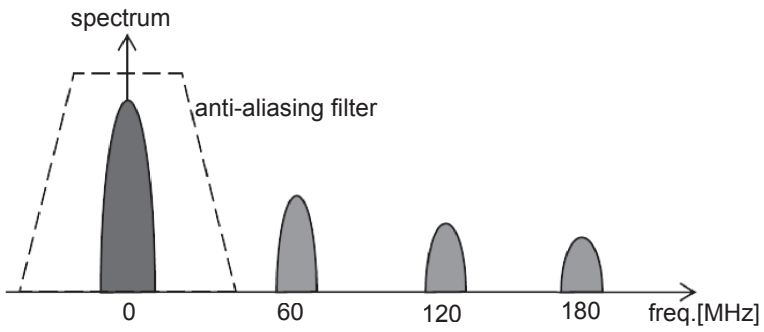

Figure 4.2: Aliasing due to the Direct insertion/cancellation method.

The output of the inserter/deleter also produces images every $f = 1/NT_1$. For example, in Fig. 4.2, spectral images are produced every 60MHz when $f_{s1} = 300$MHz sample rate signal is converted to f_{s2} =360MHz. In order to avoid further distortion and interference, the images must be attenuated. An attenuation of 50[dB] is achieved with an equiripple finite impulse response (FIR) low pass filter (LPF) with approximately 36 coefficients.

4.3 Proposed Method

In order to reduce the distortion noise that was generated after the insertion/cancellation a new technique has to be introduced. The distortion noise or aliasing can be reduced by applying multiple sets of inserters/deleters. Figure 4.3 shows the modified direct insertion/cancellation method structure with M sets of inserters/deleters.

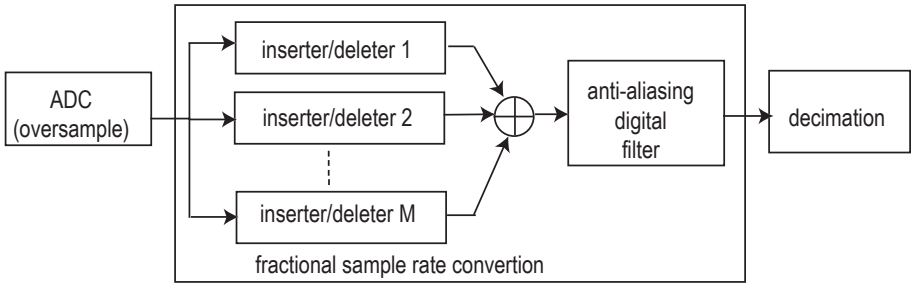

Figure 4.3: Proposed method.

Each inserter/deleter performs periodic insertion/cancellation with different insertion/cancellation phase.

In the case of Msets of inserters, the output of the inserter/deleter block is the summation of output of all inserters. This is expressed by

$$y(kT_2) = \sum_{m=1}^{M} x\left(\left\lfloor \frac{kN + R_m}{N+1} \right\rfloor T_1\right), \tag{4.6}$$

where R_m is the insertion phase of inserter m. The insertion phase of each inserter is set to be maximally spaced to each other. This can be done by

$$R_m = \left\lfloor \frac{m-1}{M}(N+1) + \varphi \right\rfloor, \tag{4.7}$$

$$\varphi < \frac{N+1}{M}. \tag{4.8}$$

In the case of Msets of deleters, the output of the inserter/deleter block is the summation of output of all deleters. This is expressed by

$$y(kT_2) = \sum_{m=1}^{M} x\left(\left\lceil \frac{kN - R_m - 1}{N-1} \right\rceil T_1\right), \tag{4.9}$$

where R_m is the deletion phase of inserter m. The deletion phase of each inserter is set to be maximally spaced to each other. This can be done by

$$R_m = \left\lfloor \frac{m-1}{M}(N-1) + \varphi \right\rfloor, \tag{4.10}$$

$$\varphi < \frac{N-1}{M}. \tag{4.11}$$

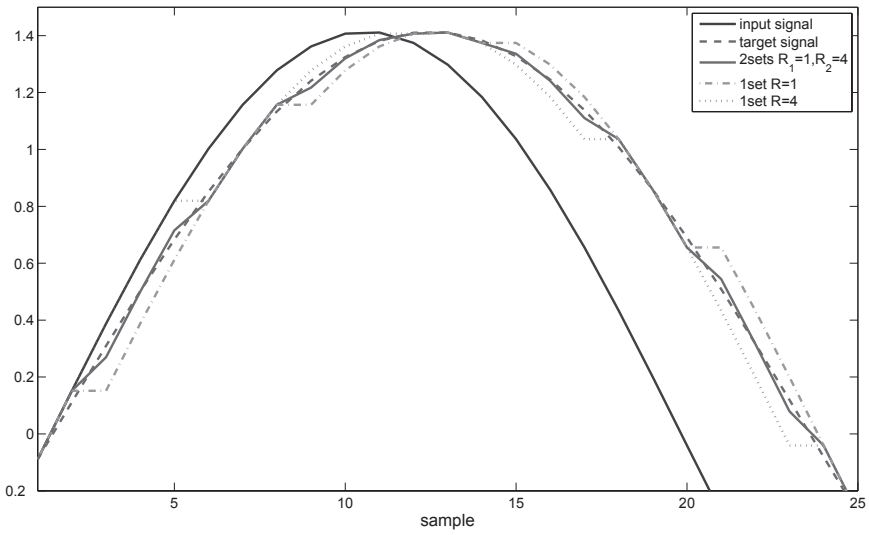

Figure 4.4: Output of 6/5-ratio SRC.

For instance, sample rate of a sinusoidal signal is converted with 6/5-ratio SRC as shown in Fig. 4.4. In the 6/5-ratio 2-sets inserters SRC, a sample is inserted after every 2nd and 5th sample of inserter 1 and inserter 2 ($N = 5, M = 2, R_1 = 1, R_2 = 4$). The output signal sequence is

$$\begin{aligned} \mathbf{y} &= [x_0, x_1, x_1, x_2, x_3, x_4, x_5, x_6, x_6, x_7, x_8, x_9, \cdots] \\ &\quad + [x_0, x_1, x_2, x_3, x_4, x_4, x_5, x_6, x_7, x_8, x_9, x_9, \cdots] \qquad (4.12) \\ &= [2x_0, 2x_1, x_1 + x_2, x_2 + x_3, x_3 + x_4, 2x_4, 2x_5, 2x_6, x_6 + x_7, x_7 + x_8, x_8 + x_9, 2x_9, \cdots]. \end{aligned}$$

In the case of 6-sets inserters for the same conversion rate ($N = 5, M = 6, R_m =$

$m-1$), the output sequence of the inserter block is

$$\begin{aligned}
\mathbf{y} &= [x_0, x_0, x_1, x_2, x_3, x_4, x_5, x_5, x_6, x_7, x_8, x_9, \cdots] \\
&\quad + [x_0, x_1, x_1, x_2, x_3, x_4, x_5, x_6, x_6, x_7, x_8, x_9, \cdots] \\
&\quad + [x_0, x_1, x_2, x_2, x_3, x_4, x_5, x_6, x_7, x_7, x_8, x_9, \cdots] \\
&\quad + [x_0, x_1, x_2, x_3, x_3, x_4, x_5, x_6, x_7, x_8, x_8, x_9, \cdots] \\
&\quad + [x_0, x_1, x_2, x_3, x_4, x_4, x_5, x_6, x_7, x_8, x_9, x_9, \cdots] \\
&\quad + [x_0, x_1, x_2, x_3, x_4, x_5, x_5, x_6, x_7, x_8, x_9, x_{10}, \cdots] \qquad (4.13) \\
&= [6x_0, x_0 + 5x_1, 2x_1 + 4x_2, 3x_2 + 3x_3, 4x_3 + 2x_4, 6x_4, 6x_5, \\
&\quad x_5 + 5x_6, 2x_6 + 4x_7, 3x_7 + 3x_8, 4_8 + 2x_9, 5x_9 + x_{10}, \cdots].
\end{aligned}$$

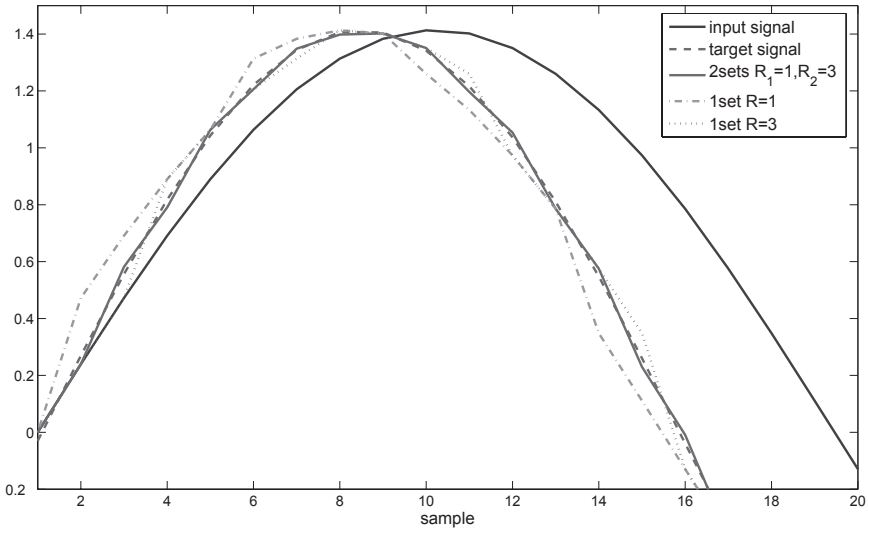

Figure 4.5: Output of 4/5-ratio SRC.

For sample rate reduction example, the sinusoidal signal is converted with 4/5-ratio SRC as shown in Fig. 4.5. In the 4/5-ratio 2-set deleter SRC, a sample is deleted every 2nd and 5th sample of deleter 1 and deleter 2 respectively ($N = 5, M = 2, R_1 =$

$1, R_2 = 4$). The output signal sequence is

$$\begin{aligned}\mathbf{y} &= [x_0, x_2, x_3, x_4, x_5, x_7, x_8, x_9, \cdots] \\ &\quad + [x_0, x_1, x_2, x_3, x_5, x_6, x_7, x_8, \cdots] \\ &= [2x_0, x_1 + x_2, x_2 + x_3, x_3 + x_4, 2x_5, x_6 + x_7, x_7 + x_8, x_8 + x_9, \cdots].\end{aligned} \tag{4.14}$$

In the case of 4-sets deleters for the same conversion rate ($N = 5, M = 4, R_m = m$), the output sequence of the inserter block is

$$\begin{aligned}\mathbf{y} &= [x_0, x_2, x_3, x_4, x_5, x_7, x_8, x_9, \cdots] \\ &\quad + [x_0, x_1, x_3, x_4, x_5, x_6, x_8, x_9, \cdots] \\ &\quad + [x_0, x_1, x_2, x_4, x_5, x_6, x_7, x_9, \cdots] \\ &\quad + [x_0, x_1, x_2, x_3, x_5, x_6, x_7, x_8, \cdots] \\ &= [4x_0, 3x_1 + x_2, 2x_2 + 2x_3, x_3 + 3x_4, 4x_5, 3x_6 + x_7, 2x_7 + 2x_8, x_8 + 3x_9, \cdots].\end{aligned} \tag{4.15}$$

This technique eliminates the lower frequency aliasing and reduces overall distortion from the inserter/deleter block outputs. This will relax the requirement and complexity of the anti-aliasing filter. The anti-aliasing for the proposed scheme can be realized with a simple sinc filter or an averaging filter with the small number of coefficients. The multiple sets of inserters/deleters block structure can be realized without any multiplier. The more sets of inserters/deleters will increase the number of adders that are used for averaging the inserter/deleter outputs, without increasing the number of multipliers. The SRC with more number of inserters/deleters relaxes the requirement of anti-aliasing filter for the same performance.

4.4 Analytical Calculation for Sinusoidal Signal

In this section, analytical calculation of distortion noise in the conventional periodic direct insertion and the proposed method is discussed. Sinusoidal signal is used as the

input signal. The distortion after the insertion/cancellation steps can be calculated by phase difference between the converted signal and the target signal. The target signal is a perfect sinusoidal signal with the amplitude, A, and the frequency, f, and is represented as,

$$S_{ref} = A\sin(2\pi ft), \tag{4.16}$$

while the converted signal is represented as,

$$S_{out} = A\sin(2\pi f(t+\delta)), \tag{4.17}$$

where δ is the phase difference. The amplitude difference due to the phase difference can be calculated by subtracting (4.16) from (4.17),

$$\begin{aligned}\Delta V(t) &= A\sin(2\pi f(t+\delta)) - A\sin(2\pi ft) \\ &= A(\sin(2\pi ft)\cos(2\pi f\delta) \\ &+ \cos(2\pi ft)\sin(2\pi f\delta)) - A\sin(2\pi ft).\end{aligned} \tag{4.18}$$

The distortion due to the phase difference is expressed as mean squared error (MSE). The analytical MSE can be calculated by averaging the square of (4.18)

$$\begin{aligned}D &= \overline{(\Delta V(t))^2} \\ &= \frac{A^2}{2}\{\cos^2(2\pi f\delta) - 2\cos(2\pi f\delta) + \sin^2(2\pi f\delta) + 1\} \\ &= A^2\left\{1 - \cos(2\pi f\delta)\right\}.\end{aligned} \tag{4.19}$$

After the insertion step, there are $N+1$ samples in an insertion sample period. Thus, there are $N+1$ variations of δ in an insertion period and the δ values are repeated in every period. Figure 4.6 shows the phase difference between the converted 300MHz to 360MHz sample rate signal and the target signal which is sampled with 360MHz. The 'n' in the figure refers to the n-th sample of the p-th insertion period.

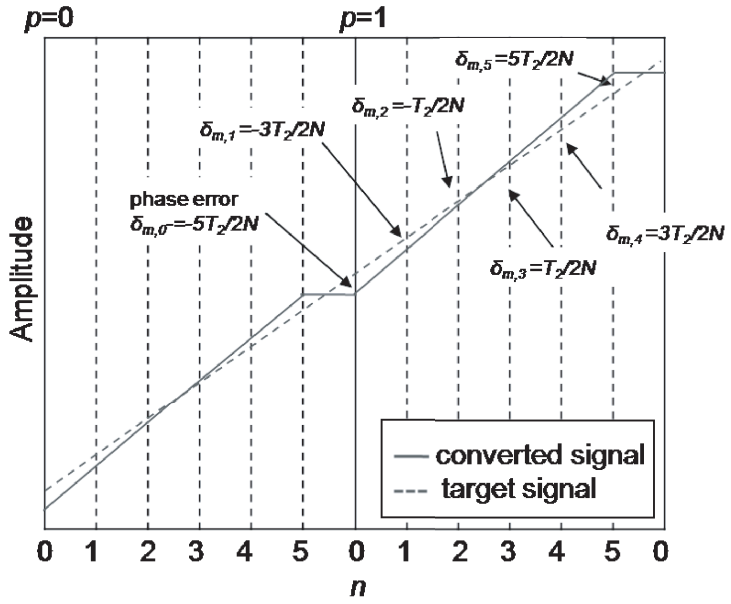

Figure 4.6: Phase difference between the converted signal and the target signal, insertion period N=5, insertion phase R=5.

The phase differences in an insertion period for inserter m are expressed as

$$\delta_{m,n} = \frac{2n - N}{2N} T_2, \ n = 0, 2, \cdots N. \tag{4.20}$$

Thus, the MSE after the insertion step for a single branch inserter can be derived by calculating the average distortion due to every phase difference. This is expressed as,

$$D_{1,up} = \frac{A^2}{N+1} \sum_{n=1}^{N+1} \{1 - \cos(2\pi f \delta_{1,n})\}. \tag{4.21}$$

In the direct cancellation method, there would be $N-1$ variation of δ in an insertion period and the δ values are repeated in every period since there are $N-1$ samples in the cancellation period after the cancellation step. Thus, the MSE after the cancellation step is expressed as,

$$D_{1,down} = \frac{A^2}{N-1} \sum_{n=1}^{N-1} \{1 - \cos(2\pi f \delta_{1,n})\}. \tag{4.22}$$

The phase differences in an cancellation period for deleter m are expressed as

$$\delta_{m,n} = \frac{N - 2n}{2N} T_2, \ n = 0, 2, \cdots N-2. \tag{4.23}$$

In the case of 2 sets of inserters/deleters, the output signal is the average of 2 signals with different phase error. The amplitude difference is calculated by

$$\Delta V_{2,n}(t) = \frac{A}{2}\sin(2\pi f(t+\delta_{1,n})) + \frac{A}{2}\sin(2\pi f(t+\delta_{2,n})) - A\sin(2\pi ft), \tag{4.24}$$

where $\delta_{1,n}$ and $\delta_{2,n}$ are phase differences for inserter/deleter 1 and inserter/deleter 2 respectively. The distortion at each insertion/cancellation phase calculated by,

$$\begin{aligned} D_{2,n} &= \overline{(\Delta V_{2,n}(t))^2} \\ &= \frac{A^2}{4}\{\cos(2\pi f(\delta_{1,n}-\delta_{2,n})) \\ &-2\cos(2\pi f\delta_{1,n}) - 2\cos(2\pi f\delta_{2,n}) + 3\}. \end{aligned} \tag{4.25}$$

The MSE in an insertion period for 2 sets of inserters is expressed by

$$\begin{aligned} D_{2,up} = \frac{A^2}{4(N+1)}\sum_{n=1}^{N+1}\{&\cos(2\pi f(\delta_{1,n}-\delta_{2,n})) \\ &-2\cos(2\pi f\delta_{1,n}) - 2\cos(2\pi f\delta_{2,n}) + 3\}. \end{aligned} \tag{4.26}$$

The MSE in a cancellation period for 2 sets of deleters is expressed as,

$$\begin{aligned} D_{2,down} = \frac{A^2}{4(N-1)}\sum_{n=1}^{N-1}\{&\cos(2\pi f(\delta_{1,n}-\delta_{2,n})) \\ &-2\cos(2\pi f\delta_{1,n}) - 2\cos(2\pi f\delta_{2,n}) + 3\}. \end{aligned} \tag{4.27}$$

In the case of M sets of inserters/deleters, the amplitude difference can be calculated by

$$\Delta V_{M,n}(t) = \frac{A}{M}\sum_{m=1}^{M}\sin(2\pi f(t+\delta_{m,n})) - A\sin(2\pi ft). \tag{4.28}$$

The distortion at each insertion/cancellation phase is calculated by,

$$\begin{aligned} D_{M,n} &= \overline{(\Delta V_{M,n}(t))^2} \\ &= \frac{A^2}{M^2}\{\sum_{m_1=1}^{M-1}\sum_{m_2=m_1}^{M}\cos(2\pi f(\delta_{m_1,n}-\delta_{m_2,n})) \\ &-M\sum_{m=1}^{M}\cos(2\pi f\delta_{m,n}) + \frac{1}{2}(M+M^2)\}. \end{aligned} \tag{4.29}$$

The MSE in an insertion period for M sets of inserters is derived by averaging (4.29) with $N+1$ samples. This is expressed as,

$$D_{M,up} = \frac{A^2}{M^2(N+1)} \sum_{n=1}^{N+1} \{ \frac{1}{2}(M + M^2) + \sum_{m_1=1}^{M-1} \sum_{m_2=m_1}^{M} \cos(2\pi f(\delta_{m_1,n} - \delta_{m_2,n})) - M \sum_{m=1}^{M} \cos(2\pi f \delta_{m,n}) \}. \quad (4.30)$$

The MSE in a cancellation period for M sets of deleters is derived by averaging (4.29) with $N-1$ samples. This is expressed as,

$$D_{M,down} = \frac{A^2}{M^2(N-1)} \sum_{n=1}^{N-1} \{ \frac{1}{2}(M + M^2) + \sum_{m_1=1}^{M-1} \sum_{m_2=m_1}^{M} \cos(2\pi f(\delta_{m_1,n} - \delta_{m_2,n})) - M \sum_{m=1}^{M} \cos(2\pi f \delta_{m,n}) \}. \quad (4.31)$$

4.5 Numerical Results

4.5.1 Analysis and Simulation with Sinusoidal Signal

Table 4.1: Simulation conditions for sinusoidal signal.

	insertion	cancellation
amplitude	$\sqrt{2}$	$\sqrt{2}$
input sample rate, f_{s1}	300MHz	300MHz
output sample rate, f_{s2}	360MHz	240MHz
conversion rate	6/5	4/5
target signal sample rate, f_{ref}	360MHz	240MHz

The mean square of the distortion in the proposed method without an anti-aliasing filter is investigated by analytical calculation and computer simulation. In the simulation, the MSE is computed by calculating the difference between the converted signal and the direct sampled signal as the target signal. The simulation conditions for the sinusoidal signal are shown in Table 4.1 and the simulation process is shown

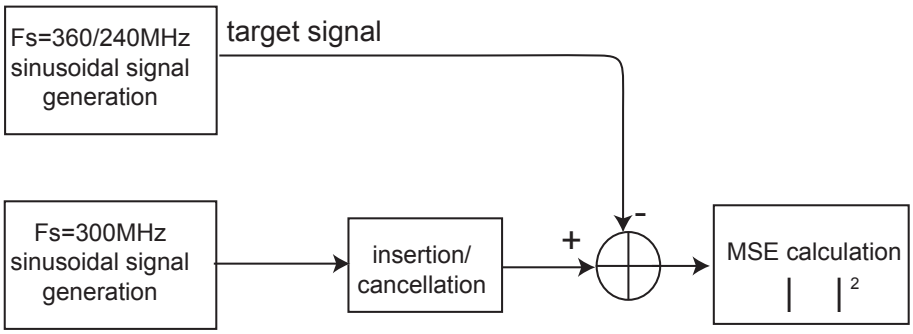

Figure 4.7: MSE simulation model for sinusoidal signal.

in Fig. 4.7 . The simulation results are compared to the analytical calculation results in Section 5.

The analytical MSE results and simulated MSE results when the sample rate is converted from 300MHz to 360MHz are shown in Fig. 4.8. The results show that the simulation results are matching the analytical calculation that are calculated using (4.21) and (4.30). The results show that the direct insertion method requires relatively high OSR. The OSR requirement is reduced by implying multiple sets of inserters.

The MSE results versus the number of sets are shown in Fig. 4.9. The results show that the MSE is lower with more sets of inserters/deleters. The results prove that the distortion noise due to the image caused by the insertion step can be reduced by implying multiple sets of inserters. In the 6/5 ($N = 5$) ratio conversion system, $6(N+1)$ sets of inserters achieve the best performance in the system. This is because in the insertion method, 1 sample is inserted to N samples in 1 insertion period in order to change the rate with $(N + 1)/N$. As the result, there are $N + 1$ samples in 1 insertion period after the insertion step. Therefore, the maximum number of inserters is $N + 1$ in the $(N + 1)/N$ SRC system.

The analytical MSE results and the simulation results when the sample rate is decreased from 300MHz to 240MHz is shown in Fig. 4.10 and Fig. 4.11. The simula-

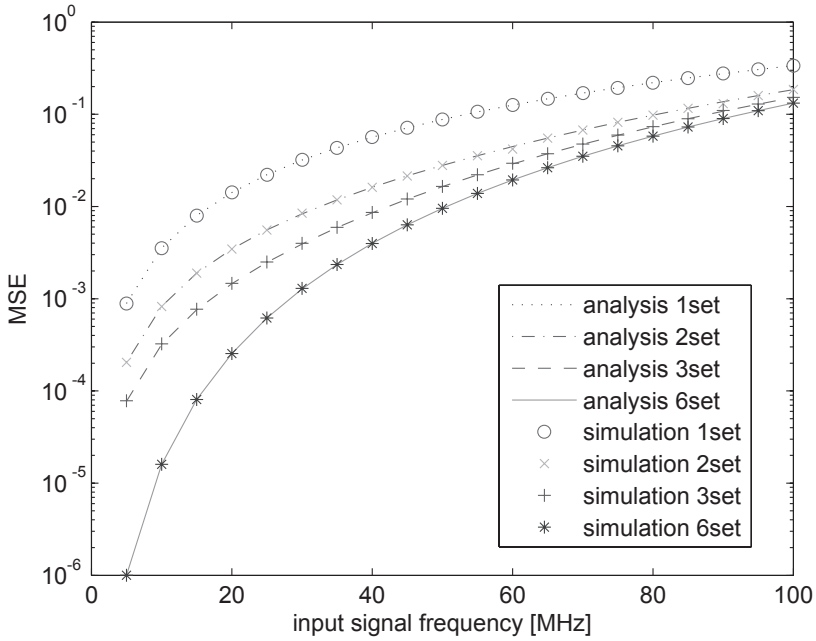

Figure 4.8: MSE results vs. input signal frequency, sample rate 300MHz → 360MHz.

tion results are matching the analytical results calculated by using (4.22) and (4.31). Similarly, better performance is obtained with higher OSR. The OSR requirement is reduced by implying multiple number of deleters. It is proven that the distortion noise is also reduced by using multiple sets of deleters in the direct cancellation method. In the direct cancellation method, 1 sample is deleted from N samples in one deletion period to change the sample rate of $(N-1)/N$. Therefore, the maximum number of deleters that give the best performance is $N-1$. The maximum number of deleters for the 4/5 SRC system is 4 sets of deleters.

Figure 4.12 shows the signal spectrum after direct insertion step in the 6/5-ratio SRC system. The aliasing due to the sample insertion is generated every 60MHz if only 1 inserter is used. The attenuation of 50[dB] is achieved with an equiripple FIR LPF with approximately 36 coefficients. The image components are reduced and shifted to the high frequency by adding more set of inserters. This relaxes the

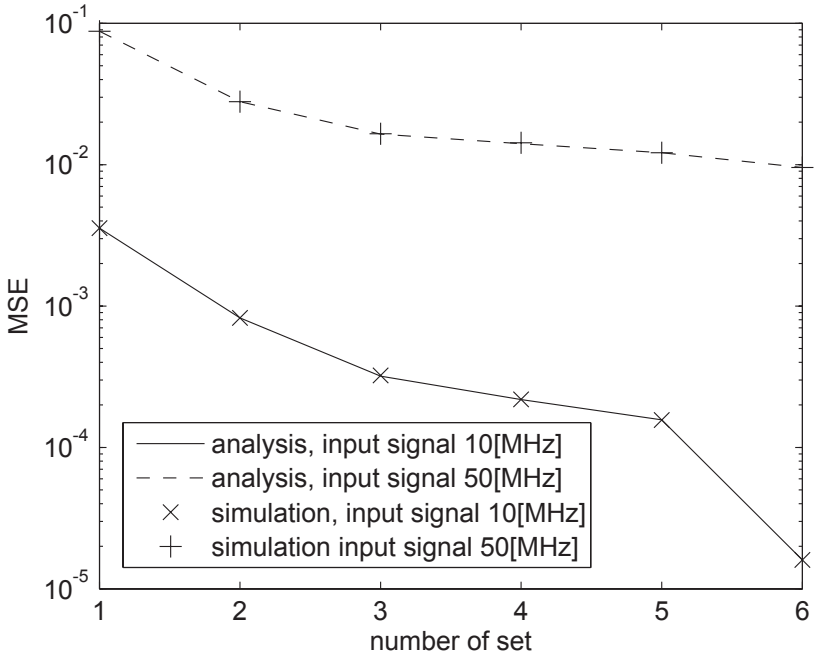

Figure 4.9: MSE results vs. number of set, sample rate 300MHz $\rightarrow$ 360MHz.

requirement and complexity of the anti-aliasing filter and improves the performance of the fractional-SRC system. The SRC with 2 sets of inserters eliminates the aliasing at 60MHz and the remaining aliasing at 120MHz can be suppressed to 50[dB] with only 8 taps of the same type of LPF. When the maximum sets of inserters are used, the generated aliasing is lower than 50[dB]. In this case, the SRC system can be realized without an anti-aliasing filter or only with a simple averaging filter.

There is some tradeoff between the complexity of inserters/deleters and the complexity of anti-aliasing. The more number of sets of inserters/deleters increases the number of adders that are used for averaging the inserters/deleters output. This will slightly increase the complexity of the SRC. The MSE and BER results show that there are significant improvements with only 2 sets of inserters/deleters. $N + 1$ sets of inserters has to be employed to minimize the distortion and maximize the performance. The number of deleters should be $N - 1$ to achieve the minimum distortion.

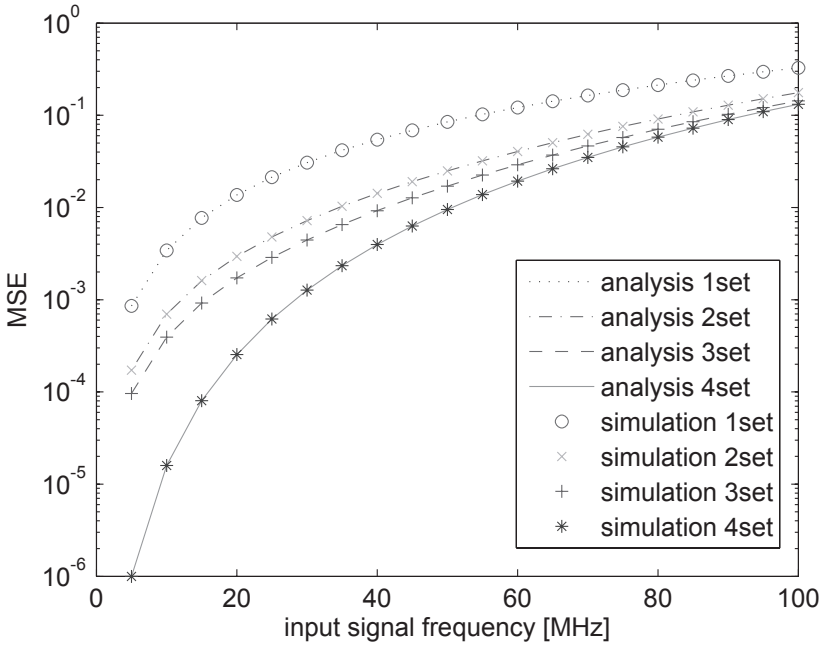

Figure 4.10: MSE results vs. input signal frequency, sample rate 300MHz $\rightarrow$ 240MHz.

Implementation with the maximum number of inserters/deleters may be difficult to realize if N is very large, as a large number of inserters/deleters have to be employed in the system. Therefore, the number of inserters/deleters has to be optimized to achieve good performance with low complexity implementation.

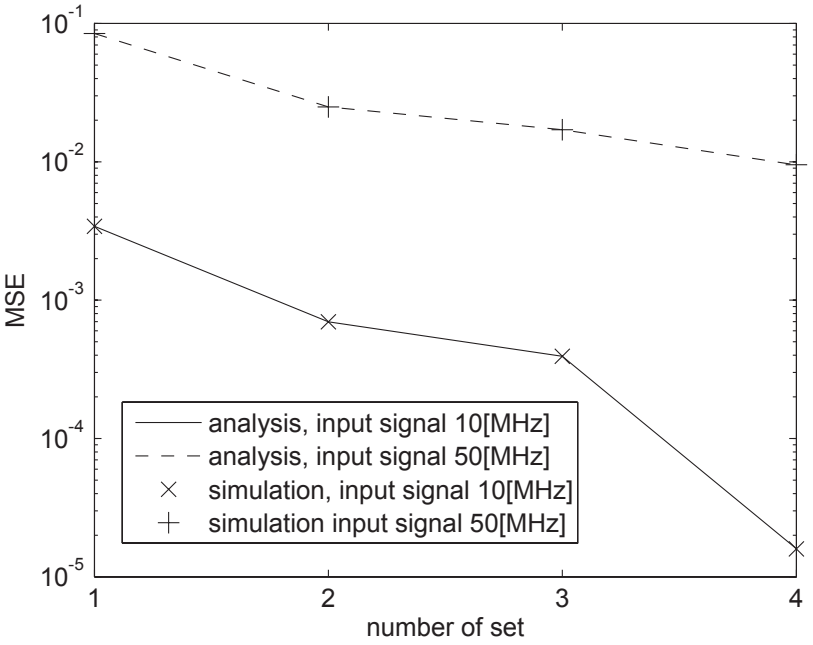

Figure 4.11: MSE results vs. number of set, sample rate 300MHz → 240MHz.

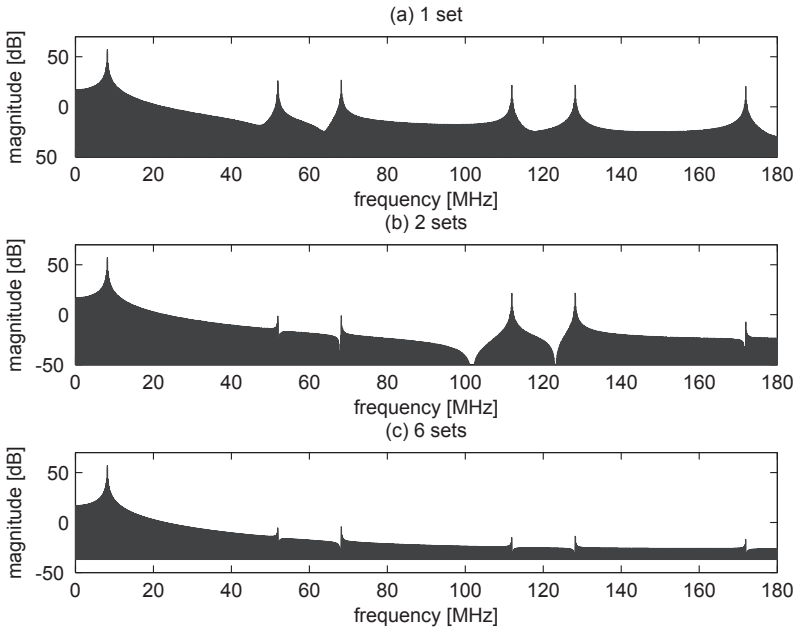

Figure 4.12: Power spectrum of 8.125MHz sinusoidal signal, sample rate 300MHz → 360MHz.

4.5.2 Implementation Example

General Pulse Waveform

Table 4.2: Simulation conditions for general pulse waveform signal.

modulation scheme	QPSK
bandwidth	20MHz
pulse shaping filter	raised cosine filter
rolloff	0.5
sample rate	300 → 360MHz

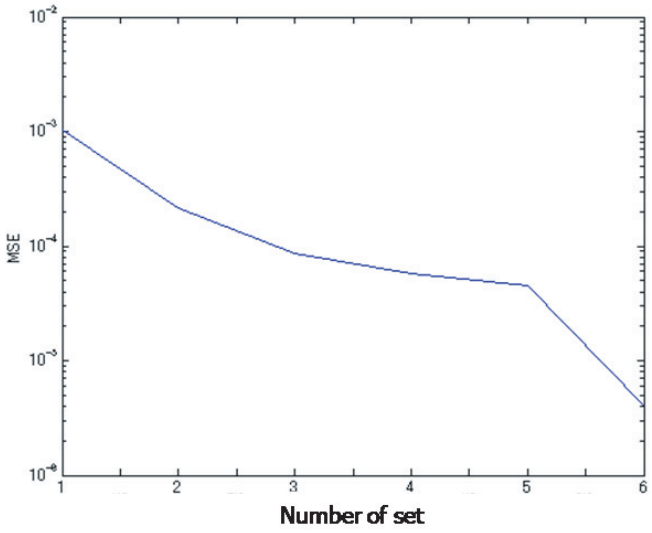

Figure 4.13: Pulse waveform: simulation results: MSE results vs. number of set, sample rate 300MHz → 360MHz.

In this section, the proposed scheme is simulated with a general pulse waveform. A random binary number is used as an information source and the information is modulated with QPSK. A raised cosine filter with a rolloff factor 0.5 is used for the pulse shaping. The data rate is set to 20MHz. The sample rate of the waveform is converted from 300MHz to 360MHz. The simulation conditions for SRC with the pulse waveform are shown in Table 4.2.

The output of the inserter is compared to the target signal for MSE calculation.

Figure 4.13 shows simulation MSE results for the pulse waveform. The MSE result for the pulse waveform is slightly lower than the 10MHz sinusoidal waveform results. The output of the inserter block is filtered by a 9-taps averaging filter for the anti-aliasing filtering. The output of the filter is downsampled to the symbol rate before demodulation for BER calculation. The BER result for the pulse waveform is shown in the Fig. 4.14. The BER performance is degraded for about 1[dB] when the conventional direct insertion SRC is used. The results show the improvements when 2 sets and 6 sets of inserters are used.

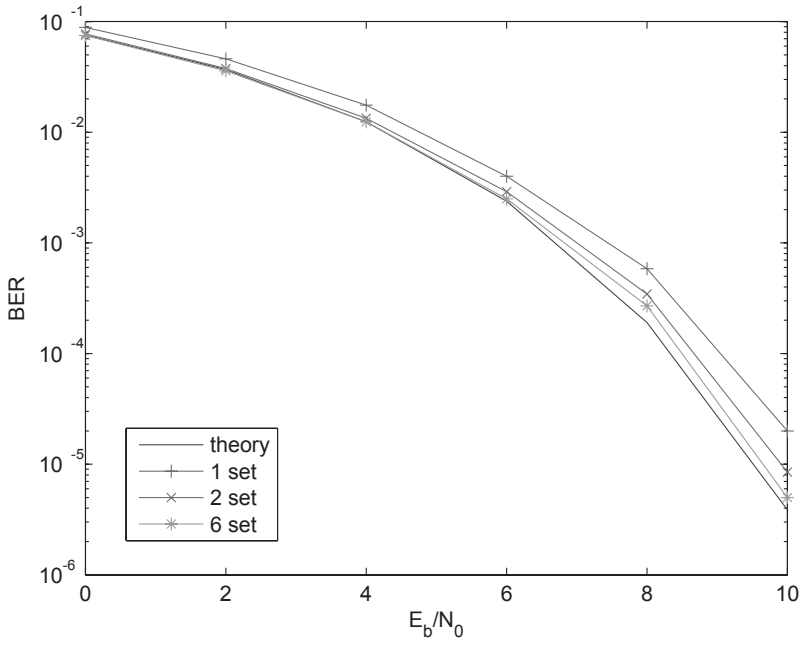

Figure 4.14: Pulse waveform: simulation results: BER results vs. E_b/N_0, sample rate 300MHz $\rightarrow$ 360MHz.

OFDM signal

In this section, the proposed SRC scheme implementation example for WLAN standard IEEE802.11g reception is discussed [40]. For this case, an OFDM (orthogonal frequency division multiplexing) signal with the carrier frequency 2400MHz and

bandwidth 16.25MHz is used as the received signal. The signal is received with the RF-sampling receiver and downconverted to the baseband. The signal is sampled with 300MHz ADC which is 1/8 of the carrier frequency. The sample rate of the signal is then converted to 360MHz with fractional SRC before it is downsampled to 40MHz as the target sample rate. Then the signal is decimated to 20MHz sample rate before it is demodulated.

Table 4.3: Simulation conditions for OFDM signal

modulation scheme	QPSK-OFDM 16QAM-OFDM
bandwidth	16.25MHz
adjacent channel center frequency after downconversion	60MHz

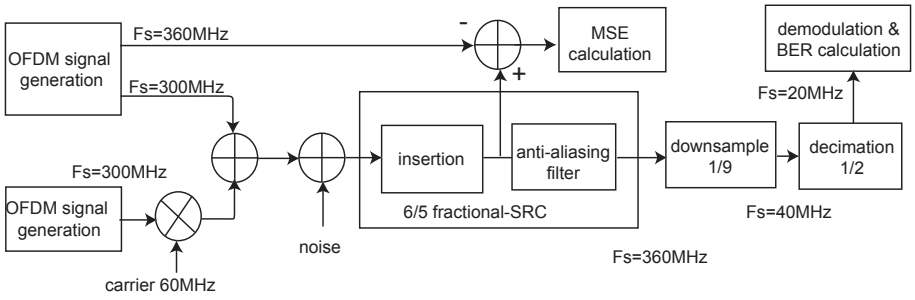

Figure 4.15: Simulation model for OFDM signal

The simulation conditions for OFDM signal are shown in Table 4.3 and the simulation process is shown in Fig. 4.15. In the simulation, a 300MHz baseband OFDM signal is used as the signal source. The 300MHz sample rate OFDM signal is converted to 360MHz sample rate by using the conventional and proposed direct insertion method. The output of the inserter block is compared to a generated 360MHz sample rate baseband OFDM signal for MSE calculation. The output of the inserter block is filtered by a 9-taps averaging filter as the anti-aliasing filter before the sample rate is downsampled to 40MHz. Then, the signal is decimated to 20MHz sample rate and is demodulated for bit error rate (BER) simulation. A 60MHz center frequency OFDM

signal is used as an interference signal for BER performance with adjacent channel interference (ACI) simulation.

Table 4.4: Simulation MSE results for OFDM

number of set	MSE
1	6.2×10^{-4}
2	1.3×10^{-4}
6	9.4×10^{-7}

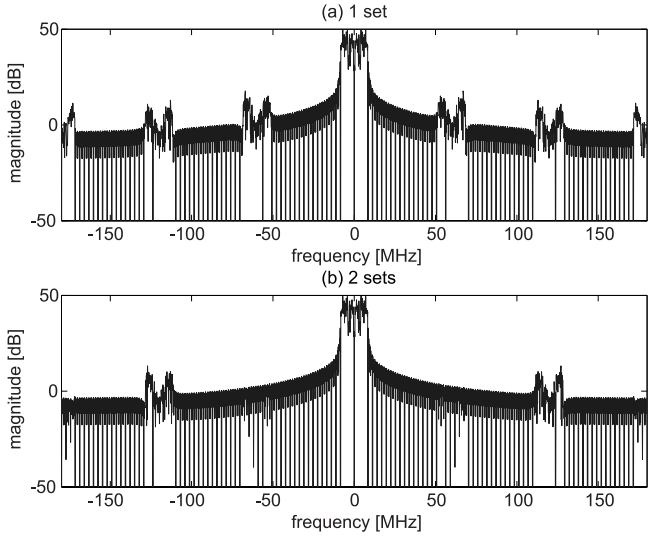

Figure 4.16: Power spectrum of OFDM signal, sample rate 300MHz → 360MHz.

Table 4.4 shows the MSE results for 1 set, 2 sets, and 6 sets of inserters when 300MHz sample rate signal is converted to 360MHz sample rate. The MSE of the signal that is converted with the conventional direct insertion is 6.2×10^{-4}. The MSE is reduced to 1.3×10^{-4} when 2 sets of inserters are used and is reduced to 9.4×10^{-7} when 6 sets of inserters are used. Figure 4.16 shows the power spectrum results. The distortion spectrum is reduced and shifted to the higher frequency when more sets of inserters are used in the system.

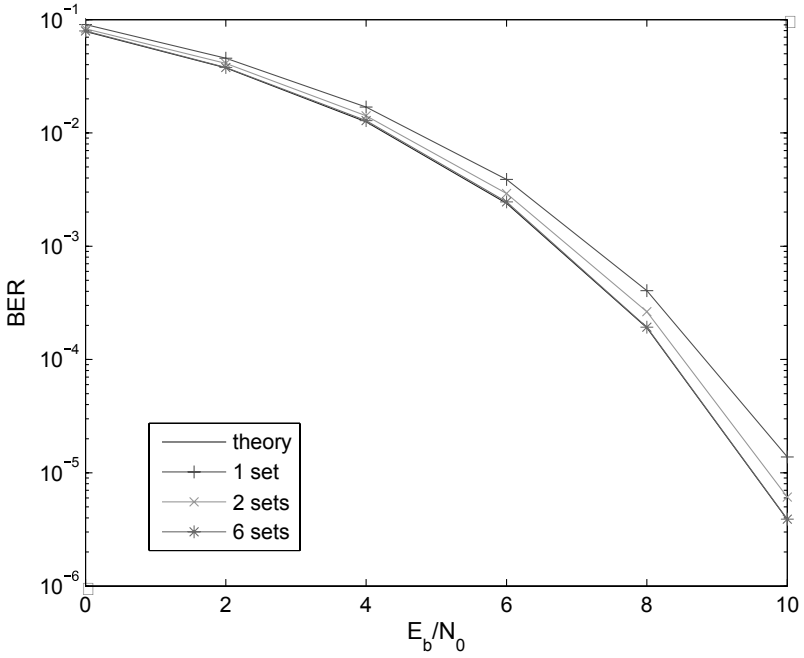

Figure 4.17: BER vs. E_b/N_0, QPSK-OFDM.

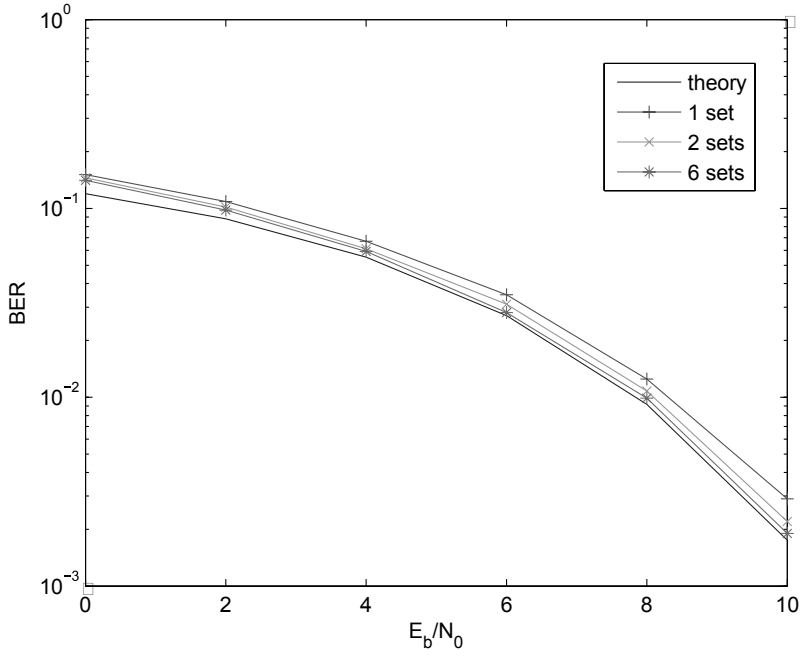

Figure 4.18: BER vs. E_b/N_0, 16QAM-OFDM.

Figure 4.17 shows the BER vs. E_b/N_0 results for QPSK-OFDM modulation and Fig. 4.18 shows the results for 16QAM-OFDM modulation when 300MHz sample rate is converted to 360MHz. The QPSK-OFDM modulation results shows 0.5[dB] degradation at the BER of 10^{-4} while the 16QAM-OFDM modulation results show 0.5[dB] degradation at the BER of 10^{-2} when only 1 set inserter is used. The performance is slightly improved when 2 sets of inserters are used and the maximum performance is obtained when the maximum number of inserters is used.

Adjacent Channel Interference

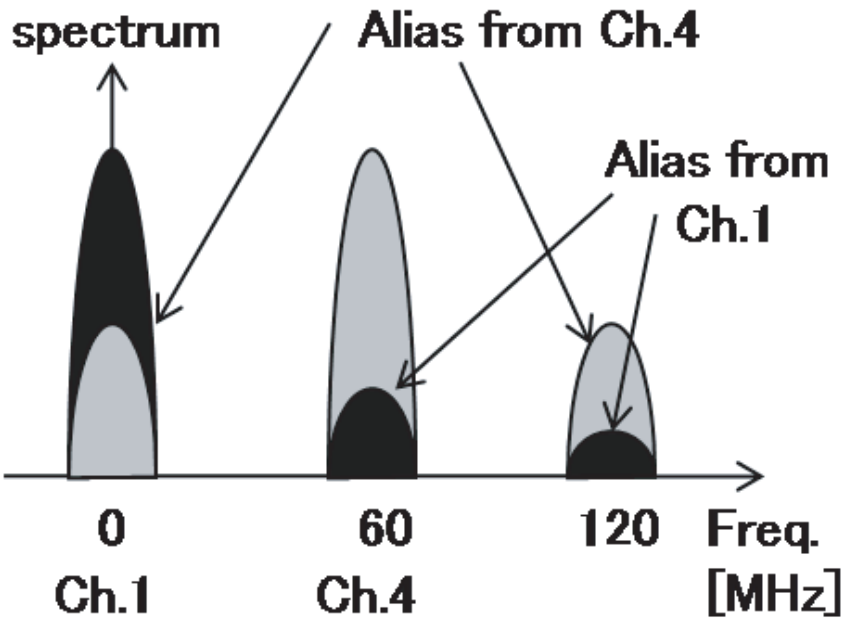

Figure 4.19: ACI due to the direct insertion.

The aliasing from the adjacent channel interferes the desired signal and degrade the performance. The effect of the ACI can be reduced by using multiple sets of inserters/deleters. In a case where channel 1 as the desired signal and channel 4 as the adjacent channel are received as shown in Fig. 4.19, the aliasing from the adjacent channel directly interferes the desired signal. The results for QPSK-OFDM

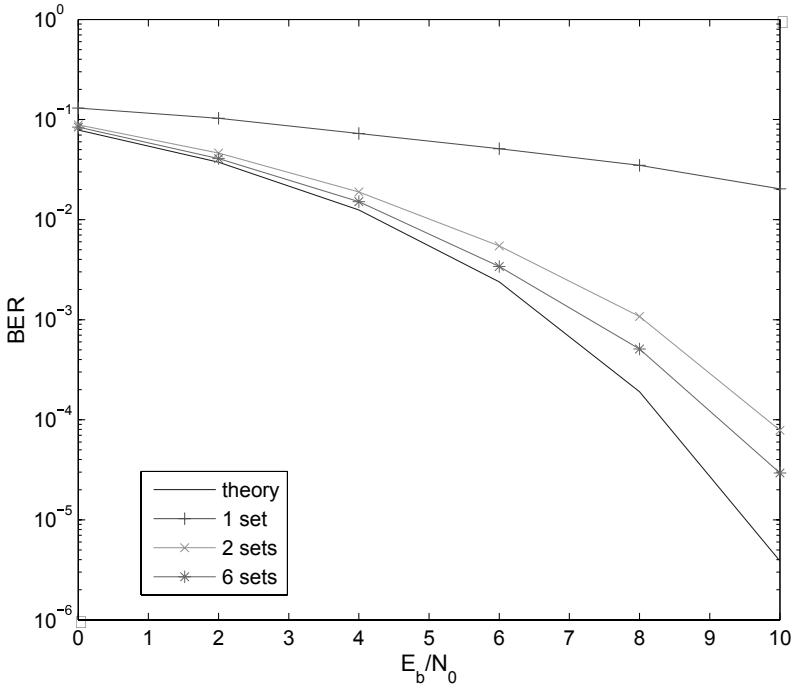

Figure 4.20: BER vs. E_b/N_0, QPSK-OFDM, SIR=-10[dB].

modulation with ACI is shown in Figs. 4.20 and 4.21. In Fig. 4.20, it is shown that the BER performance of the resampled signal at SIR=-10[dB] is severely degraded if only one inserter is used. The performance is largely improved when 2 sets and 6 sets of inserters are used. At E_b/N_0 of 8[dB], the performance is improved for about 10[dB] of SIR when 2 sets of inserters is used and it is improved for about 15[dB] of SIR when the maximum 6 inserters are used.

4.6 Conclusions

The low-complexity fractional SRC for the signal that is sampled with a high sample rate and a large OSR based on the direct insertion/cancellation scheme has been proposed. The performance of the direct insertion/cancellation scheme is improved by implying multiple sets of inserters/deleters in the sample insertion and cancellation

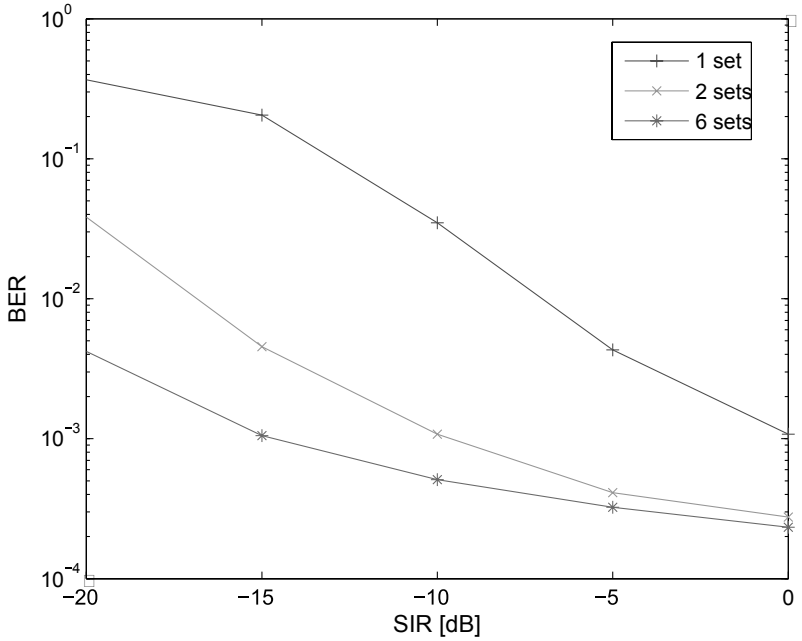

Figure 4.21: BER vs. SIR, QPSK-OFDM, E_b/N_0=8[dB].

block. Numerical results through simulation have proved that the proposed scheme can reduce the MSE, aliasing and distortion after the resampling process. It has also been proven that the proposed scheme can mitigate the ACI due to the aliasing.

Chapter 5

Overall Conclusions

In this thesis, we have investigated several receiver architecture to realize flexible wide-band receiver for SDR terminal. We used 2 difference approaches to realize the SDR terminal. One with the multi-channel low-IF receiver which are present in Chapter 2 and 3; and the other one by using RF-sampling receiver which is present in Chapter 4. In the wideband signal receivers, the received signal components may cause interference to each other. The issues regarding the ACI has been investigated, and the methods to mitigate the ACI have been proposed and discussed.

In the cases when the adjacent channel signal is much larger than the desired signal, high resolution ADCs have to be employed to accommodate such a signal with large dynamic range. The increase of the resolution of the ADC causes higher power consumption and higher implementation cost. Moreover the ACI component may directly overlap with the desired signal if the interference is much larger than desired signal.

In Chapter 2, we proposed the ACI cancellation scheme with analog filter bank for multi-channel reception. The filter bank reduces the dynamic range requirements of the ADCs. The remaining interference components are then canceled from received signal through Wiener filter. In the proposed scheme, training sequence is required periodically to estimate the characteristics of interference signal. From experiment results, it has been shown that the proposed combination scheme of the

analog and digital signal processing can mitigate the influence from the adjacent channel and enables multi-channel reception with relatively low resolution of ADCs with the adaptive digital signal processing. Therefore, the proposed multi-channel reception can be applied to a WLAN receiver system to realize the seamless handover process. This will enable VoIP services on WLAN system.

In Chapter 3, we discussed the application of undersampling for the system that has been described in Chapter 2. The proposed scheme in Chapter 2 requires multiple branches of filter bank, and each branch of the filter bank requires 2 ADCs. Moreover, high speed ADCs are also has to be prepared for the higher frequency channel. Thus, the power consumption of the ADCs may be a problem. Therefore, undersampling technique is employed in this scheme in order to lower the required sampling frequency and power consumption of the ADC. The proposed scheme only requires two branches of filter for the multi-channel reception scheme. The center frequency of the BPFs can be switched depending to the received channels.

The undersampling technique requires very high performance BPFs to avoid aliasing from the adjacent channel. Due to the restriction of circuit size, such BPF is hard to be realized. In the proposed scheme, the remaining interference components that translated in the desired channel band are canceled by using the Wiener filter. The experiment results proved that the proposed scheme can mitigate the influence from the adjacent channel. It has been also proven that the undersampling technique can be applied in this scheme even with a low quality simple BPF. The proposed scheme enables multi-channel reception with relatively low resolution and sampling frequency of ADCs with the adaptive digital signal processing.

In Chapter 4, we investigated a high-speed SRC scheme for RF sampling receiver application based on the direct insertion/cancellation technique. The objective of the scheme was to realize a high-speed and high-performance SRC scheme with low-complexity and lower power consumption. the high-speed SRC scheme for high

sample rate data can be realize by a direct insertion/cancellation scheme. However, the direct insertion/cancellation technique suffers from large aliasing and distortion as compared to the other SRC techniques. The aliasing from an adjacent channel interferes the desired signal and degrades the performance.

We proposed the low-complexity fractional SRC for the signal that is sampled with a high sample rate based on the direct insertion/cancellation scheme. In the proposed scheme we innovated the conventional direct insertion/cancellation scheme by implying multiple sets of inserters/deleters in the sample insertion and cancellation block. In the Chapter, we analyzed the mean squared error (MSE) of the converted samples with mathematical calculations and simulated the MSE by computer simulation to prove the equations. The numerical results through simulation have proved that the proposed scheme can reduce the MSE, aliasing and distortion after the resampling process. It has also been proven that the proposed scheme can mitigate the ACI due to the aliasing. Therefore, the high-speed high-performance low-complexity fractional SRC for RF sampling receiver application can be realized with the proposed scheme.

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