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Keio University

Thesis Abstract

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Thesis Title

A Study on High-Speed Low-Power Ultra-Wideband Transceiver for Short-Range Wireless Communications

Thesis Summary

Short-range, high-speed wireless is certainly the surging trend in communication systems today. Ultra-wideband (UWB) is a revolutionary approach for short-range wireless communications in that it has the potential for high data rates and low power systems. Unlike conventional wireless communication systems, UWB systems transmit and receive pulse-based waveforms compressed in time rather than sinusoidal waveforms compressed in frequency and offer data rates of several Gb/s over a communication distance of few cm. Furthermore, CMOS UWB transceiver achieves low power low cost compared with discrete component solution. Moreover, a transceiver that uses on-chip antenna can further reduce the cost of the overall system. Although UWB systems can reach several meters with data rates of up to hundreds of Mb/s, the front end circuits itself in these systems consume hundreds of milliwatts. Design of a transceiver that operates at a data rate of several Gb/s, while consuming power in the order of few tens of milliwatts is thus essential. This motivates a study on short-range, high-speed, low-power UWB transceivers. The dissertation addresses various design aspects of the circuit design for UWB transceivers and their implementation issues, and presents two major contributions in high-speed low-power short-range CMOS UWB transceivers.

Chapter 1 is an introduction of the study. Background of ultra-wideband technology and recent trends in wireless communication are outlined along with the motivation for the study.

In chapter 2, design theory and issues for impulse radio ultra-wideband transceivers are discussed. Different UWB architectures and modulation schemes are investigated for high-speed low-power operation. The possibilities of using an on-chip antenna as a future low cost solution for short distance wireless communication are investigated and issues in design of on-chip antenna are discussed at the end of the chapter.

Chapter 3 demonstrates a 750 Mb/s CMOS IR-UWB transceiver with an on-chip antenna, which is developed based on the design theory of chapter 2. The transceiver operates within 6-10 GHz band over a communication distance of 10 cm. The receiver operation is verified with simulation results while a low-power transmitter is realized in CMOS with an all-digital pulse generator circuit that limits the power consumption of the transmitter to 12 pJ/b for the maximum data rate of 750 Mb/s. A monopole on-chip antenna is fabricated on chip and demonstrated for the operation over the 6-10 GHz band.

Chapter 4 demonstrates a 4 Gb/s CMOS IR-UWB transceiver that operates over the quasi-millimeter-wave frequency band of 14-18 GHz. A transmitter that uses a PLL and an up-conversion mixer to generate BPSK modulated signal and a receiver with direct conversion architecture and a high-speed carrier and symbol timing recovery scheme are proposed. Measured results of the fabricated transmitter and simulation results of the receiver are presented that bolster the claims of 4 Gb/s data rate over quasi-millimeter-wave band.

Chapter 5 is conclusion of the study. Results from each chapter are summarized and overview of the future work is mentioned.