A Study on High-Speed Low-Power Ultra-Wideband Transceiver for Short-Range Wireless Communications

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Thesis Abstract

Short-range, high-speed wireless is certainly the surging trend in communication systems today. New wireless standards being developed such as wireless USB or wireless HDMI demand transmission of very large data at very high-speed and at low-power. Ultra-wideband (UWB) is a revolutionary approach for short-range wireless communications in that it has the potential for high data rates and low power systems. Unlike conventional wireless communication systems, UWB systems transmit and receive pulse-based waveforms compressed in time rather than sinusoidal waveforms compressed in frequency and offer data rates of several Gb/s over a communication distance of few cm. Furthermore, CMOS UWB transceiver achieves low power low cost compared with discrete component solution. Moreover, a transceiver that uses on-chip antenna can further reduce the cost of the overall system. Although UWB systems can reach several meters with data rates of up to hundreds of Mb/s, the front end circuits itself in these systems consume hundreds of milliwatts. Design of a transceiver that operates at a data rate of several Gb/s, while consuming power in the order of few tens of millwatts is thus essential. This motivates a study on short-range, high-speed, low-power UWB transceivers. The dissertation addresses various design aspects of the circuit design for UWB transceivers and their implementation issues, and presents two major contributions in high-speed low-power short-range CMOS UWB transceivers.

Chapter 1 is an introduction of the study. Background of ultra-wideband technology and recent trends in wireless communication are outlined along with the motivation for the study.

In chapter 2, design theory and issues for impulse radio ultra-wideband transceivers are discussed. Different UWB architectures and modulation schemes are investigated for high-speed low-power operation. The possibilities of using an on-chip antenna as a future low cost solution for short distance wireless communication are investigated and issues in design of on-chip antenna are discussed at the end of the chapter.

Chapter 3 demonstrates a 750 Mb/s CMOS IR-UWB transceiver with an on-chip antenna, which is developed based on the design theory of chapter 2. The transceiver operates within 6-10 GHz band over a communication distance of 10 cm. The receiver operation is verified with simulation results while a low-power transmitter is realized in CMOS with an all-digital pulse generator circuit that limits the power consumption of the transmitter to 12 pJ/b for the maximum data rate of 750 Mb/s. A monopole on-chip antenna is fabricated on chip and demonstrated for the operation over the 6-10 GHz band.

Chapter 4 demonstrates a 4 Gb/s CMOS IR-UWB transceiver that operates over the quasi-millimeter-wave frequency band of 14-18 GHz. A transmitter that uses a PLL and an up-conversion mixer to generate BPSK modulated signal and a receiver with direct conversion architecture and a high-speed carrier and symbol timing recovery scheme are proposed. Measured results of the fabricated transmitter and simulation results of the receiver are presented that bolster the claims of 4 Gb/s data rate over quasi-millimeter-wave band.

Chapter 5 is conclusion of the study. Results from each chapter are summarized and overview of the future work is mentioned.

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Chapter 1 Introduction

1.1 Background

Wireless is certainly the surging trend in technology today. Customers first discovered the benefits of wireless in their mobile phone for voice and more recently in their notebook computer for convenient internet access. Manufacturers and users are rapidly adopting personal wireless technologies to connect their own products.

Yet even with this progress what has been missing is a universal wireless technology with the performance to connect consumer electronic multimedia products. To actually deliver on consumer expectations, wireless technologies need to be significantly faster than what is currently available today while at the same time managing to be power efficient during operation.

Cost is another important factor which influences the research of wireless devices in today's ubiquitous society. Taking cost factor into account, it is desirable to design RF circuits using CMOS process and utilize the license free frequency band. Since some frequency bands are already allocated for particular applications, the cost for utilizing those bands for wireless communication is very high. In order to reduce the cost involved in wireless communication, we must be able to utilize the frequency band freely.

To meet these demands, pioneers in the industry are working on the Ultra-Wideband (UWB) technology.

1.1.1 Demands of Today's Wireless Technology:

Conventional communication systems which were designed some decades ago focused on the transmission of data at larger distances. But communication standards and needs in the modern world have changed significantly since the time conventional systems were designed. Today's wireless communication systems demand transmission of very large data at very fast rate and for many users, all at once. In the past few years, shorter range systems, from 10 to 100 meters have begun emerging, driven primarily by data applications.

Four trends are driving short-range wireless in general and ultra-wideband in particular [1-3]:

1. The growing demand for wireless data capability in portable devices at higher bandwidth but lower in cost and power consumption than currently available.
2. Crowding in the spectrum that is segmented and licensed by regulatory authorities in traditional ways.
3. The growth of high-speed wired access to the Internet in enterprises, homes and public spaces.
4. Shrinking semiconductor cost and power consumption for signal processing.

Furthermore, the recent developments in high-speed switching technology due to advanced semiconductor processes have made UWB more attractive for low-cost consumer communication applications.

1.1.2 Motivation for Using UWB

There are broadly four reasons to explain the use of very short duration pulses in UWB communication.

Firstly, data communication speed higher than the conventional narrowband systems can be achieved. Existing conventional wireless communication systems use very complex processes to avoid multipath fading effect. In case of short pulses, since the time interval is very short, the possibility of separating the transmitted signal from the multipath is higher. Consequently, the multipath fading effect is very low. Furthermore, as we can see from Shannon's channel capacity theorem,

$$C = B\log_2\left(1+\frac{S}{N}\right)$$

Where,

C = Maximum Channel Capacity (bits/sec)

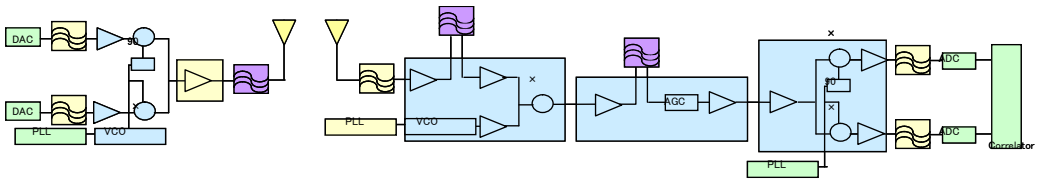
B = Channel Bandwidth (Hz)

S = Signal Power (watts)

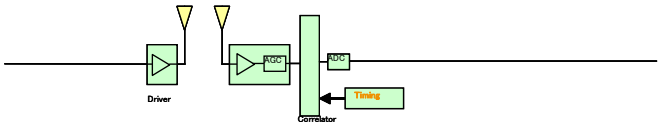
N = Noise Power (watts)

Because the upper bound on the capacity of a channel grows linearly with total available bandwidth, UWB systems, occupying 2GHz or more, have greater room for expansion than systems that are more constrained by bandwidth [2]

Secondly, the architecture of the pulse based UWB systems is very simple compared to the complex architecture of existing RF communication systems.



Double heterodyne transceiver



UWB transceiver : Simple, CMOS only

Figure 1.1 Conventional narrowband system architecture vs UWB architecture.

Figure 1.1 illustrates the difference between the conventional narrowband system and pulse based UWB system. Conventional architecture uses many complex system blocks. Also some of the blocks use compound semiconductors such GaAs. On the other hand the architecture of carrierless UWB systems is very simple. Moreover, it can be realized in CMOS which can be very cost effective.

Thirdly, due to the simplicity of architecture, UWB systems have extremely low power dissipation. Pulse based UWB transmit short duration baseband pulses directly. This way, power hungry components in receiver side can be eliminated. Furthermore, due to the emission constraints of FCC, the maximum allowed power levels for UWB are very low. So, UWB systems operate at very low power transmission levels.

Lastly, the UWB frequency spectrum occupies a large bandwidth with very low power distribution over the band. So the influence of the interference from other systems can be very small.

Pulse based UWB with several advantages over the conventional narrowband wireless communication systems proves to be very promising technology in next generation ubiquitous society.

1.2 Overview of Ultra-Wideband System

Ultra-Wideband (UWB) Radio is a potentially revolutionary approach to wireless communication in that it transmits and receives pulse based waveforms compressed in time rather than sinusoidal waveforms compressed in frequency. Unlike the conventional communication systems, which use sinusoidal carrier to transmit the data, UWB systems use very short duration pulses for data transmission. Since the pulses are very short in time domain, they occupy a large bandwidth in frequency domain.

1.2.1 History of Ultra-Wideband

The roots of UWB technology date back to the invention of radio by Guglielmo Marconi in the ninetieth century. Back then, radio transmitters used enormous amount of bandwidth to convey information over a distance using spark gap transmitters. Later in 1960s, UWB was used in radar systems for tracking the objects since the wideband nature of UWB signals results in accurate timing information. Although a century old technology, UWB found its usage in day-to-day communication systems fairly lately in the twenty first century when the Federal Communications Commission (FCC) allowed a wide frequency spectrum for the unlicensed use of UWB.

1.2.2 FCC Allowed UWB System

In February 2004, the FCC allocated the 3.1-10.6 GHz spectrum for unlicensed use [4]. This enabled the use and marketing of products, which incorporate UWB technology. Since the allocation of the UWB frequency band, a great deal of interest has generated in

industry. However, the FCC's Part 15 rules [4] place emission limits on intentional and unintentional radiators in unlicensed bands. These emission limits are defined in terms of microvolts per meter (μV/m), which represent the electric field strength of the radiator. In order to express this in terms of radiated power, the following formula can be used. The emitted power from a radiator is given by the following:

$$P = \frac{E_0{}^2 4\pi R^2}{\eta}$$

Where E_0 represents the electric field strength in terms of volts per meter (V/m), R is the radius of the sphere at which the field strength is measured, and η is the characteristic impedance of vacuum in which η = 377 ohms. For example, for frequencies greater than 960 MHz, the FCC's Part 15 rules limit emissions of intentional radiators to 500 μV/m measured at a distance of three meters in a 1 MHz bandwidth. This corresponds to an emitted power spectral density of -41.3 dBm/MHz. The UWB spectral mask, depicted in Figure 1.2, was defined to allow a spectral density of -41.3 dBm/MHz throughout the UWB frequency band in order to limit interference with other systems.

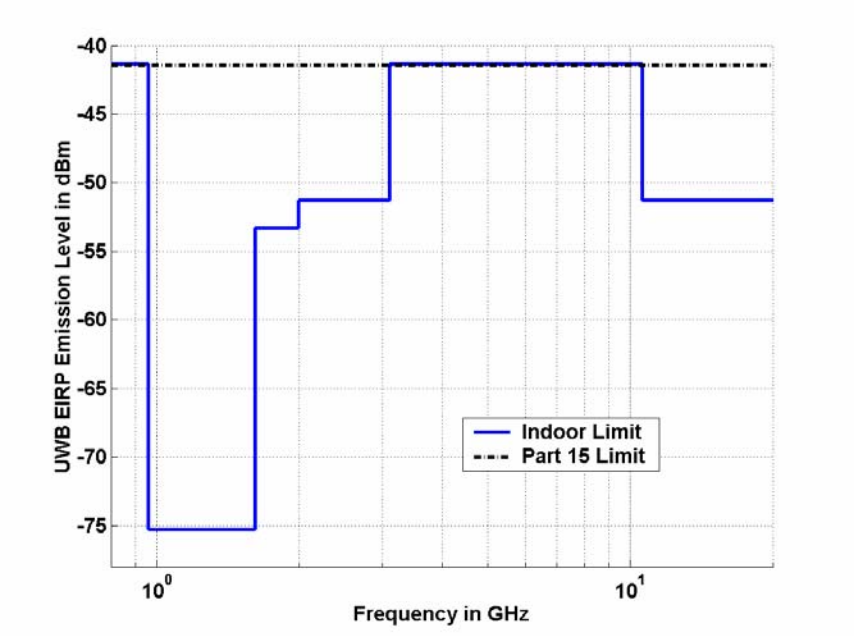


Figure 1.2 FCC spectral mask for indoor unlicensed UWB transmission.

Operation at such a wide bandwidth entails lower power that enables peaceful coexistence with narrowband systems. These specifications presented a myriad of

opportunities and challenges to designers in a wide variety of fields including RF and circuit design, system design and antenna design. This thesis focuses on approaches to implement wireless communication systems based on FCC's definition of what constitutes a UWB system.

1.2.3 Definition of UWB

Ultra Wideband is defined as any communication technology that occupies greater than 1.5 GHz of bandwidth, or greater than 25% of the operating center frequency. Most narrowband systems as shown in Figure 1.3 occupy less than 10% of the center frequency bandwidth, and are transmitted at far greater power levels. In contrast, UWB systems occupy much greater bandwidth for transmission of data at comparatively shorter distances. Recently, FCC has defined a UWB device as one with fractional bandwidths greater than 20% or the one that occupies at least 500 MHz of spectrum.

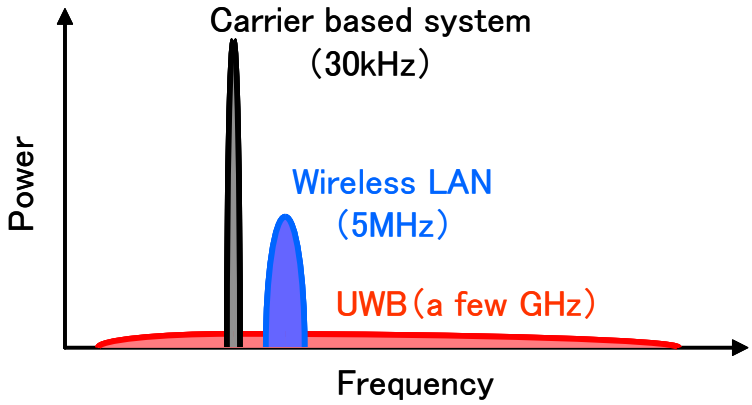


Figure 1.3 Frequency spectrum of UWB and conventional narrowband systems.

Figure 1.3 illustrates difference in the frequency spectrum occupied by different communication systems such as 30 kHz carrier based system, wireless LAN and UWB. Since UWB systems occupy a very large frequency range, their power can be distributed over the wide band and the peak transmission power levels are very low compared to the conventional communication systems such as global positioning systems (GPS), federal aviation systems (FAS), Bluetooth and WLAN. Hence, UWB signals should appear as low-power white noise and have little impact on the underlying operating devices.

1.2.4 Types of UWB systems

Broadly, UWB has two design approaches, a pulse based system and a carrier based system.

The pulse based system follows the tradition approach to use wide bandwidth by making use of modulated pulses to transfer information. Impulse Radio UWB (IR-UWB) or Direct Sequence Spread Spectrum (DS-SS) UWB is a form of this approach, which is used in conventional military applications and radios. The impulse method utilizes the transmission of short pulses without using any carrier. This method is very cost effective and also very power efficient since the pulses are generated in base band and transmitted without any carrier. Direct sequence spread spectrum (DS-SS) encoding offers another way to achieve data rate scaling through employing multiple parallel spreading codes. In this method, one or possibly two carriers are used to spread the pulse over the band. The RF front-end systems for this approach tend to be simple because of the characteristics of the pulse. Moreover, the need for up-conversion or down-conversion is eliminated which is a necessity in traditional narrowband systems.

A DS-SS system follows the traditional approach to accommodate a wide bandwidth. An information-bearing signal is generated using very short, low-duty cycle and base-band electrical impulses [3]. Because no carrier is used to up-convert or down-convert the signal, such systems are often called carrier-free, base-band or impulse radio communication systems.

If a single pulse with a certain repetition rate is transmitted over the channel, its frequency spectrum shows a peak, which can interfere with other existing communication signals. To alleviate this problem, a technique called direct sequence spread spectrum (DS-SS) is used. By using this technique, energy contained in repeated pulses is spread over a wide frequency range, and in turn the problem aroused by using single pulse approach is alleviated. Since it is difficult to control the exact shape of the impulse and consequently the overall frequency response, the DS-SS systems tend to use the entire allocated frequency band and hence sometimes called as single band systems.

DS-SS systems that use code division multiple access (CDMA) are often referred as direct sequence code division multiple access (DS-CDMA) systems. DS-CDMA systems generally use a two-band approach as shown in Figure 1.4. The low band consists of the frequency spectrum from 3.1 GHz to 5.15 GHz, and the high band ranges from 5.825 GHz to 10.6 GHz. Since the UWB frequency spectrum overlaps the existing 802.11a WLAN system from 5.15 GHz to 5.825 GHz, the two-band system avoids the use of overlapping frequency ranges.

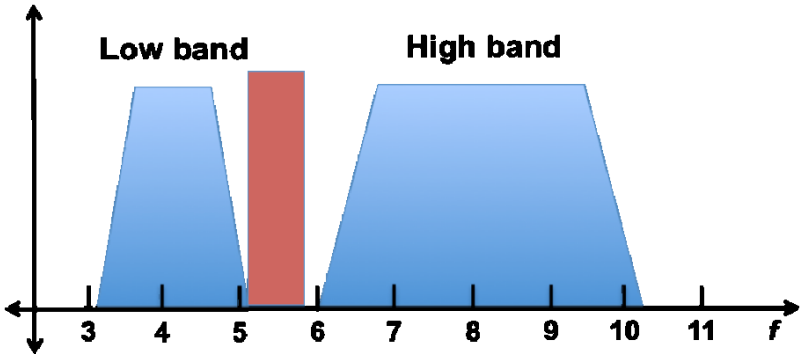


Figure 1.4 Spectrum usage of UWB DS-CDMA system.

In contrast, the carrier-based system follows the approach of traditional narrow band system that has been extended to accommodate a wide bandwidth. Therefore, the architecture of carrier-based system closely resembles to that found in conventional narrowband systems.

This approach can be thought of as an extended version of 802.11a wireless LAN despite some differences, such as frequency hopping. In this system, the entire UWB spectrum is divided into several bands with a fixed bandwidth of 528MHz. Information is transmitted using orthogonal frequency division multiplexing (OFDM) modulation on each band. As it uses several sliced bands with OFDM modulation, it is called a multiband OFDM (MB-OFDM) system [5]. Since the system uses a carrier to transmit information, the system can be categorized as a carrier-based system, which is clearly different from the pulse-based DS-CDMA system. The details of the band plan are shown in Figure 1.5. Such a technique possesses better spectral control properties.

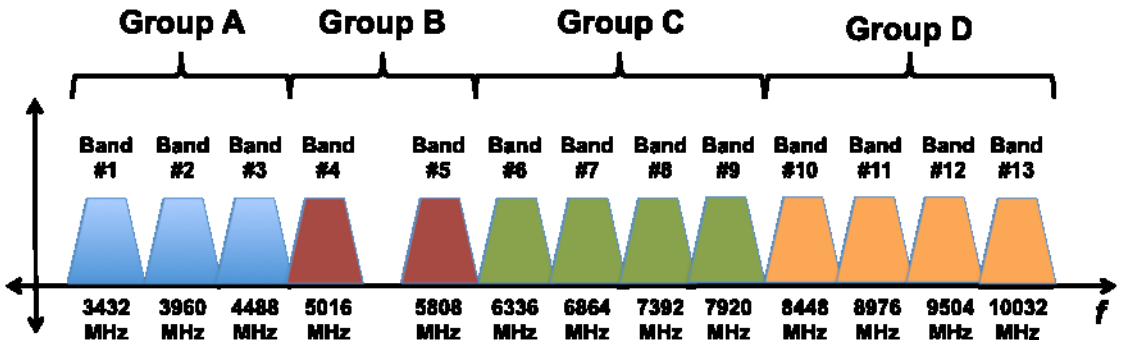


Figure 1.5 Band allocation and spectrum usage of MB-OFDM system.

Multi-band OFDM method is very robust to inter-symbol interference and can achieve very high data rates. However, due to its complex architecture, it consumes more power than the IR-UWB.

Amongst the two methods, this research focuses on the impulse radio based UWB because of the simplicity of architecture, low power dissipation, low cost and robustness to multi-path fading. However, the generation of extremely short duration pulses of the order of few hundred picoseconds poses a major challenge while adopting this method. The dissertation proposes new circuit topologies to generate extremely short duration pulses and demonstrates transceivers that operate at very high data rates using DS-SS UWB.

1.3 Research Motivation

When wireless communication systems began in early 1960s, the only objective was the reliable transfer of voice over the channel. With the success of wireless communication technology in late twentieth century, this objective has been transformed to replacing every wired system to a wireless one. This objective of wireless systems extends to the concept of ‘ubiquity’, which in terms of wireless communication can be defined as ‘anywhere at any time’. In a ubiquitous environment, communication devices will interact with each other seamlessly and users will use a simple platform to obtain information at any time without any awareness of a distinction between wireless and wired networks. The realization of this ubiquitous environment is already started with the

development of long and medium distance wireless communication systems such as cellular phones and wireless LAN. The recent advancements in ultra-wideband technology has given a new dimension to the realization of high-speed short-distance communications.

A transceiver with an embedded antenna on a single chip can be a cost effective solution for short distance communication applications. This not only eliminates the need for external antenna and expensive packaging, but also reduces the size of the module footprint by significant amount. For the communication range of few centimeters, several new applications can be thought of such as video transfer between a camera and a computer, or a video download at a kiosk, which will parallel wireless 1394 or wireless USB 3.0. These applications require transceiver systems to operate at high data rates while consuming low power. Although UWB systems (3-10GHz) can reach several meters with data rates of up to 480 Mb/s and the millimeter wave systems have potential to reach up to several Gb/s, the front end circuits itself in these systems consume hundreds of milliwatts. Since most of the handheld portable devices operate on a battery, the next generation wireless communication systems demand design of a transceiver that operates at a data rate of several Gb/s, while consuming power in the order of few tens of milliwatts.

All these factors motivate a detailed study on a high-speed low-power wireless ultra-wideband transceiver which will operate over a communication distance of few centimeters.

1.4 Target of This Research

The primary objective of this research is to design a low power high speed CMOS UWB transceiver system for the next generation ubiquitous society. The research targets on the design of a transceiver system which will communicate within the distance of few centimeters for a target data range of few Gb/s. So far considerable research has been done on the design of UWB systems and many works [10-31] have reported ultra-wideband transceiver systems as shown in Figure 1.6.

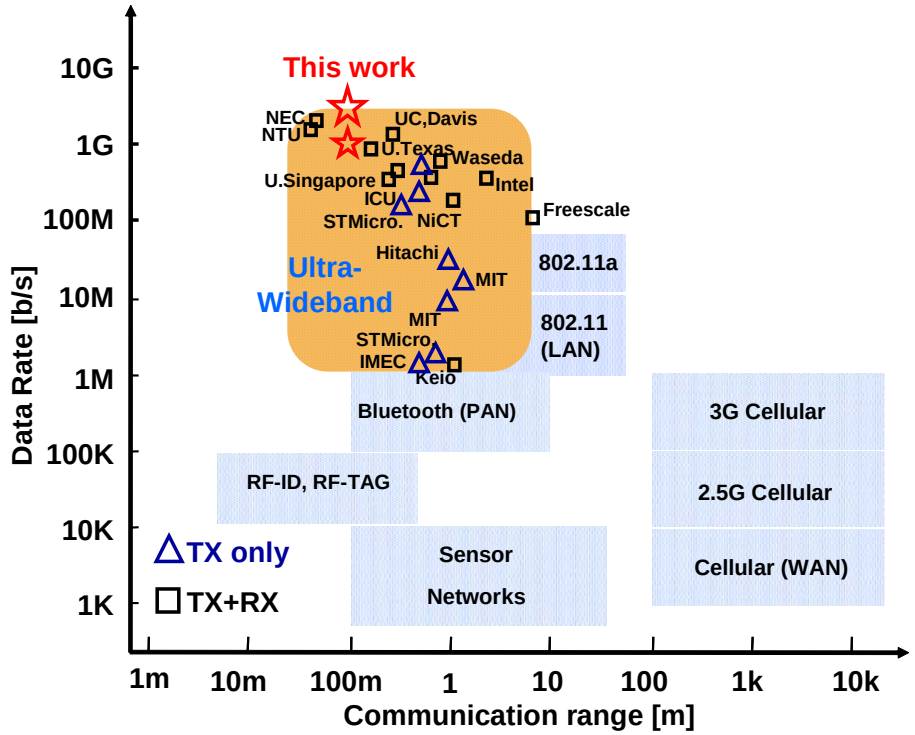


Figure 1.6 Technology trends in wireless communications.

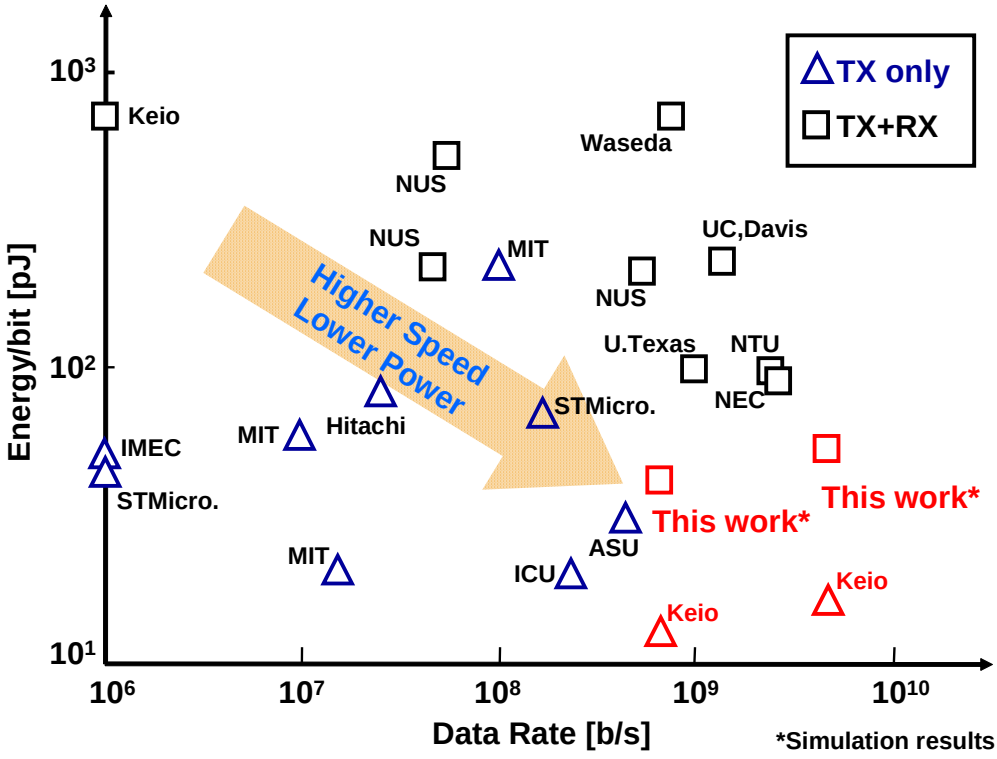


Figure 1.7 Data rate vs energy consumption of UWB systems reported recently.

Although, some of the systems [32-35] reported have reached to a data rate in the order of Gb/s within the communication distance of few centimeters, the power consumption of these systems is considerably high. If the energy per bit is chosen as a unit to compare the power consumption of various systems, most of the works reported in Figure 1.7 have the energy consumption close to 100 pJ/b. This research targets two contributions in the UWB state-of-art. First, a transceiver that will match the data rate of wireless USB which is in the order of few hundred Mb/s for the use in portable wireless handheld devices is targeted. Although many transceivers have been reported to operate with this data rate, the energy consumption of these transceivers is in the order of 100 pJ/b. Since the portable wireless handheld devices operate on battery, low energy consumption is of primary interest in the design of this transceiver. The energy consumption of the order of 10 pJ/b for the transmitter and 40 pJ/b for the receiver is targeted. The research also targets design of high speed low power transceiver for the high end communication applications such as wireless HDMI that require data rates of the order of few Gb/s. So far many works have reported transceivers that operate over 1 Gb/s data rate. However, no system has been able to reach the data rate of 4 Gb/s required for such applications. The target data rate for this transceiver is 4 Gb/s while the energy consumption requirements are 50 pJ/b for a target communication distance of 10 cm. The research target also includes design of an on-chip antenna and its simulation using 3-D electromagnetic simulator for the feasibility of communication within a distance of 10 centimeters.

1.5 Thesis Contribution and Overview

This thesis is divided into five chapters as shown in Figure 1.8. In chapter 2, design theory and issues for impulse radio ultra-wideband transceivers are discussed. Different UWB architectures and modulation schemes are investigated for high-speed low-power operation. The possibilities of using an on-chip antenna as a future low cost solution for short distance wireless communication are investigated and issues in design of on-chip antenna are discussed at the end of the chapter with the help of simulated and measured results of various on-chip antenna structure implementations.

Chapter 3 demonstrates a 750 Mb/s CMOS IR-UWB transceiver with an on-chip antenna, which is developed based on the design theory of chapter 2. The transceiver operates over 6-10 GHz band over a communication distance of 10 cm. A novel pulse generator circuit is designed to operate at very low power producing short duration bi-phase modulated pulses of 500 ps duration with a duty cycle of 750 Mb/s. The receiver operation is verified with simulation while a low-power transmitter is realized in CMOS with an all-digital pulse generator circuit that limits the power consumption of the transmitter to 12 pJ/b. A monopole on-chip antenna is fabricated on chip and demonstrated for the operation over the 6-10 GHz band.

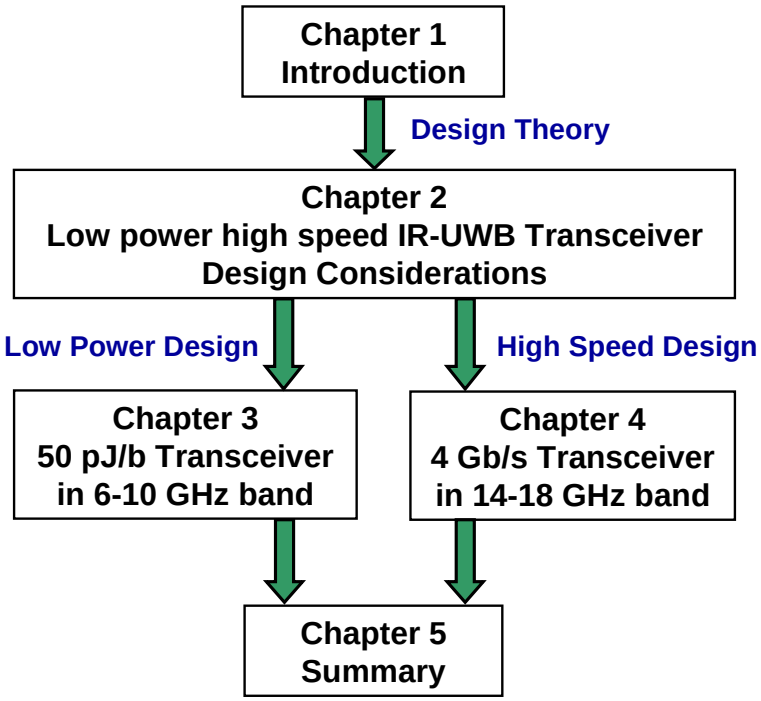


Figure 1.8 Organization flowchart of dissertation.

Chapter 4 demonstrates a 4 Gb/s CMOS IR-UWB transceiver that operates over the quasi-millimeter-wave frequency band of 14-18 GHz. A transmitter that uses a PLL and an up-conversion mixer to generate BPSK modulated signal, and a receiver with direct conversion architecture and a high-speed carrier and symbol timing recovery scheme are proposed. Measured results of the fabricated transmitter and simulation results of the receiver are presented that bolster the claims of 4 Gb/s data rate over quasi-millimeter-wave band.

Chapter 5 presents conclusion of the study. Results from each chapter are summarized and overview for the future work is mentioned.

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Chapter 2 IR-UWB Transceiver Design Considerations

2.1 Introduction

A lot of debate is under way about which system between IR-UWB and MB-OFDM is more appropriate for implementing the FCC-allowed UWB system. The debate involves numerous issues, such as power emission, implementation complexity caused by the modulation incorporated, achievable data rate, multi-user capability, and so on. In this research, impulse radio (IR) UWB system was chosen for following reasons [1-2].

- Simplicity of architecture
- Low power consumption
- Reduced Inter Symbol Interference (ISI)

An impulse-radio communicates with base band pulses of very short duration, typically of the order of a nanosecond. This results in spreading of the signal energy in frequency domain from near dc to a few gigahertz. When this pulse is applied to the UWB antenna, it propagates with distortion because of the filter like characteristics of the antenna. Also, the differentiation of the pulse occurs while traveling in space. Although IR-UWB is a promising technology, it poses several challenges in the design of the transceiver systems. Since the regulatory authorities put a limit on the total radiated power, the transceiver must be designed to work with reduced power constraints.

For IR-UWB, a number of architectures are available to choose from. However, the choice is decided by several factors such as power consumption, bit error rate (BER), simplicity in implementation, type of modulation scheme used, achievable data rate and so on. These factors generate a tradeoff in the choice of suitable architecture. Following sections present an overview of the design flow for IR-UWB transceivers.

2.1.1 System Design Flow

The top down approach for IR-UWB system design involves following steps

1. **Consideration of propagation channel model**

The propagation channel can be modeled from one amongst several models such as static (Additive White Gaussian Noise) model, a Rayleigh model or a Ricean model. The propagation model varies depending on the environment such as residential indoor, office indoor, built-up outdoor, industrial outdoor and body area networks. Based on these environments, propagation model can be of either of free space propagation or urban propagation or UWB propagation (802.15.3a).

2. Link budget estimation

Link budget estimation is summation of gain and loss in the transceiver system. The link budget involves a rough estimation of following factors [3-4]

- Noise (thermal noise, 1/f noise)
- Transmitter and receiver antenna gain
- Propagation loss (Static or variable)
- Noise figure
- Modulation and detection performance
- Process gain
- Error correction gain
- Link margin

The link budget analysis helps determine the feasibility of the transceiver system and is an important step before the selection of the architecture. A link budget calculation is also an excellent means to understand the various factors which must be traded off to realize a given cost and level of reliability for a communication link.

3. Selection of band of operation

The transceiver design, especially the front-end design changes according to the frequency band of operation. IR-UWB systems primarily utilize two bands: the 3-5 GHz upper band and the 6-10 GHz lower band. Recently, the quasi-millimeter-wave and millimeter-wave bands have also been investigated for the operation. Interference from other communication systems such as cellular phones, wireless LAN and Bluetooth are a

key factor in choosing the band of operation. Also, issues like harmonics and band-pass filter performance, and issues in antenna and LNA design affect the selection of band. All these issues should be thoroughly investigated before choosing the frequency band of operation.

4. Modulation scheme design

Since the modulation scheme employed decides transceiver complexity, it is apparent that before choosing the architecture, it is necessary to design the modulation scheme. Of course, a UWB signal is not different from any other signal, and any other modulation scheme can be applied, including orthogonal or bi-orthogonal modulations. However, basic modulation schemes such as pulse position modulation, pulse amplitude modulation and phase and frequency modulation are popular among IR-UWB transceivers. The choice of modulation scheme depends on the required bit error rate (BER) and the data rate. The next section describes the modulation scheme design in detail.

5. Architecture design

Once the modulation scheme is designed, the transceiver architecture can be decided. Based on the modulation scheme, the architectures are divided into two major categories, which are coherent and non-coherent architecture. Each architecture has its own advantages and disadvantages and the selection depends on the system requirements such as ease of implementation, data rate and cost.

6. Components design

Although components design forms the last step in the design flow, it is one of the most important tasks in the realization of transceiver system. Although the architectures are different for different modulation schemes, some of the components are common in most of the architectures. Components such as pulse generator and receiver front-end parts such as LNA or mixer are common in any architecture and play a crucial part in the overall performance. Hence, their designs need a thorough understanding of the system requirements and performance standards.

A brief overview of the two main steps in the design flow, which are modulation scheme design and architecture design, are presented in the next sections.

2.2 Modulation Schemes for IR-UWB

A major challenge when designing UWB systems is choosing the right modulation type. Data rate, transceiver complexity, BER performance, and spectral characteristics of the transmitted signal are all related to the employed modulation scheme. Determining the right modulation scheme for the right application is, thus, essential.

The pulse used for UWB communication can be a monocycle Gaussian pulse or a Gaussian monocycle pulse train. The pulse train is acting somewhat like a carrier, which can be used for the purpose of modulation and transmission. The regular monocycle pulse train contains no information. In order to transmit information, the monocycle pulse train needs to be modulated by data. Information transmission can be achieved using a number of ways, including amplitude, time and phase modulation of the UWB pulses [5]. The choice of modulation scheme affects the bit error performance.

In a UWB signal, information can be encoded in a variety of methods. Three of the most popular modulation schemes used for UWB transmission by various groups are as below.

2.2.1 Pulse Position Modulation (PPM)

Pulse position modulation is based on the encoding information by modifying the time shift between the pulses. A pulse transmitted at the nominal position represents a '1', and a pulse transmitted after the nominal position represents a '0'.

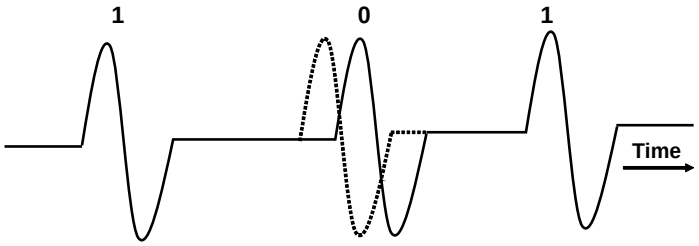

Figure 2.1 Pulse position modulation (PPM) scheme.

Figure 2.1 illustrates the pulse position modulation scheme. In this figure, one bit is encoded by one impulse. Additional positions can be used to provide more bits per

symbol. The time delay between pulses is typically a fraction of a nanosecond, while the time between nominal positions is typically much longer to avoid interference between pulses.

2.2.2 Pulse Amplitude Modulation (PAM)

Pulse amplitude modulation is based on the principle that the amplitude of the impulses is encoded by data. Digital PAM is also called amplitude-shift keying (ASK) or as on-off keying (OOK) for two-level PAM. Figure 2.2 shows the PAM UWB scheme. As with pulse position modulation, more levels can be used in PAM to encode more than one bit per symbol.

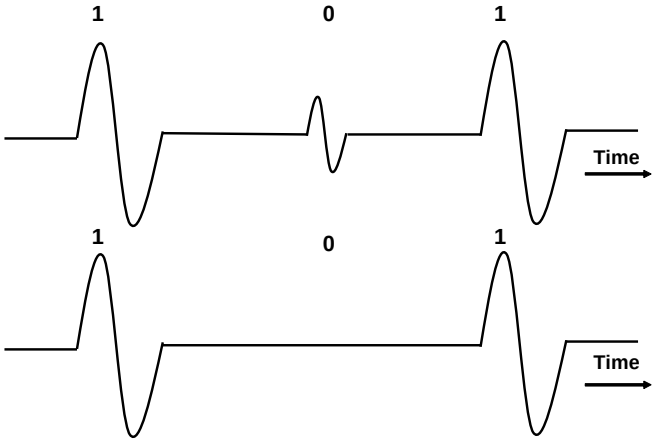

Figure 2.2 Pulse amplitude modulation (PAM) and on-off keying (OOK) scheme.

2.2.3 Phase Shift Keying (PSK)

Phase-shift keying (PSK) is a method in which the phase of a signal is varied in order to transmit information. In binary phase shift keying (BPSK) which is also known an bi-phase modulation (BPM), the phase of the signal is varied by 180 degree with the polarity of the data as shown in Figure 2.3. A variation of BPSK in which four phases are used based on the combination of data bits, known as quadrature phase shift keying (QPSK) is also used in some transceiver systems.

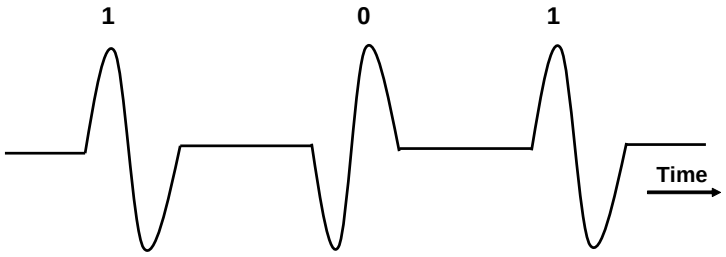

Figure 2.3 BPSK modulation scheme.

Other modulation schemes include multiple access techniques such as direct sequence spread spectrum (DS-SS) [6], time hopped [7] and delay hopped[8] signaling. Although PPM is the most common modulation scheme among IR-UWB transceivers, it has some disadvantages. First, it requires control of time positions on a pulse-to-pulse basis. Therefore a series of wide-bandwidth circuits are required. This is where jitter accumulates. A bi-phase system only needs a stable, low-phase-noise clock, since the spacing of the pulses is constant. In digital clocking, jitter is reduced with bi-phase modulation. Furthermore, since PPM always delay pulses, the time interval required for transmitting PPM pulses is more than that of BPSK limiting the data rate. Given the same pulse width, BPSK can achieve more data rate than that of PPM [5].

This research makes use of the BPSK modulation scheme for transmission of pulse train because of its simplicity and robustness. However, the use of BPSK poses another challenge in the design of receiver. In BPSK, the information is transmitted by changing the phase of the signal. In order to recover the data, the demodulator must obtain correlation between the incoming RF signal and the LO signal. The reason for choosing the BPSK modulation scheme is further elaborated with actual transceiver design in chapters 3 and 4.

2.3 Architecture Overview

In order to achieve high speed and low power performance using IR-UWB, the conventional narrowband architectures need to be modified [9-12]. This section presents an overview of architectures for IR-UWB with merits and demerits of each.

2.3.1 Transmitter Architecture

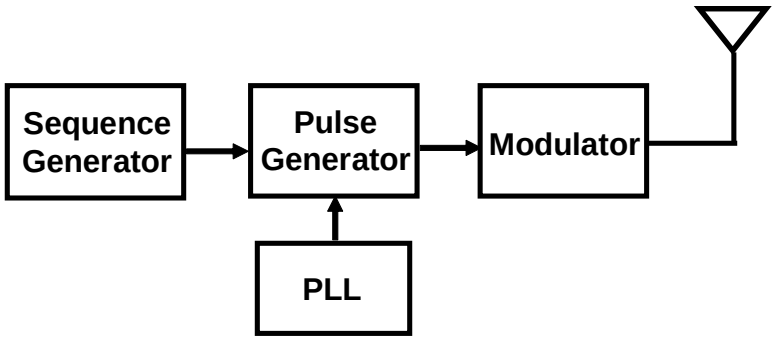

Figure 2.4 IR-UWB transmitter architecture.

Figure 2.4 depitcts the typical IR-UWB transmitter architecture. Since IR-UWB uses short duration pulses to transmit information over the channel, the pulse generator circuit forms the main block of the transmitter. The pulses generated can be either Gaussian monocycle pulses or a train of monocycle pulses depending on the modulation and transmission scheme. Since the operating frequency range is in the order of GHz, a PLL is used to generate stable frequency. The sequence generator can be a counter which generates a sequence which is then mixed with the signal from PLL using the pulse generator to generate a pulse. The pulse can be directly connected to the antenna after modulation without the need for power amplifier as the required output power levels for UWB are very low. However, if the output amplitude of the generated pulse is low, then a power amplifier may need to be inserted before the signal can be fed to the antenna.

Although simple than the conventional narrowband system architecture, the IR-UWB transmitter architecture poses several challenges in its design. Firstly, the generation of extremely narrow pulses of the order of fraction of a nanosecond is extremely difficult. Secondly, the pulses need to be shaped in order to satisfy the spectrum limits imposed by the governing authorities such as FCC. The use of additional filtering or pulse shaping circuits can increase the power dissipation canceling the advantages that come from the simplicity of architecture. If the operation of each block shown in Figure 2.4 can be incorporated in a single circuit, i.e. pulse generator circuit itself, the power consumption of the transmitter can be reduced drastically. Chapters 3 and 4 present new design

topologies for the high speed low power IR-UWB transmitters which overcome the issues discusses above.

The receiver architecture is broadly categorized into two types namely, non-coherent and coherent architecture.

2.3.2 Non-coherent Receiver Architecture

Figure 2.5 illustrates the typical non-coherent receiver architecture for pulse based UWB. Use of OOK modulation is most common in this kind of architecture. The received pulses are amplified by the LNA. They are self mixed at the mixer and passed through the low pass filter. The VGA then amplifies the pulses which are then compared by the comparator to detect the base band data. This architecture is very simple because the complex synchronization circuits are not necessary. Furthermore, the influence of multi-path, jitter and non-linearity of antenna is also less in this architecture. However, since the received signal amplitude is very low, the amplitude of mixer output after self mixing the pulses is extremely low. A number of gain stages are required in order to bring the signal to a detectable level. This in turn increases the power consumption of the circuit

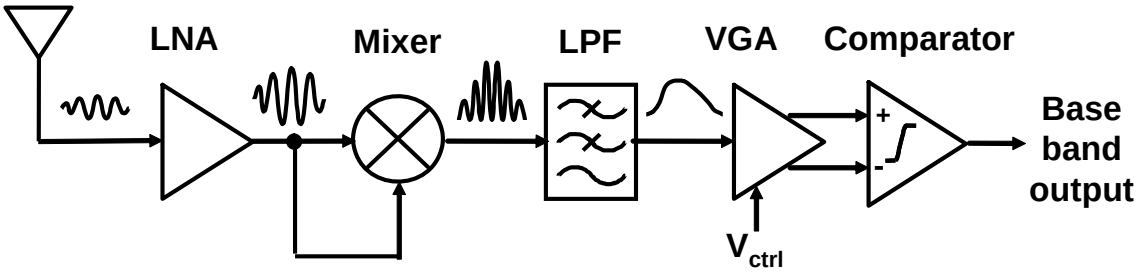

Figure 2.5 Non-coherent receiver architecture.

2.3.3 Coherent Receiver Architecture

As illustrated in Figure 2.6, the coherent receiver typically consists of a template pulse generator and timing controller for controlling the generation of template pulses. Unlike non-coherent architecture, the received pulses are first amplified, then mixed with template pulses and then passed through integrator and comparator to get the original data.

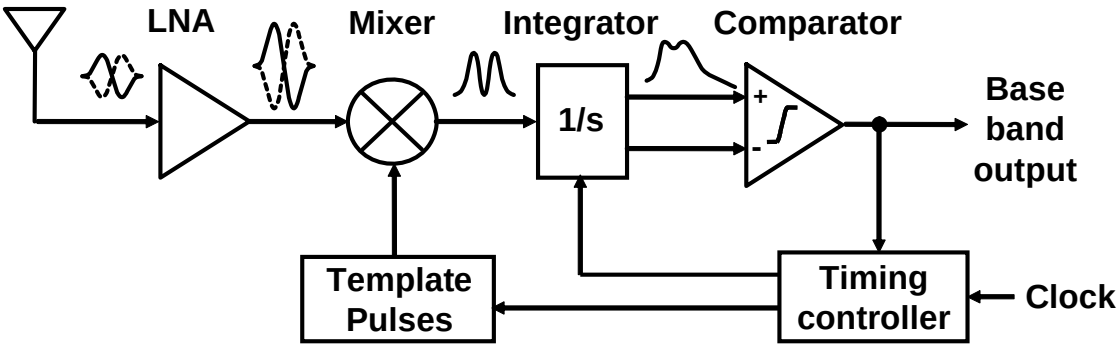

Figure 2.6 Coherent receiver architecture.

In UWB transceiver architectures, noise immunity and BER performance are crucial and coherent architecture has an edge over non-coherent one. Although, coherent receiver architecture is more complex than the non-coherent architecture, in this work, the coherent architecture is chosen in order to achieve higher data rates while keeping the noise and BER low. However, coherent architecture poses some challenges in the design of high speed low power transceivers. Firstly, in coherent architecture, the incoming RF signal is mixed with the template signal (LO) generated locally for demodulation. In order to demodulate the base band data with minimum number of errors, obtaining correlation between RF and LO is critical. Since IR-UWB systems operate at the frequency range of several GHz, timing precision of the order of picoseconds is required in the design of the correlator. As the UWB systems operate at very high data rates, design of a high precision carrier and symbol timing recovery circuit that will operate at data rates of few Gb/s is thus essential. Secondly, the design of analog circuits such as LNA, mixer, integrator and comparator that operate at such high frequency while keeping the power consumption of the receiver to a considerably low level is needed. All these factors pose a major challenge in the design of coherent receiver architecture. Receiver designs in chapter 3 and chapter 4 give solutions to above problems and demonstrate high speed low power IR-UWB receivers.

2.4 On-chip Antenna

Since the primary interest of this research is designing a transceiver circuit to achieve communication within 10 cm of distance, designing an antenna on the chip similar to the

other circuits would be highly cost effective. The targeted applications of the system are portable appliances having very small sizes, the on-chip antenna would not only be of low cost due to fabricated on the CMOS chip but also very effective for chip to chip communication due to its miniature size. The radiation efficiency of on-chip antenna is generally quite low due to dielectric losses and designing a wideband on-chip antenna poses quite a challenge. But considering the cost effectiveness and the shorter distance of communication, this can be a feasible choice.

2.4.1 UWB Antenna Requirements

The allocation of UWB band has created surge of opportunities and challenges to the antenna designers. The fundamental challenge in UWB antennas is achieving wide impedance bandwidth while maintaining high radiation efficiency. Spanning 7.5 GHz, almost a decade of frequency, this bandwidth goes beyond the typical definition of a wideband antenna. UWB antennas are typically required to attain a bandwidth, which reaches greater than 100% of the center frequency to ensure a sufficient impedance match is attained throughout the band such that a power loss less than 10% due to reflections occurs at the antenna terminals.

Apart from a wide bandwidth, linear phase is required for optimum wave reception, which corresponds to a constant group delay. If the phase is linear throughout the frequency range, the group delay will be constant for the frequency range. Constant group delay is required to minimize pulse distortion during transmission. This is an important parameter while considering wideband antennas because it helps to indicate how well a UWB pulse will be transmitted and to what degree it may be distorted or dispersed.

Radiation efficiency is also an important characteristic because it helps to indicate how well a UWB pulse will be transmitted and to what degree it may be distorted or dispersed. Since transmit power of UWB signals is very low (typically below noise floor), a high radiation efficiency is required.

Also, since the primary focus of UWB systems in terms of application is small integrated circuits for portable appliances, the size of the antenna is an important factor. The antenna is required to be physically compact.

2.4.2 Antenna Performance Index

One of the important parameters for measuring performance index of antenna is the transfer characteristic i.e. S_{21} between the receiving antenna and transmitting antenna. Here the transfer characteristic can be defined as the ratio of power given to the input of the antenna from the transmitter side to the power received by the antenna at the receiver side. If we consider the radiation efficiency, the equation of S_{21} can be written as follows.

$$\boldsymbol{S_{21} = -S_{11} + \eta_t - PL + \eta_r - S_{22}}$$

Where c is the speed of light (3×10^8 m/s) and d is the distance between two antennas, which for this research is greater than 5 cm.

If both the transmitter and receiver antennas are identical, their characteristics are same i.e. $\eta_t = \eta_r$ and the above equation for S_{21} becomes

$$S_{21} = 2\eta - PL \qquad \textbf{(2.1)}$$

This S_{21} can be treated as an important characteristic for performance measure of the antenna. Another important measure for antenna performance index is VSWR i.e. Voltage Standing Wave Ratio. VSWR and return loss are both dependent on the measurement of the reflection coefficient Γ. Γ is defined as ratio of the reflected wave V- to the incident wave V+ at a transmission line load as shown in Figure 2.7, this case the load being the antenna.

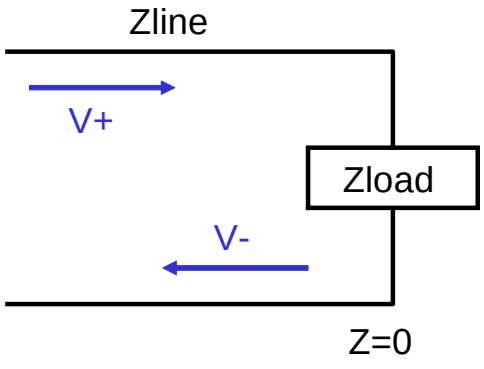

Figure 2.7 Transmission line model.

VSWR measures the ratio of the amplitudes of the maximum standing wave to the minimum standing wave.

Return loss (S_{11}) is another measure of performance index. If reflections between the circuit and the antenna are low, power is delivered efficiently to the antenna. However, when it comes to very small size antenna like on-chip antenna, small reflections are not always considered as good. The reason being the radiation efficiency in case of small antenna is extremely low.

Radiation efficiency is determined by the ratio of the radiated power, P_{rad} to the input power at the terminals of the antenna,

$$\eta = \frac{P_{in}}{P_{out}} = \frac{R_r}{R_r + R_L} = \frac{1}{1 + \frac{R_L}{R_r}} (< 1) \qquad \textbf{(2.2)}$$

(R_r: Radiation resistance, R_l: Loss resistance)

Because radiation resistance of antenna is proportional to electrical area of antenna, radiation resistance of small antenna is low. As a result, radiation efficiency is also low. With high antenna loss and low radiation efficiency, antenna cannot radiate sufficiently even if the input power is high and reflections are negligible.

The minimum required value of S_{21} for the antenna can be calculated with the help of link budget. Link budget is calculated using addition and subtraction of gain and losses of individual blocks of the whole system. Broadly, link budget is the estimation of unknown values of the parameters of the individual blocks in the system. The link budget equation can be written as follows.

$$G_r = -(P_t + G_t - PL - N - NF - S - M) \qquad \textbf{(2.3)}$$

Where,

M : Link Margin[dB]

P_t : Input power of the pulse input give to the antenna[dBm]

G_t : Transmitter antenna gain[dB]

G_r : Receiver antenna gain[dB]

PL : Path loss[dB]

N : Average noise power per transmitted bit

NF : Noise Figure on receiver side

S : Required SNR at the last stage of Receiver

Here, the value of P_t+G_t is limited by the FCC mask for the permitted maximum radiated power which is -41.3 dBm/MHz. Since the bandwidth is 4 GHz, the total value becomes

$$\begin{aligned} &\mathbf{10\log_{10}(4\times10^{3})\approx 38.0} \\ &\boldsymbol{P_t + G_t = -41.3[dBm/MHz] + 38.0[dB\cdot MHz]} \\ &\mathbf{= -3.3[dBm]} \end{aligned}$$

The path loss for 10 cm distance becomes

$$\begin{aligned} 20\log_{10}\left(\frac{4\pi f_c d}{c}\right) &= 20\log_{10}\left(\frac{4\pi\times 8\times10^{9}\times10\times10^{-2}}{3\times10^{8}}\right) \\ &\approx 30.0[dB] \end{aligned}$$

Average noise power per transmitted bit is fixed for a fixed bandwidth and can be taken as

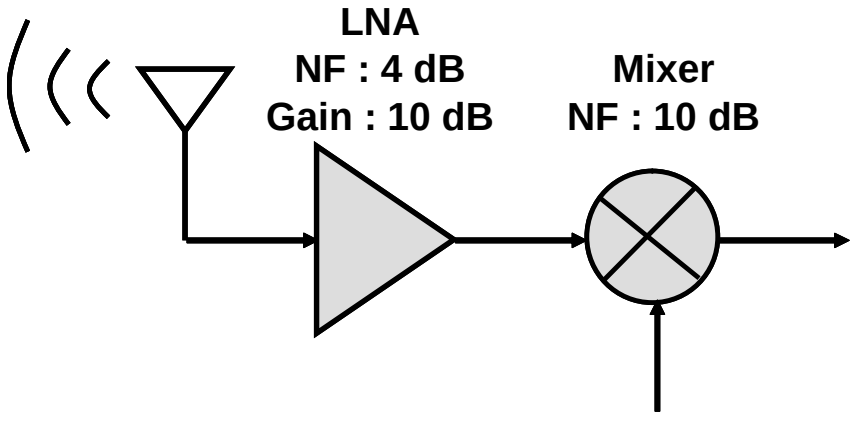

Figure 2.8 Receiver front-end.

$$\begin{aligned} N &= -174 + 10\log_{10} B \\ &= -174 + 10\log_{10}(4\times 10^{9}) \\ &\approx -78.0[dBm] \end{aligned}$$

(B:Bandwidh)

For noise figure calculation, the front end of the receiver can be considered as shown in Figure 2.8 below Noise figure for this kind of multiple stage receivers can be calculated by Friis equation. If NF_1 and NF_2 are noise figures for 1st and 2nd stages respectively and G_1 is the gain of the first stage, the total noise figure can be calculated by

$$NF_1 + \frac{NF_2 - 1}{G_1} \qquad \textbf{(2.4)}$$

Therefore, the total NF can be calculated as 4.9dB.

The value of other parameters can be taken as follows.

Link Margin M : 6dB

Required SNR at the last stage of Receiver, S : 7dB

With the above values, the receiver antenna gain can be calculated using equation 5-3 as follows.

-	P_t+G_t	-3.3dBm
+	PL	30.0dB
+	N	-78.0dBm
+	NF	4.9dB
+	S(On-Off Keying)	7.0dB
+	M	6.0dB
	G_r	-16.8dB

S_{21} can be represented as $G_t + G_r$ - PL. Since the transmitter and receiver antennas are same, $G_t = G_r = G_a$, equation for S_{21} becomes $2G_a$ - PL. Therefore, the required S_{21}within 10cm distance comes out to be -63.6dB.

2.4.3 Classification of Antennas

There are several types of antennas commercially available and new types being researched. Depending on the application and the characteristics, on-chip antennas can be classified into three broad categories.

1. Dipole Antenna

Dipole antenna is very commonly used antenna where space constraints are not strict. It consists of two elements facing away from each other. Generally, the length of each element is λ/4 where λ is the wavelength of the transmitting wave. The total length of the antenna is λ/2.

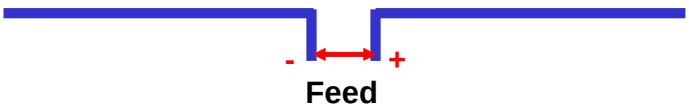

Figure 2.9 Dipole antenna.

Usually, the antenna elements are straight as shown in Figure 2.9, but in some cases, the elements can be bent for the area adjustment. The antenna is fed in the center by the signal.

2. Monopole antenna

Monopole antenna is the simplest practical antenna. Unlike the dipole, it consists of a single element mounted vertically on the ground plane. This way, ground plane acts as a mirror image of the element above ground and the monopole can be seen as a dipole antenna. As shown in Figure 2.10, monopole antenna can be fed from the ground. Since monopole consists of single element, the antenna length can be λ/4: half of that of dipole.

This way, the implementation area of monopole can be half of that of dipole. But the performance of monopole is inferior to that of dipole. There is a tradeoff between the length of the antenna and its performance. Antenna gain is an important factor in comparing performance of the antenna. The gain can be defined by following equation.

$$G = 4\pi A_e / \lambda \qquad (2.5)$$

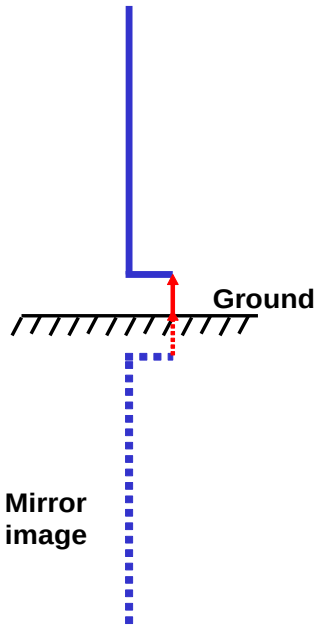

Figure 2.10 Monopole antenna.

Where λ is the wavelength and A_e is aperture area of antenna. Aperture area is the area of the antenna element that contributes to the actual radiation. When the antenna is radiating, the current distribution in the antenna is like that of a standing wave. If the maximum amplitude of current distribution of the standing wave is assumed constant, the area of the antenna in which this current flows is called aperture area [13]. In case of like dipole or monopole which have a linear element, the unit is changed to length and this term is called effective length of the antenna as shown in Figure 2.11.

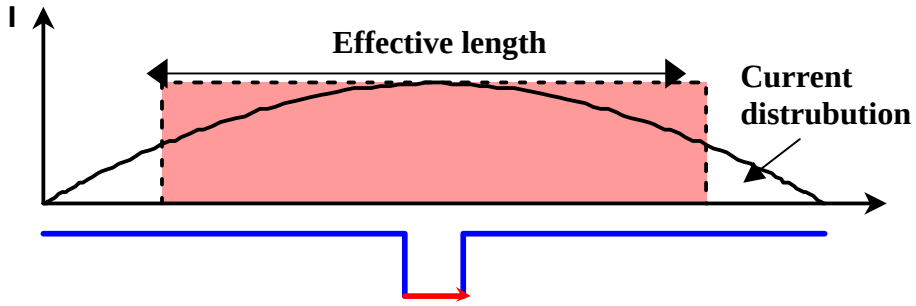

Figure 2.11 Concept of effective length of the antenna.

Aperture length is proportional to the total length of the antenna. Hence, if the length of the antenna is reduced, its aperture length also reduces causing reduction in performance.

3. Loop antenna

Loop antenna consists of a single element rounded to form a loop. Unlike monopole or dipole antenna, the element in loop antenna is shorted. Consequently, loop antenna can be considered as a transmission like with short-circuited ends. When the total length of the loop is equal to the wavelength, standing waves are formed on the element and the antenna radiates similar to that of monopole or dipole. Since the perimeter of the loop antenna is equal to the wavelength, its element length is twice or four times more than that of dipole or monopole antenna. This means, the performance of loop antenna is superior to that of dipole or monopole at the cost of higher area.

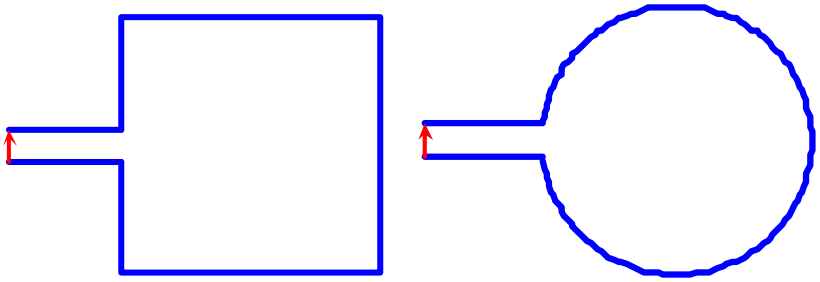

Figure 2.12 Loop antenna.

The selection of one antenna among the three results in a trade-off since each type of antenna has its own advantages and disadvantages. Dipole and monopole antennas are best suitable for on-chip implementation since they take less chip area compared to loop antenna resulting in lower cost.

2.4.4 Wavelength-Shortening Effect

One important factor that needs to be considered while designing on chip antenna is wavelength-shortening effect. There is a dielectric layer between the signal line and ground. In order to reduce the velocity of electromagnetic waves in the dielectric medium, the signal line placed in the dielectric medium is seen longer by the signal compared to

that of vacuum. The appearance of the metal line in dielectric medium can be considered as

$$\frac{1}{\sqrt{\varepsilon_r}} \qquad \textbf{(2.6)}$$

(ε_r : dielectric constant).

This is called wavelength-shortening effect. The dielectric constant of the SiO_2 layer used as an insulator in most of the CMOS LSI chips is 3.9. Hence, on-chip antenna can be accommodated in half the size compared to the antennas that are mounted in air or vacuum.

Table 2-I Wavelength shortening effect.

Frequency	Loop antenna perimeter when designed in vacuum	Loop antenna perimeter when designed in SiO_2
8 GHz	37.5 mm	18.99 mm

While considering the system operating in the frequency band of 6-10 GHz, the center frequency of 8 GHz is chosen as the pulse generator frequency. The wavelength of 8 GHz frequency is 37.5 mm. For the dipole antenna the length becomes λ/2 and if the wavelength shortening effect is taken into account, the required on-chip length for the dipole antenna turns out to be 9.49 mm.

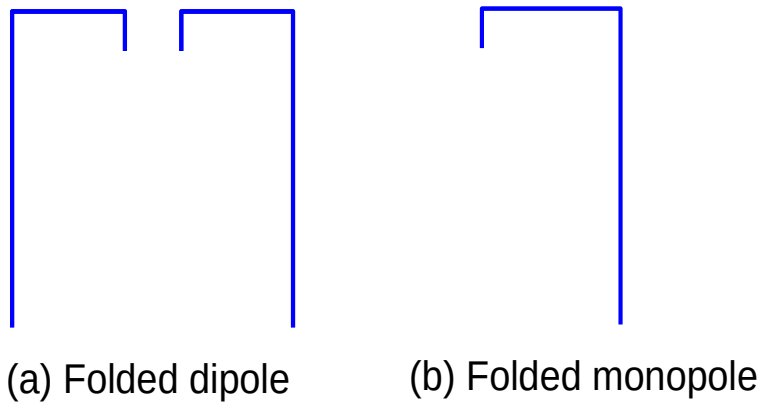

Figure 2.13 Dipole and monopole with folded element.

For the chip size of 2.8 mm × 2.8 mm, this length also seems very difficult to realize, but if the element of the dipole is bent as shown in Figure 2.13, the 9.49 mm dipole antenna can be realized on the chip. Similarly, monopole antenna, although half of the size of the dipole, needs to be bent in order to fit on the chip.

2.4.5 Antenna Element Structure

Although, not much research has been done on the use of antennas integrated in silicon chips, a few papers have reported the use of on-chip antennas [14-16]. Since the implementation area on the chip is limited, different antenna topologies were proposed to maintain the same performance while reducing the size on chip. For the convenience of measurement, three kinds of dipole antennas were designed previously in this research namely, simple folded dipole, short-L type dipole and meander type dipole as shown in Figure 2.14.

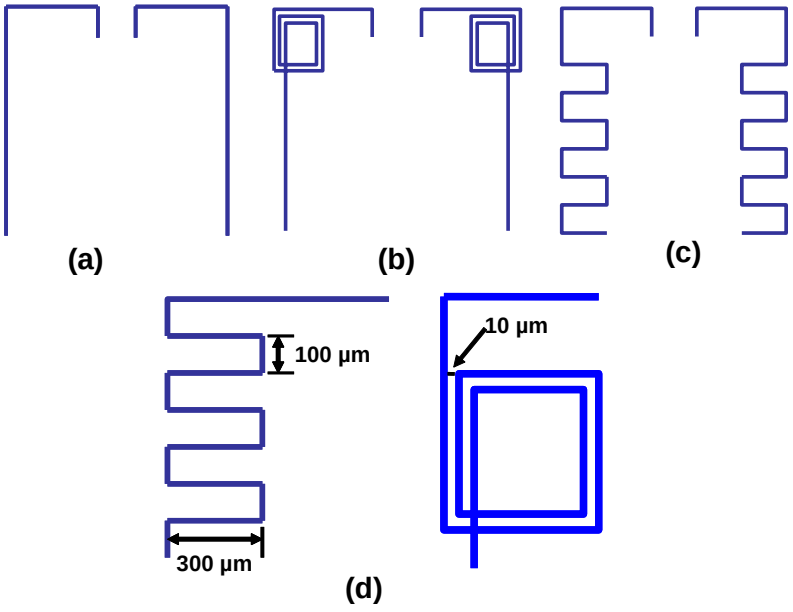

Figure 2.14 Antenna structures (a) Simple folded dipole, (b) Short-L dipole, (c) Meander dipole, (d) Bent structure of Meander and short-L.

The parameters of the folding elements for Meander and Short-L type dipole were decided as shown in Figure 2.14(b), so that the antennas are accommodated on the 2.5 square mm chip. Meander dipole has the element bent in a zigzag way. For short-L dipole,

the antenna element is folded like that of an inductor. All the three types of antennas were simulated in a 3-D simulator to see their performance at the frequency of 8 GHz and communication distance of 30 cm. Figure 2.15 shows the simulated S21 of the three types of dipole antennas in the frequency range of 6 -10 GHz.

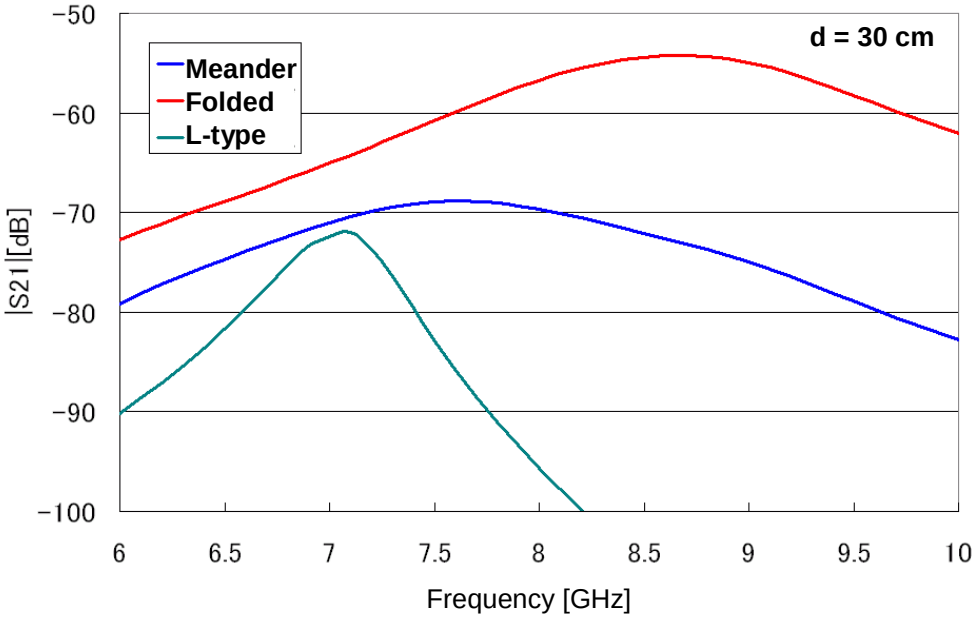

Figure 2.15 Simulated S_{21} of the three antenna structures.

From simulation, it was observed that the simple folded type dipole has the highest gain amongst the three topologies. To verify the simulation results, a test-chip was fabricated with all the three antenna topologies. One end of the antenna was connected to GSGSG pads so that the antenna characteristics can be measured using probes. Figure 2.16 shows the chip micrograph with the three antenna topologies. The effect of metal line placed in the proximity of on-chip antenna was simulated with the 3-D magnetic solver. From simulation it was found out that a minimum distance of 150 µm needs to be kept between the antenna element and dummy metals in order to avoid the effect of dummy metals on the antenna. Due to design rule requirements, the dummy metal was placed near the on-chip antenna. However, in the next implementation of on-chip antenna described in chapter 3, the dummy metal placement is kept 150 µm away from the antenna element.

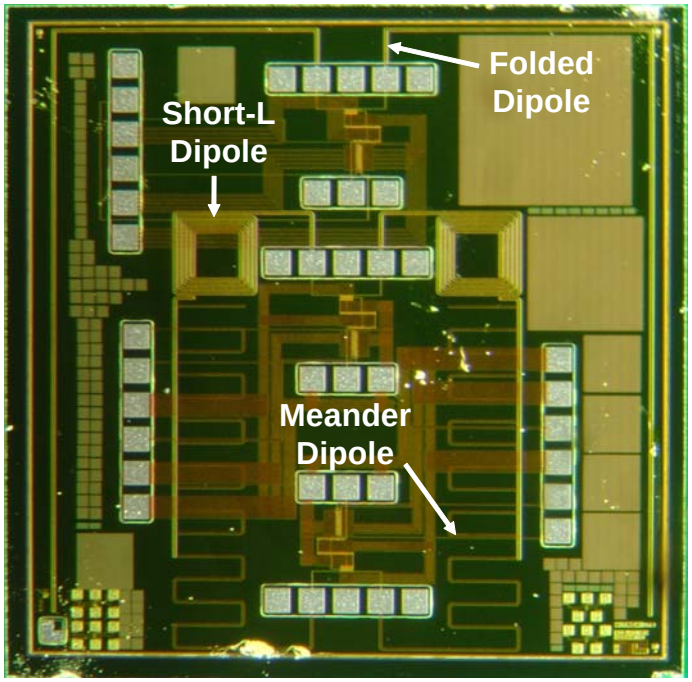

Figure 2.16 Chip micrograph with the three antennas.

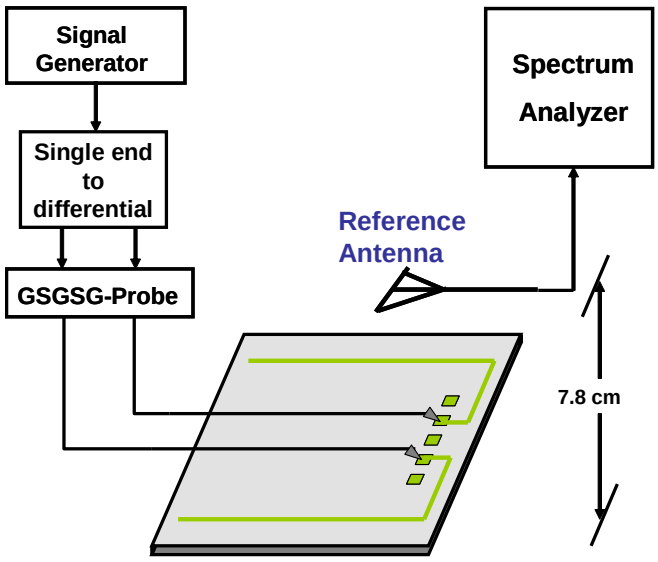

Figure 2.17 Antenna measurement setup.

The characteristics of the three antennas were measured for a short distance of 7.8 cm. Since no signal generator is placed on chip, the frequency of 8 GHz was given to each antenna from a signal generator with the help of GSGSG probes. Figure 2.17 shows the

measurement setup. The 8 GHz single ended signal was converted to differential signal using balun before being fed to the probes. A test antenna was kept at a distance of 7.8 cm from the chip and the signal from the on-chip antenna was captured by the test-antenna and given to the spectrum analyzer. From the observed amplitude of received signal on spectrum analyzer, the S_{21} of the on-chip antenna was calculated.

The measured S_{21} of the three antennas is as shown in Figure 2.18. Since the measurement was not carried out in an anechoic chamber, the measured characteristic of antenna shows irregularities due to the influence of surrounding environment as well as leakage from probes. Due to the limitation in the measuring environment, distance of 7.8 cm was set up, in which case, the antenna gain requirement comes to -65.1 dB.

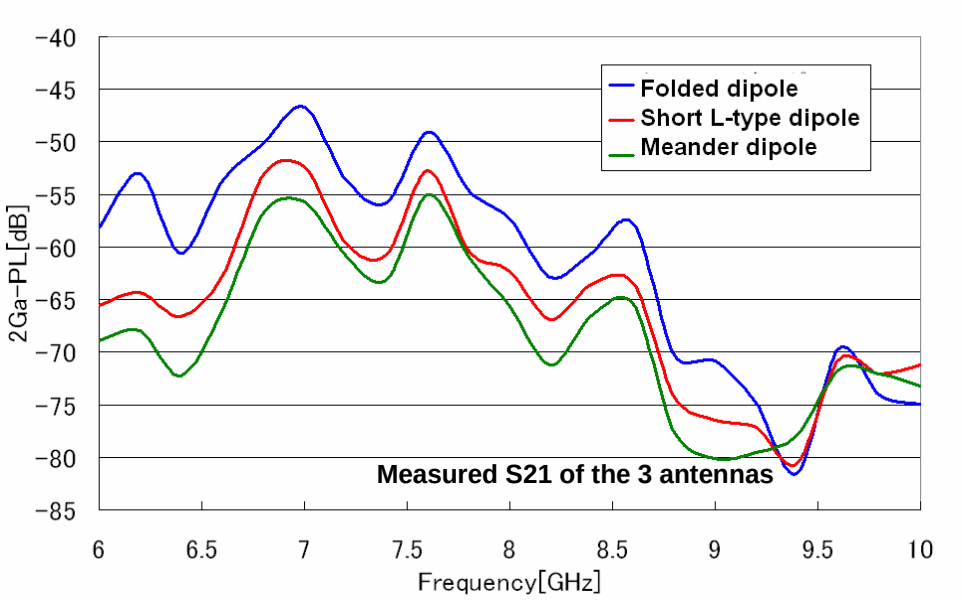

Figure 2.18 Measured S21 of the three antenna structures.

Meander and short-L type dipole antennas have the same element length but occupy less area compared to that of simple folded dipole. However, measured results confirm the observation from simulated results that the folded dipole has higher efficiency than Meander and short-L type dipole.

2.5 Conclusion

Design considerations for high-speed low-power IR-UWB transceivers were presented. Steps in the design flow such were discussed along with different modulation schemes and IR-UWB transceiver architectures. Taking various factors into account such as transceiver complexity, BER performance, it is observed that the coherent architecture with BPSK modulation scheme are best suitable for high-speed low-power transceiver design. A study on feasibility of on-chip antenna for the operation in UWB band was presented. Various antenna topologies and structures were studied. From simulation and measured results, it was observed that monopole antenna is best suitable for 6-10 GHz operation.

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Chapter 3 Design of 750 Mb/s 12 pJ/b 6-to-10 GHz Transceiver

3.1 Introduction

The next generation wireless handheld devices demand high data rates for the transfer of multimedia content at low power. With UWB systems developed with data rates crossing few hundred Mb/s mark, energy consumption plays a key role in deciding their performance. A fair number of works [1-13] have attempted to design either high speed or low power transceivers. However, as the power consumption and data rate present a tradeoff in the transceiver design, most of the works that report data rates higher than 100 Mb/s have energy consumption of the order of 50 - 100 pJ/b and those with the low energy consumption have data rates of the order of few Mb/s. While the standards for wireless USB interface and wireless 1394 are already on the verge of development, a transceiver with data rates of the order of few hundred Mb/s and energy consumption of tens of pJ/b is highly desired for short distance wireless communication applications.

Also, a transceiver with an embedded antenna on a single chip can be a cost effective solution for short distance communication applications, eliminating the need for external transmission line connections and expensive packaging. The usage of on-chip antenna can enable the realization of a low cost single chip solution.

This chapter describes design of an IR-UWB transceiver to achieve data rate of 750 Mb/s for short distance communications within 10 centimeters. The transceiver is designed to operate in the frequency band of 6 - 10 GHz. The chapter demonstrates a novel pulse generator circuit which incorporates the functionality of modulator and pulse shaping filter to achieve extremely low power operation. The transceiver operation is verified with simulation while the transmitter chip is fabricated and tested to achieve data rate as high as 750 Mb/s and energy consumption as low as 12 pJ/b. The chapter also describes the design and fabrication of an embedded on-chip antenna and its performance within 6-10 GHz band.

3.2 Motivation for using 6-10GHz Band

The allocated bandwidth and transmitted power for UWB communication differs in each country. However, the allocated it can be divided into two major bands, a 3-5GHz band and 6-10GHz band as shown in Figure 3.1.

Since the bandwidth of 6-10GHz band is twice that of 3-5GHz band, the time domain pulse width for the pulse utilizing high band is half that of lower band. As the pulse for the 6-10GHz is smaller in time domain, more number of pulses can be accommodated in the given time period compared to the 3-5GHz pulses and higher data rate can be achieved.

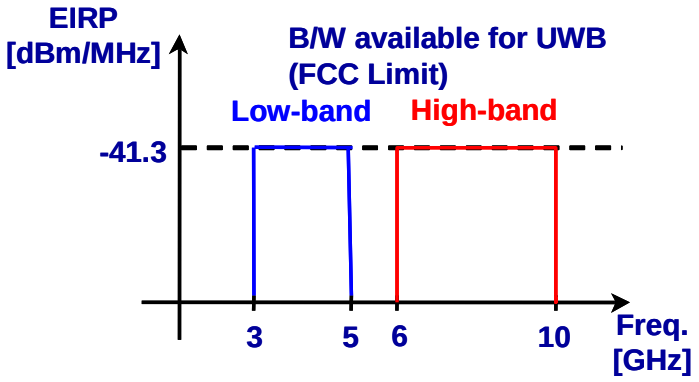


Figure 3.1 UWB band classification.

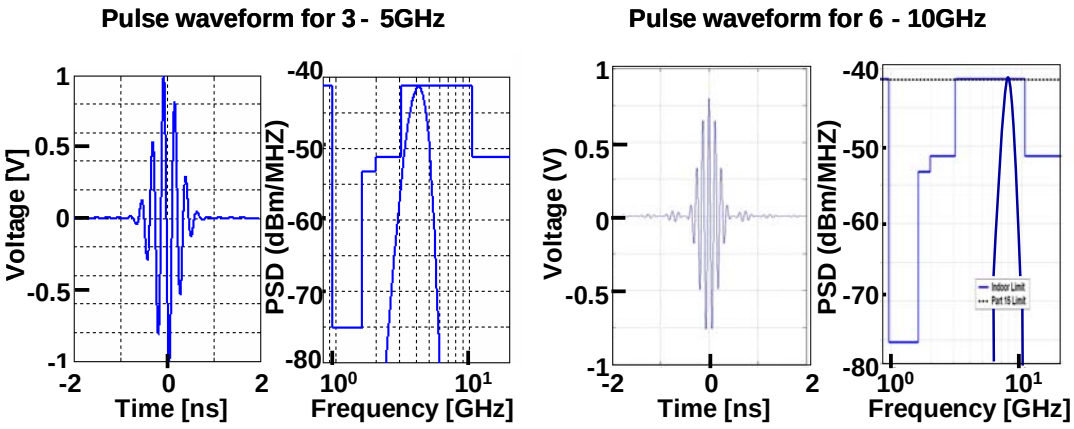


Figure 3.2 Time domain waveform of pulse and its frequency domain spectrum for low and high bands.

The 6-10GHz pulse shape and its spectrum is shown in Figure 3.2. Another reason for choosing 6-10GHz band is to avoid interference from wireless LAN which utilizes the 5GHz band. Furthermore, with the use of the 6-10 GHz band, the use of an on-chip antenna is possible as the wavelength of the pulse is shorter than 3-5 GHz band.

3.3 Transceiver Architecture

IR-UWB being carrier-less communication, the design of the transceiver system involves two important factors - shape of the pulse and modulation scheme. Choosing an efficient modulation technique and an optimal pulse width for the transmitting pulse is not only important in achieving the maximum performance from the transmitter, but also crucial in the design of various blocks in the receiver. The following sections explain in detail the modulation scheme and design of the pulse for the proposed transceiver.

3.3.1 Modulation Scheme

In the proposed transmitter architecture, BPM scheme is employed because it offers several advantages over the other two schemes. The required SNR of PPM is larger than that of BPM to attain the same BER in a multi-path environment. Therefore, the output power of BPM can be lower than that of PPM [5]. Moreover, BPM is superior to PPM in terms of BER performance because in PPM, the data is sent in the form of time-shifted pulses. In a multipath environment, delayed signals come at various times and the receiver cannot distinguish which is real one. This causes false detection of data degrading BER performance of the PPM system [5]. Furthermore, for PPM, a 2x data rate clock is required while for BPM 1x data rate clock is sufficient. However, BPM requires coherent receiver architecture for signal recovery, which is more complex than the non-coherent architecture required by OOK or PPM. In UWB transceiver architectures, noise immunity and BER performance are crucial and coherent architecture has an edge over non-coherent one. In this work, the coherent detection scheme is chosen in order to achieve higher data rates while keeping the noise and BER low.

3.3.2 Pulse Design

The transmitted pulse in IR-UWB systems can be either a Gaussian monocycle pulse or an impulse train. Gaussian monocycle pulse is more popular and used in many IR-UWB transceiver systems [6-8]. Due to its wider spectrum, it can be suitable for the higher data rate applications. However, it requires additional pulse shaping circuits like RF filters to accommodate the pulse in the allowed spectral mask of FCC. On the other hand, the impulse train acts somewhat like a carrier and can be used for the purpose of modulation and transmission. In the proposed transmitter, we have used impulse train utilizing bi-phase modulation. Since the time domain pulse width decides its frequency spectrum, it is important to design a pulse that makes optimal usage of the available spectrum within the limits imposed by FCC. To decide the optimal pulse width, pulses with different widths were simulated in Matlab and their corresponding frequency spectra were observed. Figure 3.3 shows the block diagram of simulation schematic of the transmitter in Matlab.

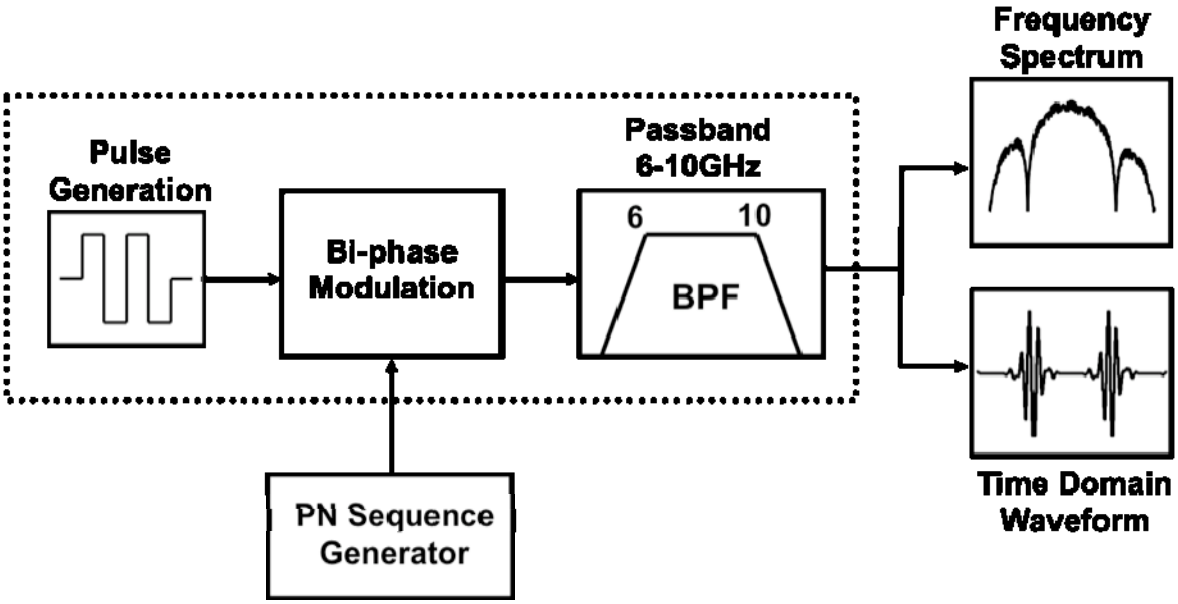


Figure 3.3 Matlab simulation schematic for the transmitter.

Bi-phase modulated pulses are generated which are then passed through a band pass filter with a pass-band of 6-10 GHz. The frequency spectra of the generated pulses are obtained by taking FFT of the time domain signals. The band pass filter shown in the

simulation model is not used in the actual transmitter implementation since functions of all the blocks shown within the dotted box are incorporated in the pulse generator circuit itself. Simulation was carried out for three different pulses with widths of 0.25 ns, 0.5 ns, and 1 ns with a pulse repetition frequency of 800 MHz. Figure 3.4 shows their time domain waveforms. The pulses were generated such that the peak power spectral density (PSD) of each pulse in the frequency domain remained the same and below the FCC spectral emission mask as illustrated in Figure 3.5. It can be observed that there is a clear tradeoff between the pulse width and the pulse peak amplitude. The 1 ns pulse occupies bandwidth of 2 GHz and is not suitable for high pulse repetition rates.

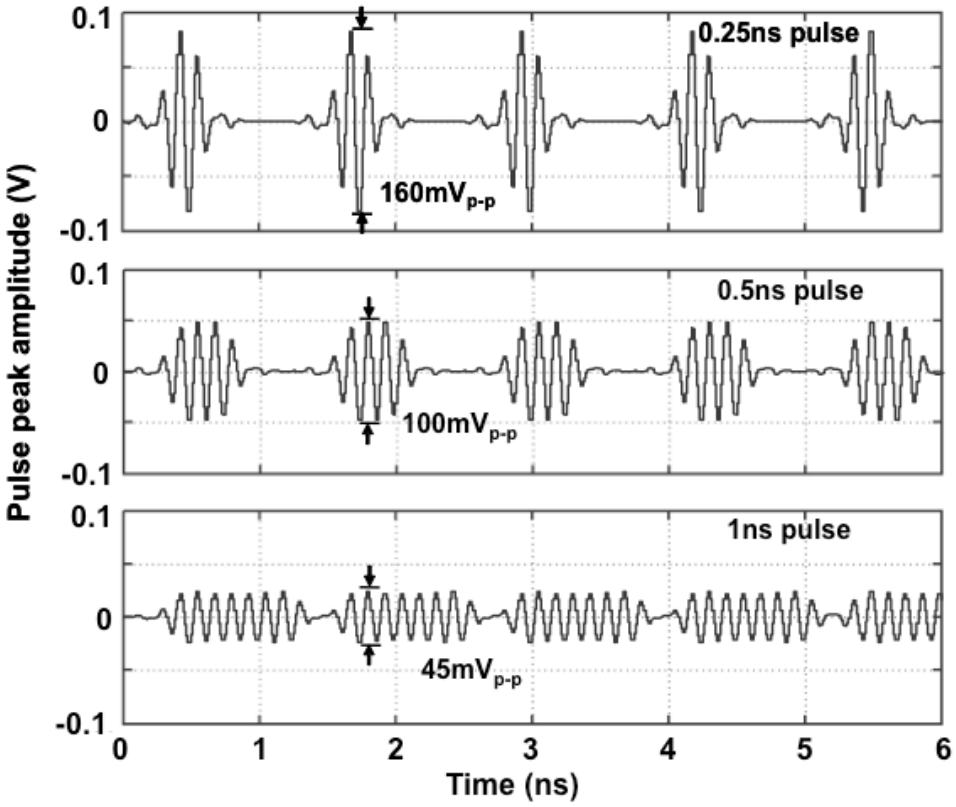


Figure 3.4 Time domain waveforms of the simulated pulses for different pulse widths (when peak power spectral density of all pulses are kept at same level).

Also, its peak-to-peak amplitude is limited to 45 mV. On the other hand, the 0.25 ns pulse is short enough to achieve the repetition rate of over 1 Gbps and has peak-to-peak amplitude of 160 mV. But it occupies almost 8 GHz of bandwidth and can interfere with the 802.11 wireless LAN at 5 GHz. Also, due to its large bandwidth wideband matching

circuits are necessary. The 0.5 ns pulse with 4 GHz of bandwidth achieves optimal balance between available spectrum usage and peak-to-peak amplitude. Therefore pulse width of 0.5 ns was chosen in the proposed pulse generator design.

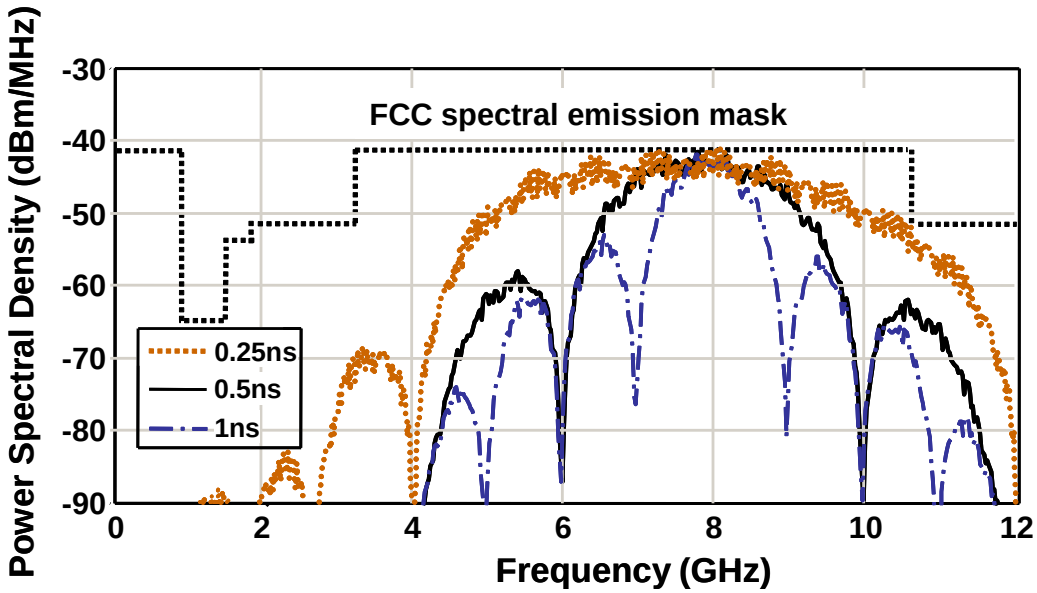


Figure 3.5 Frequency spectrum of pulses with different pulse widths.

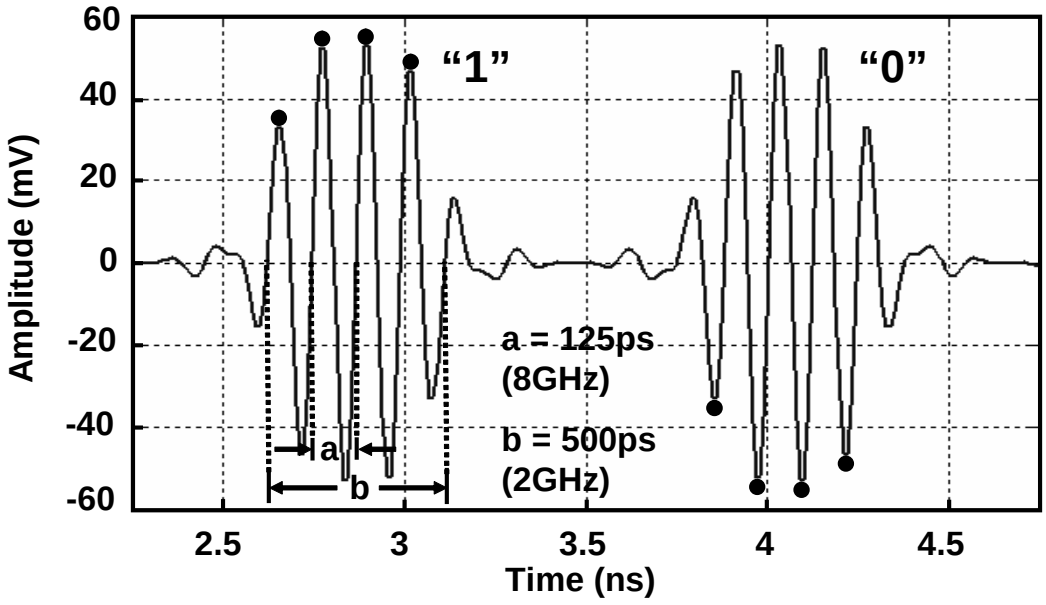


Figure 3.6 Time domain waveform and parameters of the proposed pulse.

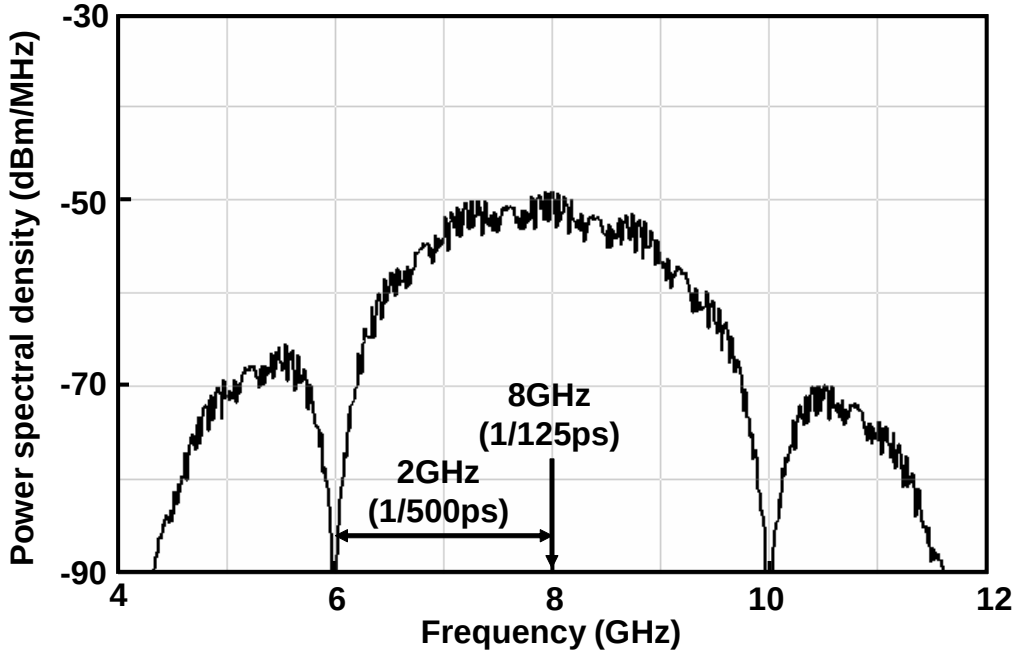


Figure 3.7 Frequency spectrum of the proposed pulse.

Figure 3.6 and Figure 3.7 depict the design of proposed pulse and its simulated power spectral density (PSD) using Matlab respectively. The pulse consists of four cycles of 125 ps duration each, corresponding to a total duration of 500 ps and center frequency of 8 GHz. The center frequency of 8 GHz was chosen for two reasons: first, to avoid interference with wireless LAN around 5GHz and second, to fully utilize the 4GHz bandwidth within the 6-10 GHz band. The 500 ps pulse duration corresponds to ±2 GHz of bandwidth around the center frequency of 8 GHz which can be observed from the simulated power spectrum of the pulse in Figure 3.7.

3.3.3 Transmitter Architecture

In order to achieve the low power consumption, the transmitter architecture needs to be as simple as possible. Figure 3.8 depicts the conventional IR-UWB pulse generator (PG) architecture [6]. As explained in section 2.3.1, the pulse generator uses various blocks for generation and shaping of the UWB pulse. An oscillator generates a sine wave signal which is used as a center frequency. The sine wave is passed through a raw impulse forming block, a modulator and a pulse shaping filter to generate a base band

Gaussian impulse train , which is then mixed with the oscillator signal to generate the UWB pulse.

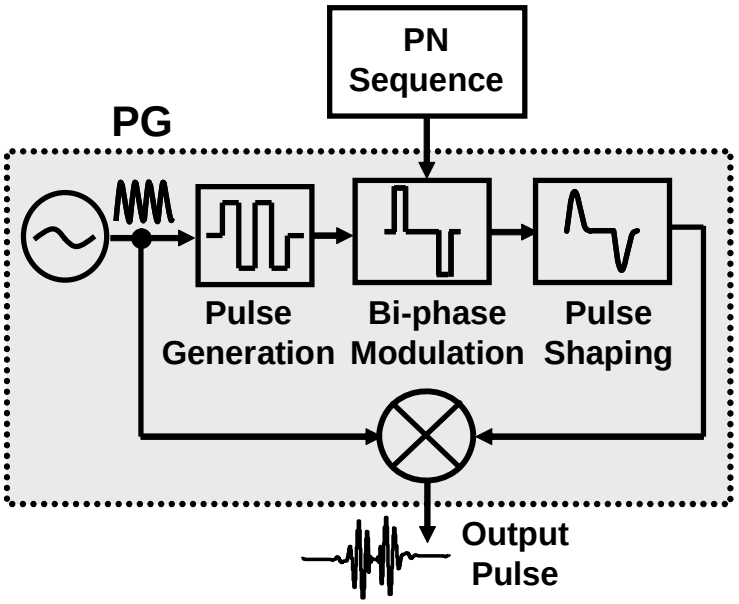


Figure 3.8 Conventional IR-UWB transmitter architecture.

This approach uses many blocks to generate a UWB pulse which results in more power dissipation. Also, the design of analog circuits such as mixers and filters that operate at such high frequencies is a tedious task. If all the functions of pulse generation, modulation and shaping are combined in one block, the power consumption of the whole transmitter can be reduced drastically resulting in simplicity of architecture. This work proposes such pulse generator circuit. Figure 3.9 shows the block diagram of the proposed transmitter. Two transmitter architectures are proposed; one with an external antenna and the other with embedded on-chip antenna. The architecture with external antenna is very simple and consists of a pulse generator connected directly to an external antenna as depicted in Figure 3.9(a). Based on the data and clock signals given externally, the pulse generator generates UWB compliant BPSK modulated pulses of 500 ps duration with a center frequency of 8 GHz. Unlike the conventional pulse generator, all the functionalities of base band pulse generation, modulation and pulse shaping are incorporated in one single pulse generator (PG) circuit. This makes the transmitter

architecture very simple resulting in extremely low power consumption. The operation of the pulse generator is explained in detain in circuit design subsection.

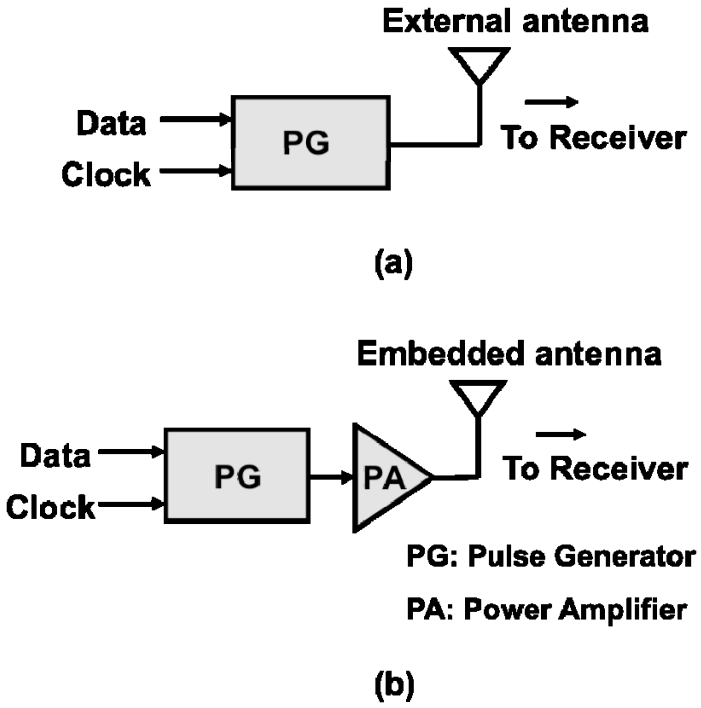


Figure 3.9 Transmitter architecture, (a) with external antenna, (b) with on-chip antenna.

If a highly efficient external antenna is used, the need for power amplifier is eliminated. The embedded on-chip antenna on the other hand, has a low efficiency due to the dielectric substrate losses. The input signal to the on-chip antenna must be amplified in order to achieve communication over the same distance as that with the external antenna. For this purpose, a power amplifier (PA) is added to drive the embedded antenna as shown in Figure 3.9(b). In this work, performance of both the transmitters, using embedded antenna and the external antenna is evaluated.

3.3.4 Receiver Architecture

As discussed in section 3.2.1, a coherent receiver architecture was chosen for the proposed transceiver. Also, the pulse design requires the receiver to have a coherent architecture. Figure 3.10 shows the receiver architecture.

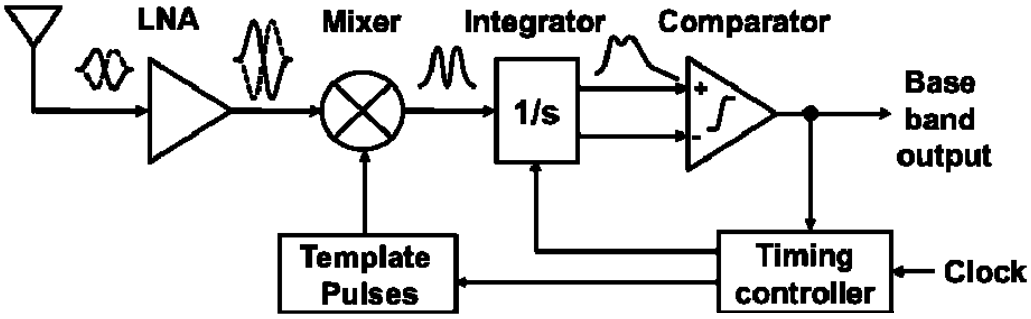


Figure 3.10 Coherent receiver architecture.

The incoming BPSK modulated RF data amplitude is very low. It is amplified with the LNA and then passed to the coherent mixer for demodulation. The incoming BPSK modulated pulses are multiplied with the replica pulses generated locally by the replica pulse generator. The mixed signal contains positive or negative peaks depending on the polarity of the input signal. It is then passed through the integrator, which integrates the input data according to the time constant. The output of integrator is connected to comparator, which samples the input. The decision of the polarity of output is made according to the threshold set in the comparator. The output of the comparator is the demodulated base band data.

Although the receiver architecture looks very simple, the design of each block poses several challenges for high speed low power design. Power hungry components such as LNA, mixer and timing controller need to be carefully designed such that they consume minimum amount of power. Also the LNA and mixer need to operate over a wide bandwidth of 6 – 10 GHz. The design of each block in the receiver is further elaborated in the circuit design subsection.

3.4 Circuit Design

3.4.1 Pulse Generator Design

Pulse generator is the foremost essential block of the transmitter. Figure 3.11 depicts the schematic of the all-digital pulse generator. As described in section 3.3.3, the functionalities of pulse generation, modulation and shaping are all performed using the

single circuit. Clock and data signals are given directly to the pulse generator (PG) which generates the bi-phase modulated pulses of 500 ps duration and 8 GHz center frequency.

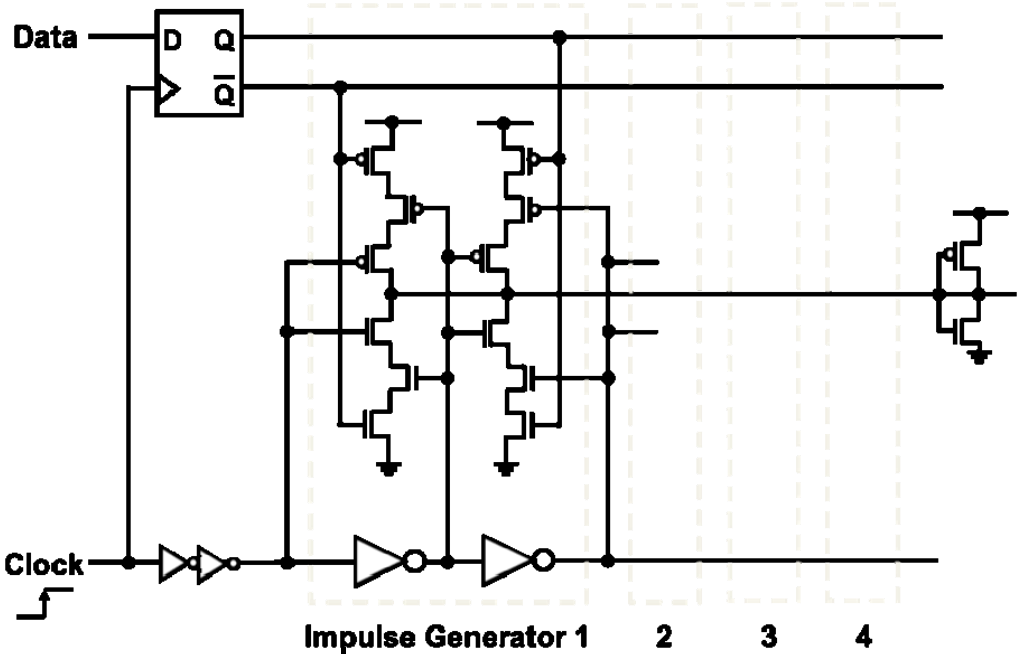


Figure 3.11 Schematic of the proposed pulse generator.

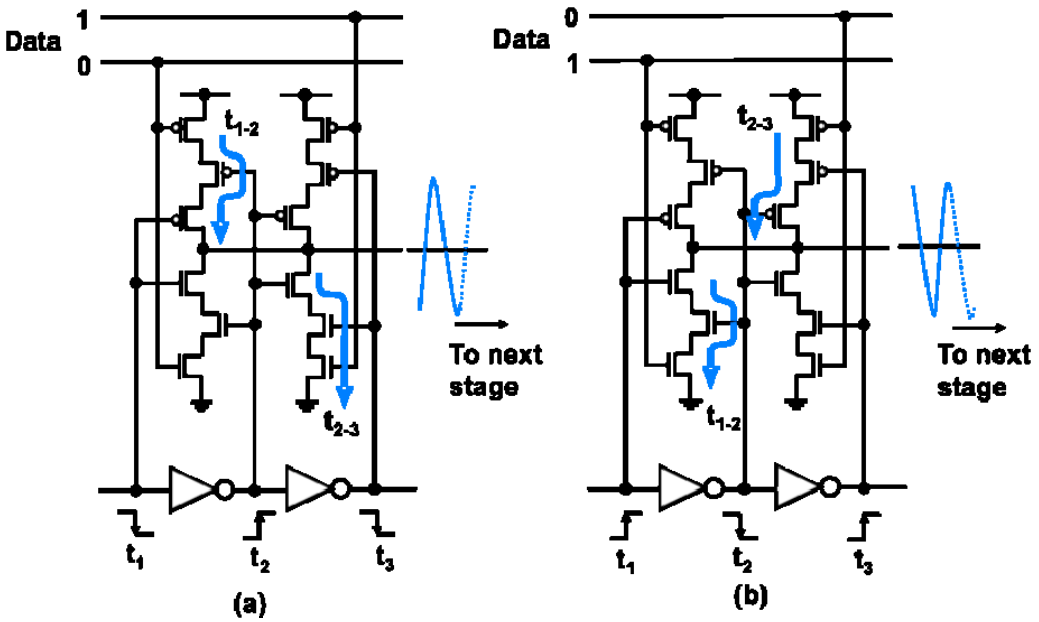


Figure 3.12 Operation of single stage of PG when (a) Data is '1', (b) Data is '0'.

Four Impulse Generator (IG) cells are concatenated to form a chain. Each IG cell generates a 125 ps monocycle impulse which when combined together form the output pulse. The IG cell is comprised of six PMOS and NMOS transistors each, forming an upper and a lower part. When all the transistors in the upper part are on, the output voltage is connected to VDD or pulled up generating the positive peak of the impulse.

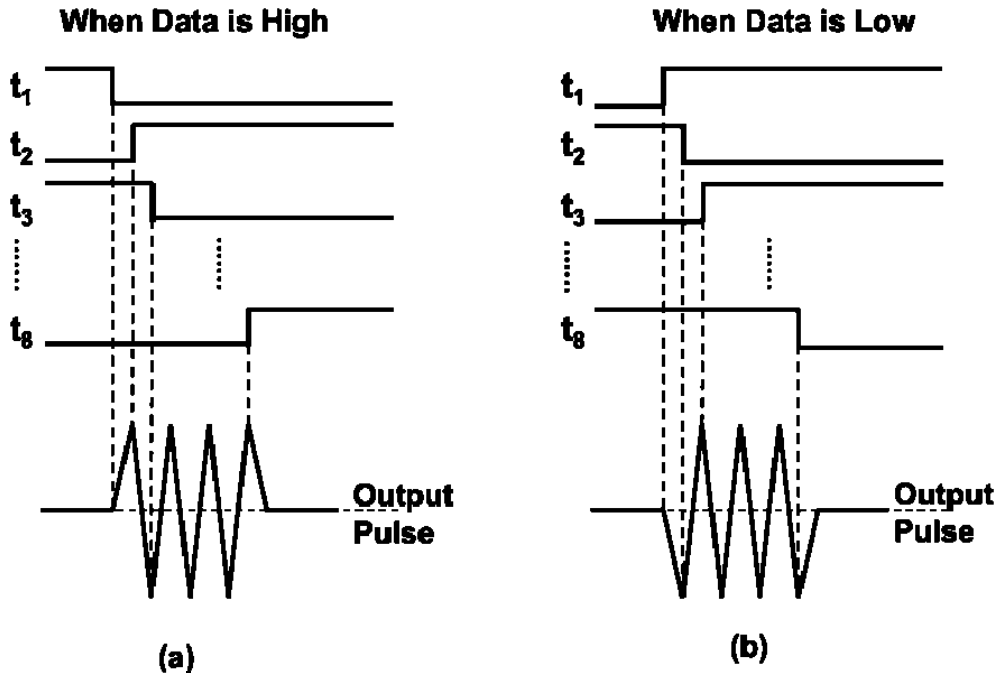


Figure 3.13 Pulse generation timing waveform (a) Data '1' case, (b) Data '0' case.

Similarly, when all the transistors in the lower half turn on, the output is pulled to ground generating the negative peak of impulse. The switching of the transistors in these two parts is controlled by the combination of incoming clock and data signals. Each IG cell consists of two inverters, each providing the necessary delay of 62.5 ps. The lower and upper parts of the IG cell are again divided into two parts, each part operating on the rising and falling edge of the clock to generate bi-phase modulated pulses. The delay time of the inverters and the pulse center frequency in turn, can be controlled by changing the bias current of inverters and is compensated over device fluctuations and temperature/voltage changes.

The operation of the pulse generator is explained in detail in Figure 3.12. When the data is “1”, the upper left transistors of the IG cell are turned on at falling edge of the

clock and the output is pulled to VDD. As the clock passes through the first inverter, the diagonally opposite path of the IG cell turns on and at the rising edge of the clock, output is pulled down to ground.

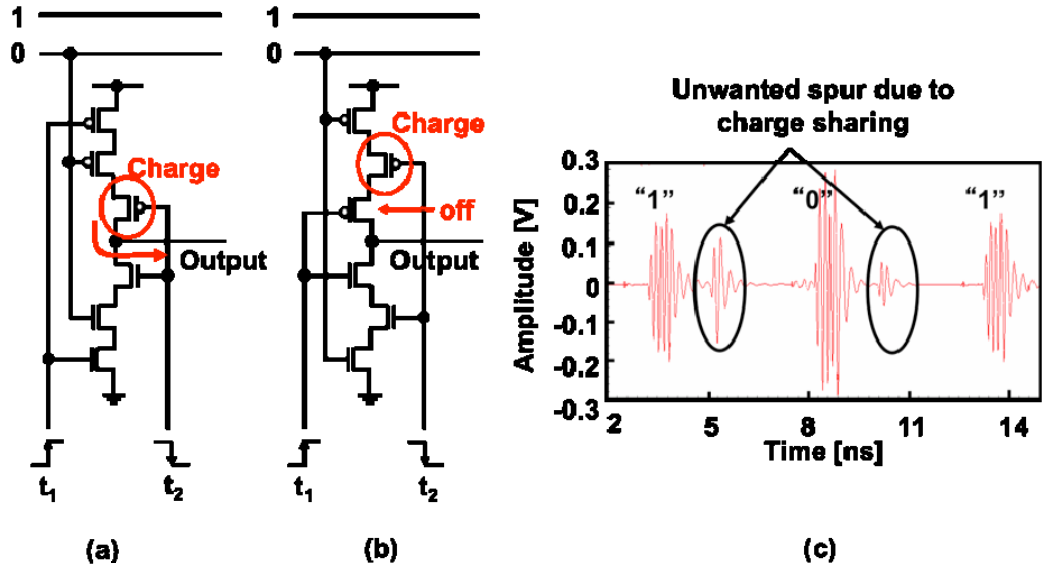


Figure 3.14 Charge sharing (a) another topology of IG cell (b) modified circuit (c) unwanted noise in between charge sharing.

When the clock passes through all four IG cells, a 500 ps pulse is generated. Similarly, a 180 degree phase shifted pulse is generated when data is "0", but at the opposite clock transition. Figure 3.13 further illustrates the operation of the IG cell with clock timing waveforms. Since the "1" and "0" pulses are generated at different clock timings, the clock is inverted at every data transition, keeping the pulse position constant for "1" and "0" pulses. This gives rise to a problem of charge sharing.

Figure 3.14(a) illustrates one particular topology of the IG cell that creates charge sharing problem. While the data is "1", at the rising edge of the clock, current should not pass through any of the upper or lower parts. However, at the clock transition, transistors connected to output dissipate the charge stored during the previous cycle creating unwanted spurious noise at the output as shown in Figure 3.14(c).

Charge sharing problem can be reduced to a large extent by modifying the circuit topology to that shown in Figure 3.14(b). This topology is used in the final transmitter implementation.

The pulses generated by the transmitter must be shaped in order to satisfy the FCC spectrum mask. In the proposed transmitter, the functionality of pulse shaping is incorporated in the pulse generator circuit itself by changing the dimensions of transistors in the impulse generator cells. The transistors widths in IG cell 1 and 4 are kept smaller so that the current flowing in them is less than that in IG cells 2 and 3. This in turn reduces the amplitude of the 1st and 4th impulse formed, thereby giving the pulse a raised cosine effect. This eliminates the need for additional band pass filters or pulse shaping circuits resulting in low energy consumption.

The simplicity of architecture of the pulse generator and its all digital design enables it to operate at a very low power. Furthermore, current flows through each impulse generator cell only when clock and data signals are active, resulting in an intermittent operation. For the data rate of 750 Mb/s, the period of each bit is 1.33 ns, while the pulse duration is 500 ps, which means that the circuit is on for only 38% of the time, resulting in significant reduction in energy consumption.

3.4.2 Power Amplifier

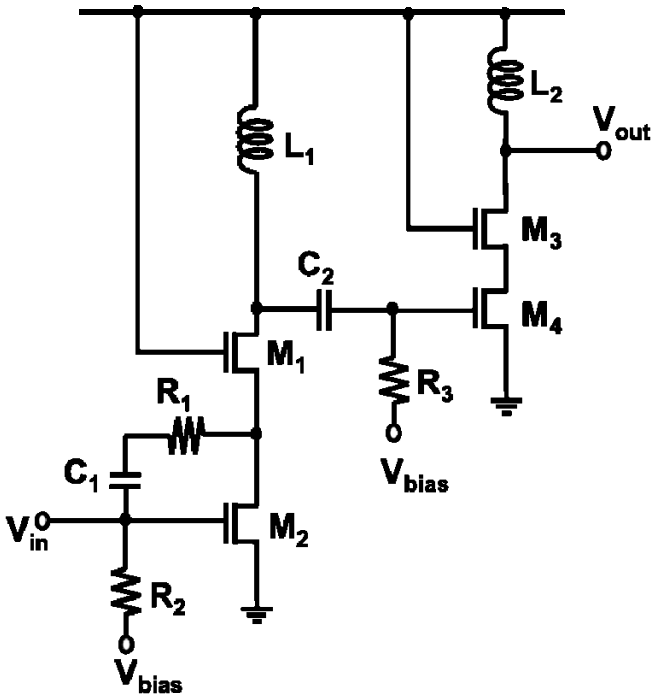


Figure 3.15 Circuit schematic of power amplifier.

The generated pulse is then amplified with the help of a power amplifier before feeding to the on-chip antenna. Since IR-UWB signals typically occupy bandwidth of several GHz, the design of a low power and wideband power amplifier is a challenging task.

Figure 3.15 shows the circuit schematic of the power amplifier incorporating cascade topology with resistive shunt feedback [14]. A single ended power amplifier is designed to drive the monopole on-chip antenna. The resistive shunt feedback has comparatively larger power dissipation, but provides good stability and wideband matching. Since inductors cost the maximum area among all the passive components in a circuit, the number of inductors is kept to a minimum of two in the proposed power amplifier.

3.4.3 Low Noise Amplifier

The low noise amplifier (LNA) is the foremost essential block of the receiver front end. As its name suggests, the primary function of LNA is to amplify the incoming RF signal while limiting the noise to a minimum level before the signal is demodulated. In wireless communication systems, modulated signals are transmitted over the air and received by the receiver antenna. The amplitude of the received signals is order of tens of microvolts. It needs to be amplified in order to bring it to the level suitable for demodulation. Since the change any of the parameters of LNA affects the overall performance of the system, its design involves consideration of number of factors such as linearity, gain, noise figure, stability, wideband matching and power dissipation.

Since the receiver operates in the frequency range of 6-10 GHz, the foremost concern of the LNA design is the matching over a large bandwidth of 4 GHz without sacrificing the gain. From the link budget estimation, the required gain of LNA is over 15 dB in the operating bandwidth. Also, the LNA input impedance should match with that of the antenna which is 50 ohm so as to amplify the signal with minimum loss. The input return loss (S_{11}) is a parameter used to quantify the matching of LNA. The input return loss must be kept below -10 dB over the entire operating frequency range in order to ensure proper matching between antenna and LNA input stage. The requirement of output impedance

matching is not stringent since the LNA output is connected to subsequent gain stages or mixer.

The second most important factor in LNA design is the noise figure. Since the emission levels of UWB systems are well below that of conventional narrowband systems, the noise figure requirements of UWB LNA are very stringent. The target noise figure for the LNA in this system is 4 dB so as to maintain a good signal to noise ratio.

As discussed in the previous sections, keeping the power dissipation to the lowest is the most important priority in designing the proposed system. Among all the blocks in receiver front end, LNA consumes the most amount of power and hence its power dissipation is a major concern while designing the circuit schematic. The target power dissipation for the LNA is kept under 20 mW. The LNA circuit was designed taking above factors into consideration. Figure 3.16 shows the circuit schematic of LNA.

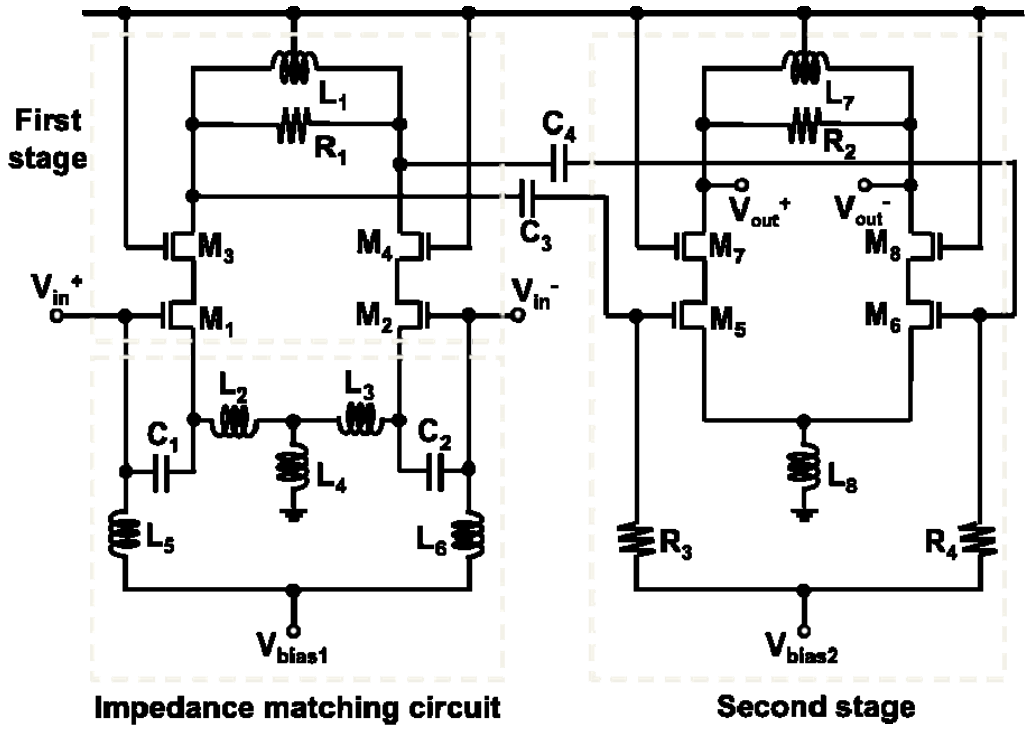


Figure 3.16 Circuit schematic of two-stage LNA.

Unlike the transmitter, the circuits in the receiver side are particularly sensitive to supply and substrate noise and hence are designed in differential logic in order to reject common mode disturbances. Since it is difficult to satisfy the performance requirements

discussed above with a single stage of LNA, two gain stages are cascaded in the proposed LNA. The LNA consists of an impedance matching stage and amplifying stage. The impedance matching stage uses inductive degeneration to match the input impedance of LNA to that of receiver antenna. In order to increase the flexibility in circuit design, capacitors C_1 and C_2 were added in between the source and gate of transistors M_1 and M_2. The amplifying stage consists of cascode topology. The cascode topology improves the frequency characteristic of the amplifier and reverse isolation between input output stages [15]. The amplifying stage incorporates shunt peaking by using inductor and resistor as a load in order to increase the gain. The second amplifier stage is similar to first one and further amplifies the signal coming from the first stage.

3.4.4 Mixer

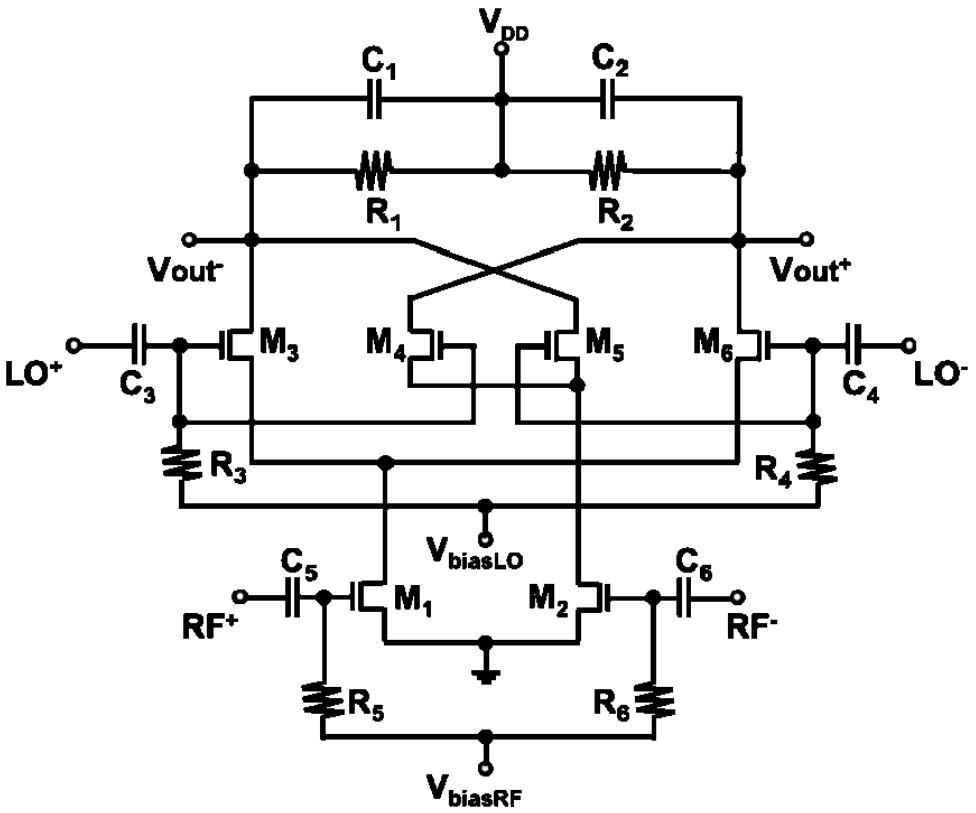


Figure 3.17 Double balanced Gilbert cell mixer circuit schematic

Mixer is another critical block in the design of UWB receiver after low noise amplifier. The mixer is required to have good linearity, noise figure, conversion gain as well as isolation. Furthermore, the power dissipation of the mixer should be kept to a minimum. Since the proposed receiver operates in the 6-10 GHz frequency range, design of a mixer which satisfies above requirements is a challenging task.

Figure 3.17 shows the mixer schematic. A double balanced Gilbert cell topology is used. The signal amplified by the LNA is applied to the RF port of the mixer formed by transistors M_1 and M_2. Transistors M_3-M_6 form the LO port of the mixer. The LO signal generated by replica pulse generator is single ended and is converted to differential signal before feeding to the LO port. The LO and RF bias is given through resistors R_3-R_4 and R_5-R_6 respectively. Resistors R_1 and R_2 form the load while capacitors C_1 and C_2 are used to increase the flexibility of the design.

3.4.5 Integrator

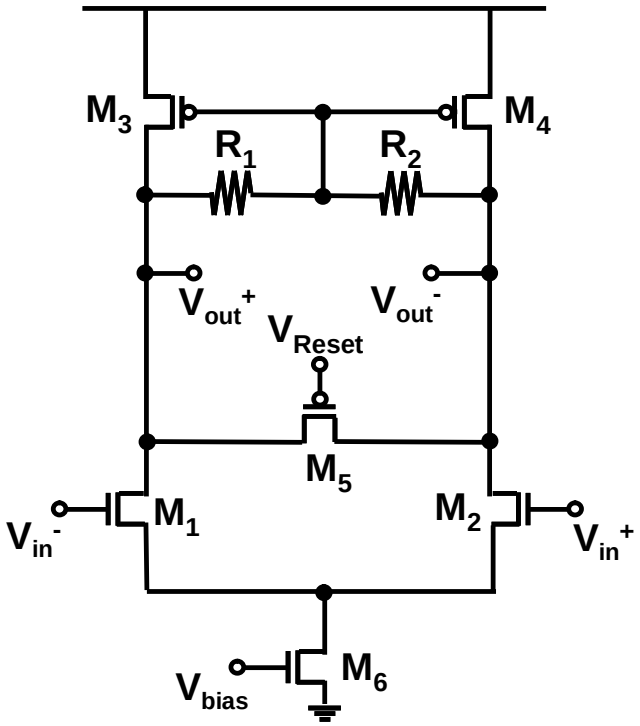


Figure 3.18 Circuit schematic of integrator and amplifier.

The output of mixer contains high frequency components which need to be removed before the signal is passed to the comparator for obtaining the base band data. The integrator block performs this operation since an integrator is essentially a low pass filter. Figure 3.18 shows the circuit schematic of the integrator.

The output signal of mixer is of very low amplitude. In the proposed receiver, the integrator also acts as an amplifier. Transistors M_1 and M_2 form a common source stage and amplify the incoming signal from mixer output. Transistors M_3 and M_4 form the PMOS load while resistors R_1 and R_2 form the low pass filter. Typically, the cutoff frequency of the low pass filter is decided by the base band data rate. In this case, the base band data rate is 750 Mb/s. The low pass filter cut off frequency was kept around 1 GHz so as to accommodate the higher data rates. Since the cut off frequency is very high, use of external capacitors is eliminated as the parasitic capacitance of transistors M_1 and M_2 can be used as a capacitor. Transistor M_5 acts as a reset switch for discharging the output to ground.

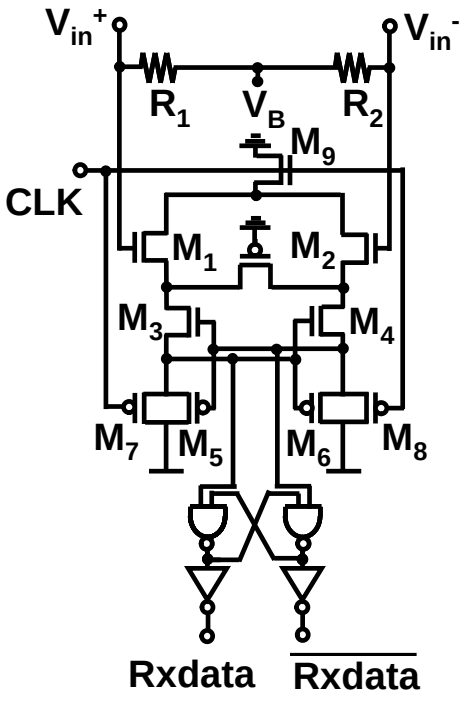


Figure 3.19 Hysterisis comparator schematic

3.4.6 Comparator

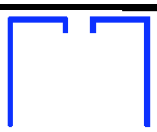
The comparator samples the input data and decides the polarity of it depending upon the difference in the two inputs. The hysterisis comparator schematic used in the proposed receiver is shown in Figure 3.19.

Transistors M_1 and M_2 are sense transistors and M_3-M_6 are cross coupled devices while M_7 and M_8 are reset transistors. When CLK signal is high, the transistors M_7 and M_8 are off and M_1 and M_2 are turned on coupling the voltage difference between inputs V_{in}+ and V_{in}- to the sources of M_3 and M_4. The output of the latch is the base band data.

3.5 On-chip Antenna

With the 6-10GHz frequency band, the fabrication and utilization of an embedded on-chip antenna has become feasible due to shorter wavelengths. For short distance communications up to a few centimeters, on-chip antenna can be a good candidate for a single chip system solution due to its low cost. In this work, we try to investigate the feasibility of embedded on-chip antenna for short distance UWB communications in the range of few centimeters.

Table 3-I Comparison of different antenna topologies.

Type	Shape	Miniaturization	Gain	Input
Folded dipole		×	○	Differential
Monopole		○	△	Single Ended
T-antenna		×	△	Single Ended

So far few papers have reported the on-chip antennas [16-19] presenting different antenna topologies such as patch antenna or dipole or loop antenna. Since the implementation area on the chip is limited, a small size and high efficiency antenna is desirable. Three antenna topologies were studied namely, dipole, monople and T-antenna for the proposed transmitter. Each antenna topology was simulated using CST Microwave Studio.

Table 3-I shows the comparison of each antenna topology. After comparing the three topologies, monopole antenna was chosen for two reasons. Firstly, monopole antenna requires half of the size of that of dipole antenna. Secondly, the output pulse from power amplifier is single ended. If a dipole is used, a balun needs to be inserted before the dipole. With the use of monopole antenna, the single ended power amplifier output can be connected directly to the monopole. However, realization of ground plane is necessary for monopole antenna, which in this case is provided by the silicon substrate.

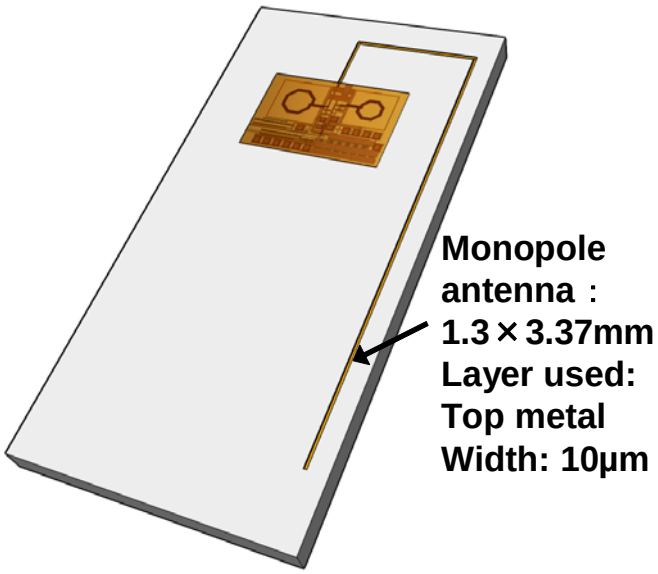


Figure 3.20 Design of embedded on-chip monopole antenna.

As discussed in section 2.4.4, the element length of the on-chip antennas on a silicon substrate can be reduced to a significant extent with the use of wavelength shortening effect. With this principle, a signal line placed in the dielectric medium is seen longer by the signal compared to that placed in vacuum. The dielectric constant of the SiO_2 layer between the signal line and ground is 3.9. Due to the wavelength shortening effect, the

effective length of the antenna in the presence of dielectric medium can be thought of as (ε_r : dielectric constant) $1/\sqrt{\varepsilon_r}$. Hence, the on-chip antenna can be accommodated in half the size compared to the antennas that are mounted in air. The wavelength (λ) for 8 GHz frequency is 37.5 mm and size of monopole antenna required in air is λ/4 = 9.35 mm. However, on a silicon substrate, due to wavelength shortening effect, the monopole antenna can work with 4.67 mm length. The structure of antenna designed in this work is illustrated in Figure 3.20. Antenna element width of 10 μm was decided and the length of the antenna element was chosen as 4.3 mm to work over the band of 6-10 GHz. The antenna element was folded so as to accommodate on the limited size of the chip. This shape of the antenna was designed for broadband matching using simulation while taking the wavelength shortening and various other effects into consideration.

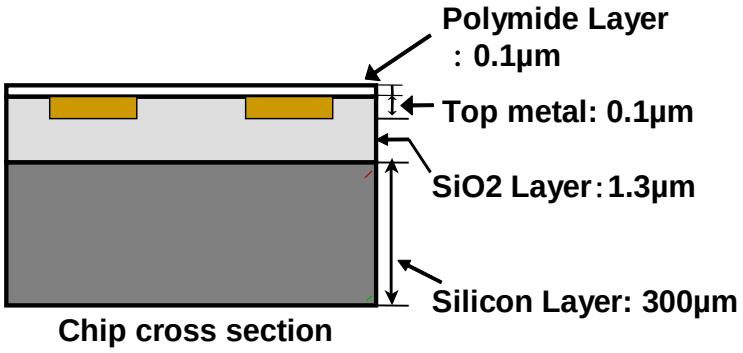


Figure 3.21 Cross section of chip with embedded antenna.

Figure 3.21 shows the antenna structure on the chip and thickness of different layers in the chip cross-section. The simulated and measured characteristics of the embedded antenna are discussed in next sections.

3.6 Transceiver Simulation Results

A simulation of proposed transceiver was carried out with the help of Spectre RF to evaluate the performance. Each block in the transmitter was simulated individually as well as the system as a whole. Figure 3.22 shows the simulated time domain waveforms at various blocks of transceiver. Since the performance of the designed circuit varies significantly from the simulation results to the actual implementation due to the influence

of parasitic capacitances, inductances and resistances, the pulse generator designed in the proposed transmitter was simulated in post layout environment taking parasitic capacitances and inductances into account. It can be seen from the figure that the transmitted data can be recovered successfully at a data rate of 750 Mb/s.

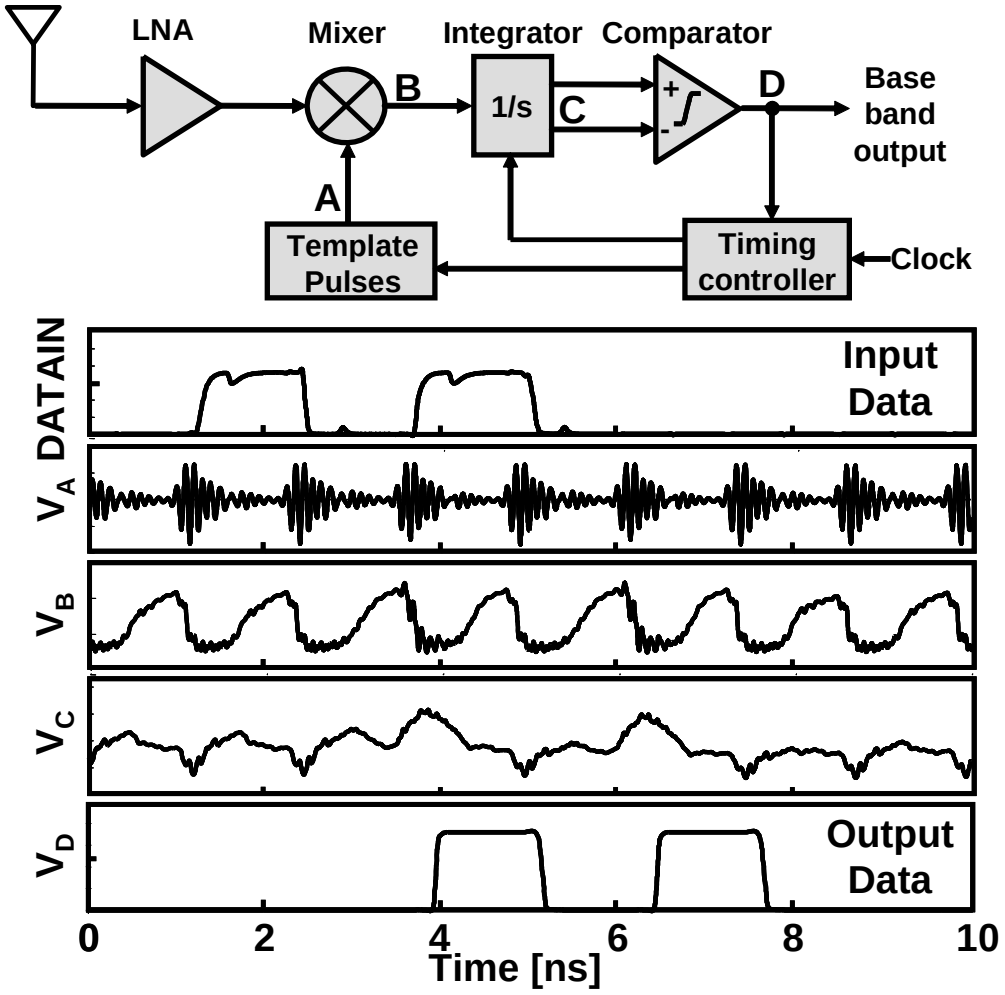


Figure 3.22 Simulated time domain waveform at various blocks of receiver.

3.7 Test-chip Implementation and Measurement Setup

The proposed transmitter chip was fabricated using 0.18 μm CMOS technology with 6 metal layers and a supply voltage of 1.8 V. Figure 3.23 shows the chip microphotograph with the pulse generator, power amplifier and the embedded monopole antenna. The die area of the transmitter without embedded antenna is 0.045 mm^2, which is significantly less compared to the conventional transmitters. Figure 3.24 shows the measurement setup

for the transmitter measurement. The digital Clock and Data signals were given with the help of signal generator and the analog output was measured on oscilloscope and spectrum analyzer. Network analyzer was used for the measurement of return loss and gain of various individual blocks.

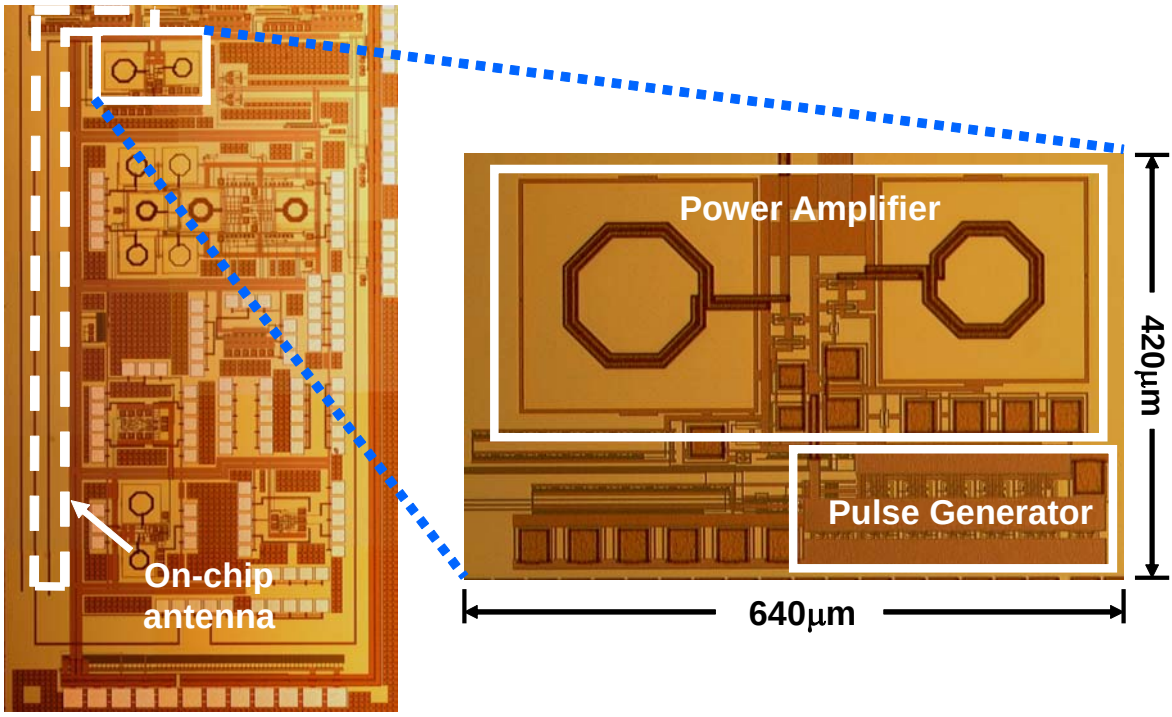


Figure 3.23 Chip photomicrograph with transmitter and on-chip antenna.

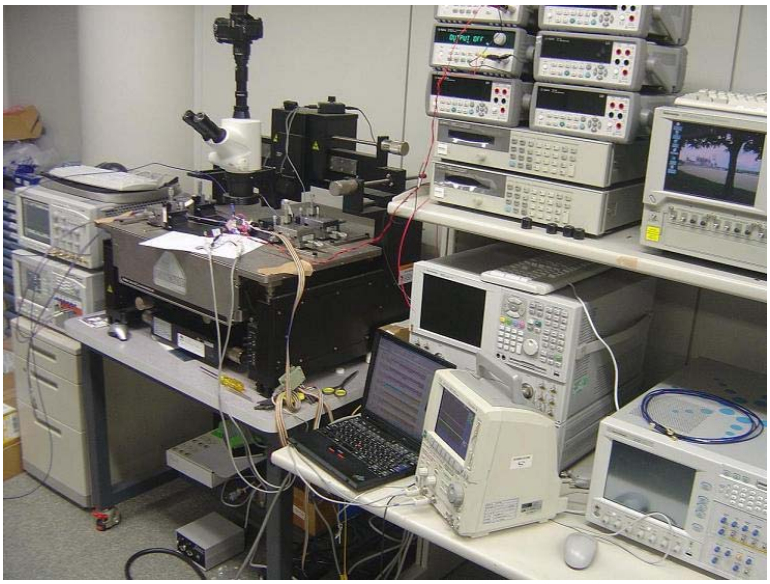


Figure 3.24 Measurement setup.

A PCB board was designed for the measurement of the chip. The board was made from FR4 substrate to work with high frequency signals. The test-chip was mounted on the PCB board for measurement and the connections from chip to board were made by bonding wires. Figure 3.25 depicts the test board and mounting of chip on board.

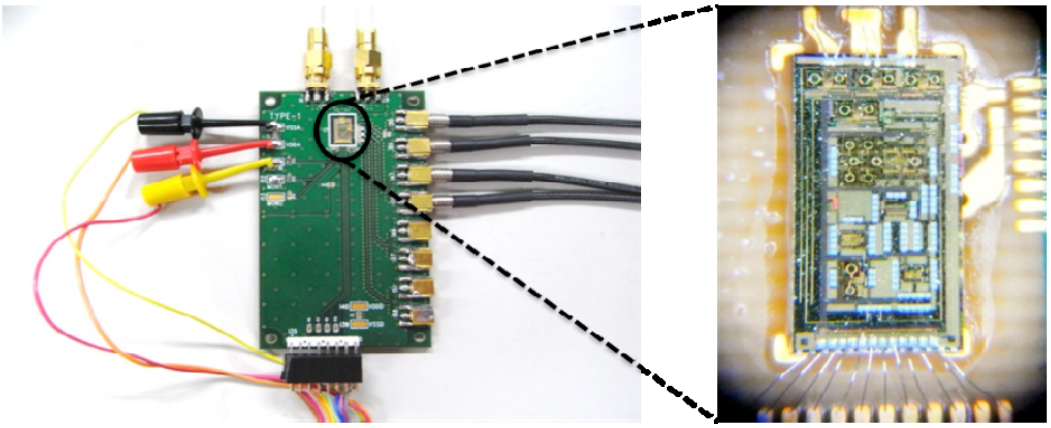


Figure 3.25 PCB board for measurement and mounted chip.

3.8 Measured Results

The measured pulse output waveform at power amplifier output for pseudo random data input measured on an oscilloscope is presented in Figure 3.26. Pulse center frequency of 8 GHz was observed. In this transceiver implementation, the center frequency was not calibrated. However, in the implementation of whole transceiver system, the centre frequency of the pulse needs to be roughly calibrated because the performance of the correlator in the receiver is affected by the matching of the center frequency between the transmitted pulse and replica pulse in the receiver. In that case, a DLL can be used to adjust the center frequency by changing the inverter delay in IG cell. The transmitter with DLL will consume more power. However, when used intermittently, for example between each data packets, additional power consumption can be reduced drastically.

Figure 3.27 shows the measured pulse waveform at the output of pulse generator connected directly to a 50 ohm load. This load can be an external antenna with 50 ohm impedance. The measured pulse peak-to-peak amplitude was 70 mV using power amplifier and 30 mV without using power amplifier respectively.

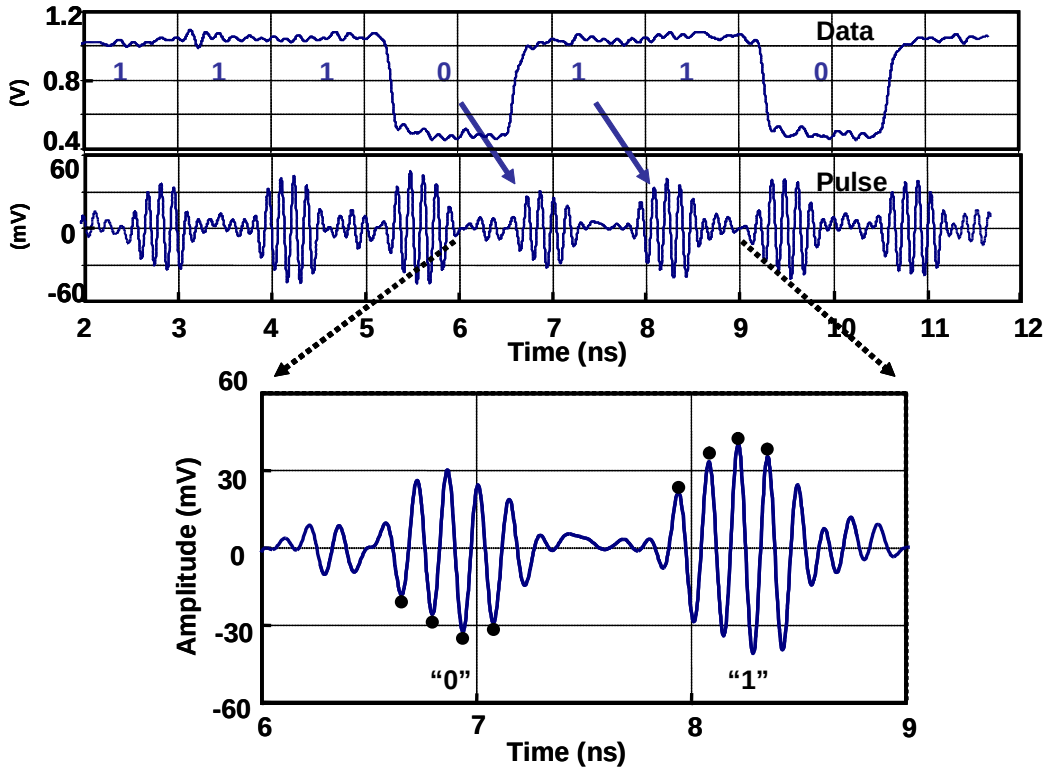


Figure 3.26 Measured 750 Mb/s time domain waveform at the power amplifier output.

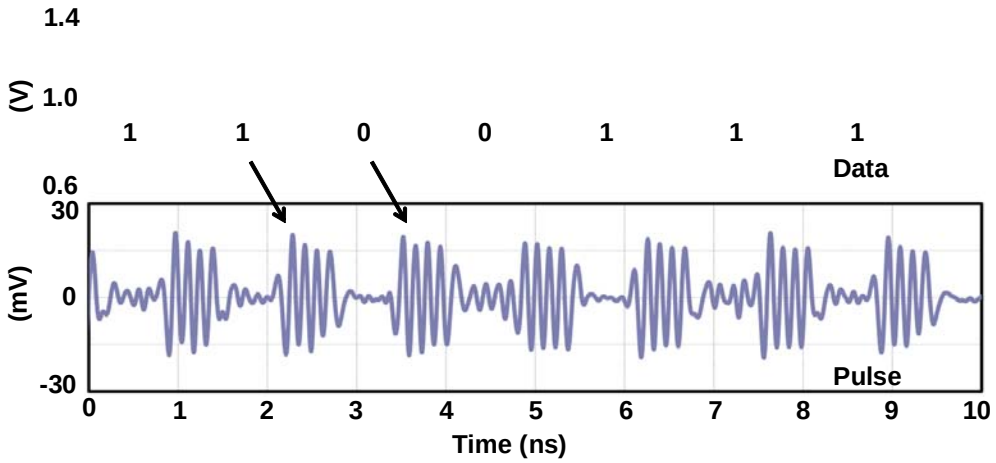


Figure 3.27 Measured 750 Mb/s time domain waveform at the pulse generator output.

Maximum pulse repetition rate of 750 Mb/s was achieved. The total energy dissipation, with the use of power amplifier for the pulse repetition rate of 750 Mb/s was 41 pJ/b, and was reduced to 12 pJ/b without using power amplifier. This is the lowest energy consumption and highest data rate among different reported UWB transmitters at the time of publication of this work [21]. Table 3-II shows the comparison.

Table 3-II Performance comparison of IR-UWB transmitters (Assumed communication distance in this work < 10 cm).

	This Work*	[1]	[2]	[3]	[4]
Band of Operation	6 – 10 GHz	3.1 – 5 GHz	3.1 - 5 GHz	3.1 – 10 GHz	3.1 - 10 GHz
Data Rate	750Mb/s	10Mb/s	36Mb/s	400Mb/s	1.8Gb/s
Energy Consumption	12pJ/b**	47pJ/b	82pJ/b	247pJ/b	126pJ/b
Technology	180nm	90nm	180nm	180nm	90nm

*For communication distance ≤ 10cms
** Transmitted power ≈ -30 dBm

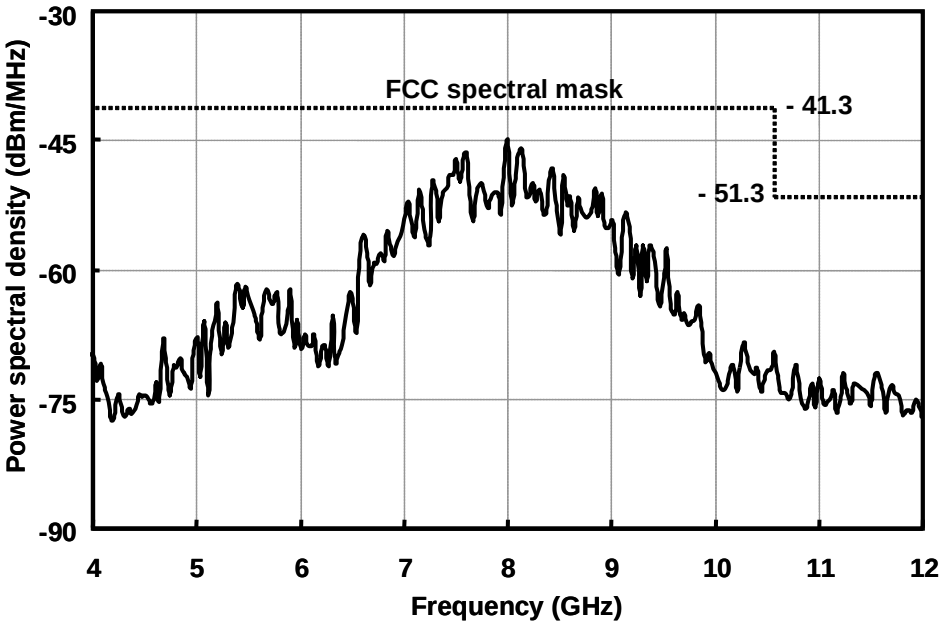


Figure 3.28 Measured power spectral density of transmitter at power amplifier output.

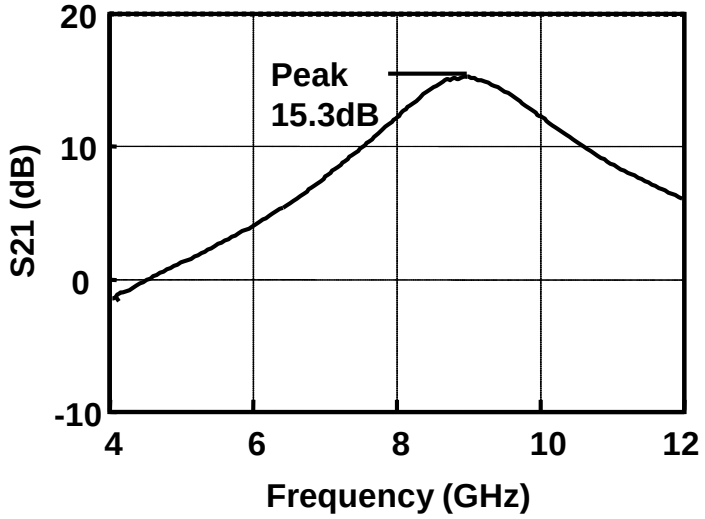


Figure 3.29 Measured S21 of power amplifier.

The measured power spectral density with the help of a spectrum analyzer at the power amplifier output is depicted in Figure 3.28. It can be seen that the measured spectrum matches with the simulated spectrum for 6-10 GHz band and is well below the FCC spectral mask for UWB communications systems.

Figure 3.30 depicts the measured return loss of the embedded antenna. The antenna is matched over a frequency band of 2.4 GHz. It was found out from the simulation that the antenna has maximum directivity of 5.4 dBi and radiation efficiency of -22 dB.

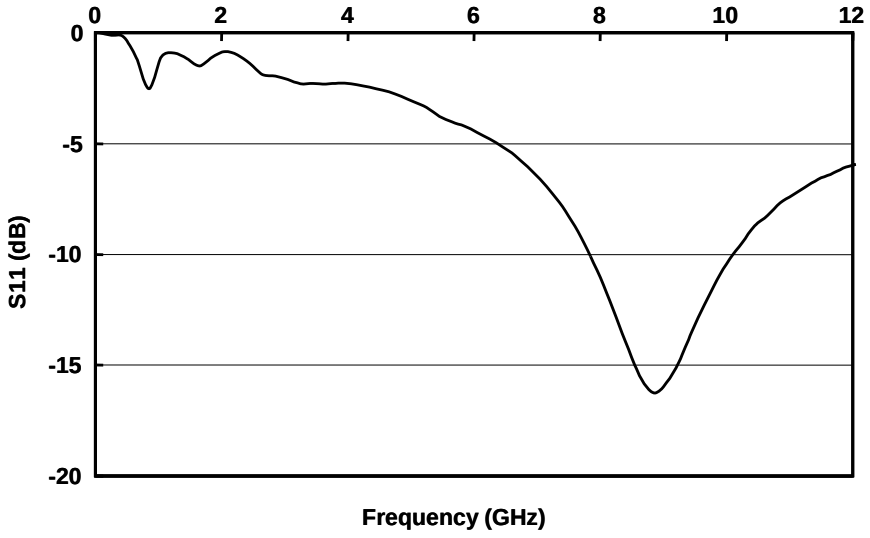


Figure 3.30 Measured S11 of on-chip antenna.

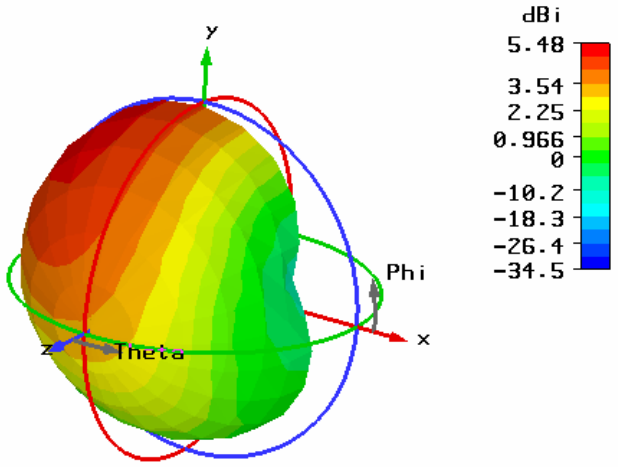


Figure 3.31 Simulated directivity and efficiency of on-chip antenna.

Table 3-III Performance summary.

Antenna	External	Embedded
Layout area	0.045mm^2	0.29mm^2
Energy consumption*	12pJ/b** (at 750Mb/s)	41pJ/b (at 750Mb/s)
Technology	0.18μm CMOS	
Supply voltage	1.8-2.2V	
Pulse center frequency	8GHz	
Band of operation	6-10GHz	
Maximum data rate	750Mb/s	

*For communication distance ≤ 10cms
** Transmitted power ≈ -30 dBm

Figure 3.31 shows the directivity pattern of on-chip antenna simulated in CST microwave studio. On-chip antenna measurements such as directivity, gain and efficiency were not carried out since they require special environment such as anechoic chamber and mobile probes. However, the total transmitted power from the on-chip antenna can be estimated by adding the power delivered to the antenna by power amplifier (-20 dBm) and the simulated efficiency of the antenna (-22 dB). The estimated transmitted power by

on-chip antenna is approximately -42 dBm which is sufficient enough for the detection of the signal within a distance of few centimeters if a high gain low noise amplifier is used at the receiver front end. Claims made by some of the on-chip antenna papers [15-17] reporting the antenna efficiency of -6 dB to -10 dB bolster the idea that short distance communication using on-chip antennas is indeed a possibility. In this work, verification of the on-chip antenna simulation results with the measured results was not possible because of limitations of measurement environment and remains a topic of future research. The need for power amplifier can be eliminated by using a high efficiency external antenna, in which case, the area and energy dissipation of the chip is reduced by 85% and 70% respectively. Table 3-III summarizes the performance of the proposed transmitter.

Although the receiver operation was verified with only simulation results, the wideband LNA was designed and fabricated in 0.18 μm process and its performance was measured.

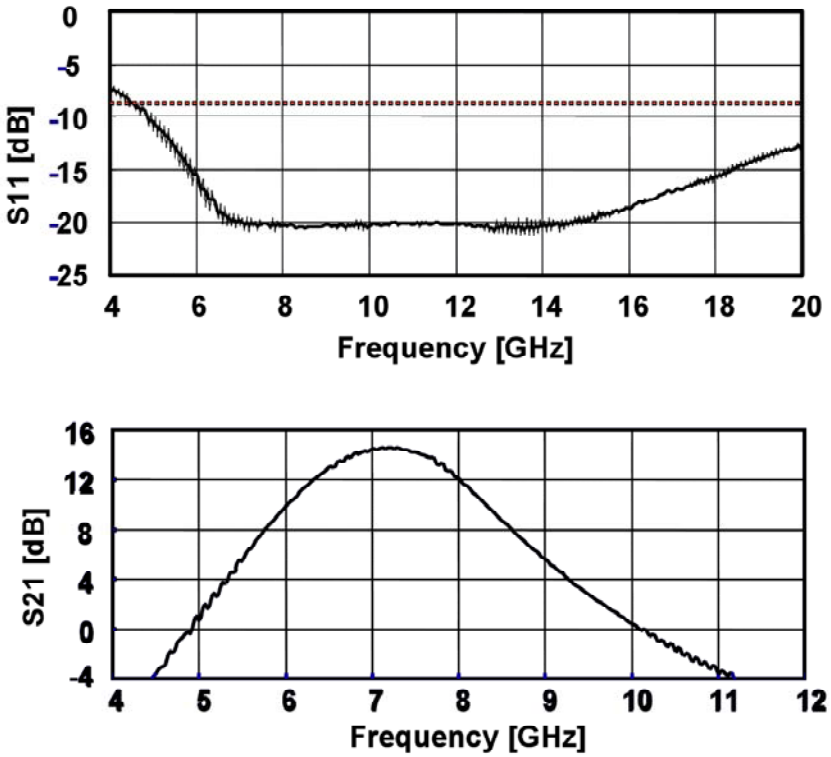


Figure 3.32 Measured return loss and gain of LNA.

Measured results matched with the simulated results. The LNA was matched over the entire 6-10 GHz frequency band and the maximum gain of LNA was 15 dB. Figure 3.32 shows the measured S_{11} and S_{21} characteristics of LNA.

3.9 Conclusion

A 750 Mb/s IR-UWB transceiver was designed for short distance communication within 10 cm. The transceiver operation was verified with simulation results while the transmitter was fabricated in 0.18 μm CMOS and its operation was confirmed with measured results. The transmitter generated bi-phase modulated pulses of 500 ps duration and 8 GHz center frequency. Highest data rate of 750 Mb/s was achieved with an energy consumption of 12 pJ/b. The transmitter complies with the FCC spectrum mask. An embedded on-chip antenna was designed and fabricated for 6-10 GHz band operation for short distance communications.

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Chapter 4 Design of 4 Gb/s Quasi-millimeter-wave Transceiver

4.1 Introduction

With the advent of micrometer and millimeter wave technologies using ultra-wideband, the research on short-range high-speed communication has seen a sudden upsurge. Up until recently, the focus of research on Ultra-wideband systems was on the 3.1 – 10.6 GHz band due to the limitation of CMOS in operating at higher frequencies. The usage of higher frequency bands, such as quasi-millimeter wave and millimeter wave was limited to costly compound semiconductor processes [1-3]. However, the advancement in CMOS technology in recent years has enabled industry and academia to exploit these higher frequency bands and created opportunities for design of low cost and low power systems [4,5]. The maximum allowed transmitted power by the FCC for indoor use in these higher frequency bands is –51.3 dBm/MHz. Due to their large bandwidth, these bands have a potential for very high data rates that can reach up to a few Gb/s. Also, the higher frequency range gives scope to design antennas on the silicon substrate [6-9] providing opportunities for developing low cost single-chip solutions. RF CMOS systems operating in this frequency range can be used in radars, wireless personal area networks and industrial-scientific-medical applications.

For a communication distance of few centimeters, several new applications can be thought of such as video transfer between a camera and a computer, or a video download at a kiosk, which will parallel wireless 1394 or wireless USB 3.0. These applications require transceiver systems to operate at high data rates while consuming low power. Although UWB systems (3-10GHz) can reach several meters with data rates of up to 480 Mb/s and the millimeter wave systems have potential to reach up to several Gb/s, the front end circuits itself in these systems consume hundreds of milliwatts. Design of a transceiver that operates at a data rate of several Gb/s, while consuming power in the order of few tens of millwatts is thus essential.

In this chapter, a transceiver is designed to operate in the 14-18 GHz band for a target communication distance of 10 cm. The transceiver is designed for the burst transmission to realize high speed and low power operation. The transceiver operation has been verified by system simulation. As a first step towards its silicon implementation, a

transmitter was designed and fabricated in 65 nm CMOS. As discussed in the later sections, since the PLL is a common block in both transmitter and receiver, its phase noise affects the overall system performance. Hence, its operation was verified with the experimental results in the transmitter implementation.

This chapter is organized into five sections. In section 2, transceiver architecture is explained in detail. A link budget estimation is discussed to show the feasibility of the proposed transceiver architecture and the effect of phase noise in PLL on BER is demonstrated using Matlab simulation. Section 3 discusses circuit topologies and schematics of various blocks in the transmitter. In section 4, measured results of the fabricated transmitter test-chip are presented. Finally, the performance summary and conclusion are given in section 5.

4.2 Architecture Overview

The transceiver architecture design involves consideration of two factors: link budget and modulation scheme. Transceiver architecture should be chosen such that it will make optimum usage of the available output power and bandwidth. Two main architectures, namely coherent and non-coherent architecture, are popular among UWB transceivers. Coherent architecture is more complex than non-coherent one and consumes more power due to additional blocks. However, in UWB transceivers, noise immunity and low BER are crucial factors in evaluating the system performance and in this respect coherent architecture has an edge over non-coherent one. In this research, we have chosen coherent architecture with BPSK modulation scheme.

4.2.1 Transmitter Architecture

The transmitter architecture is shown in Figure 4.1. It consists of a PLL and an up-conversion mixer. The PLL multiplies the reference signal of 2 GHz to generate an local oscillator (LO) frequency of 16 GHz. The LO is then passed through an up-conversion mixer where it is mixed with base-band data to generate BPSK modulated signal. In a conventional impulse radio UWB transmitter, data is sent over the channel in the form of modulated short duration pulses. In case of data rates of hundreds of megabits per second,

this achieves significant reduction in power dissipation as the time interval between consecutive data bits is large enough for the transmitter circuitry to switch on and off.

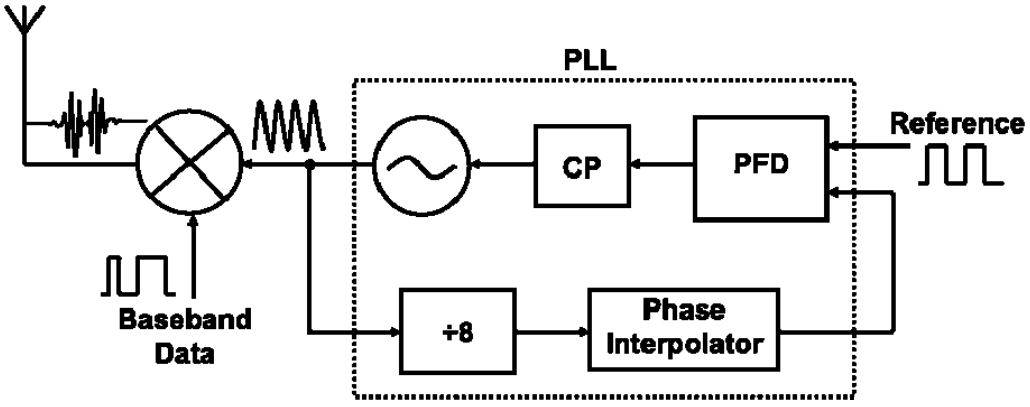

Figure 4.1 Transmitter architecture.

But as the data rates approach 4 Gb/s as shown in Figure 4.2, this time interval reduces significantly leaving no time for the circuitry to switch between the pulses. Simulation results showed that for a data rate of 4 Gb/s, the power dissipation did not change by a significant amount in case of a pulsed transmission and that of a continuous wave transmission. Instead, if the data is sent over in the form of bursts, power dissipation can be reduced since the circuitry is switched off during down time. Hence, the transmitter in this architecture is designed to generate continuous BPSK waveform with burst transmission instead of short duration pulses.

The PLL uses a ring oscillator instead of an LC oscillator for high-speed on off switching in burst transmission. The ring oscillator has faster startup time compared to the LC oscillator. Furthermore, it takes smaller area on chip due to the absence of passive components. As explained in the next subsection, the transceiver makes use of a faster carrier and symbol timing recovery circuit. In order to realize faster locking time of the PLL for burst transmission, a ring oscillator is preferred over the LC oscillator. However, the ring oscillator introduces more phase noise compared to LC oscillator. In section 2.3, we investigate the effect of phase noise on the overall system performance and maximum tolerable phase noise.

For the homodyne architectures employing bi-phase modulation scheme, detection by I/Q mixing is most common. In I/Q detection, the received signal is mixed with I/Q

signals generated by LO to recover the baseband signal. However, at frequencies in the order of tens of GHz, generating I/Q signals is a tedious task requiring high precision phase shifters or quadrature mixers. Furthermore, I/Q detection requires separate mixers for quadrature signals causing additional power consumption as well as increase in chip area. Also I/Q imbalance can corrupt down converted signal constellation, thereby affecting the BER. To avoid these problems, we have proposed direct conversion receiver architecture with a high speed carrier and symbol timing recovery scheme. This architecture uses only one mixer thereby reducing power consumption as well as chip area.

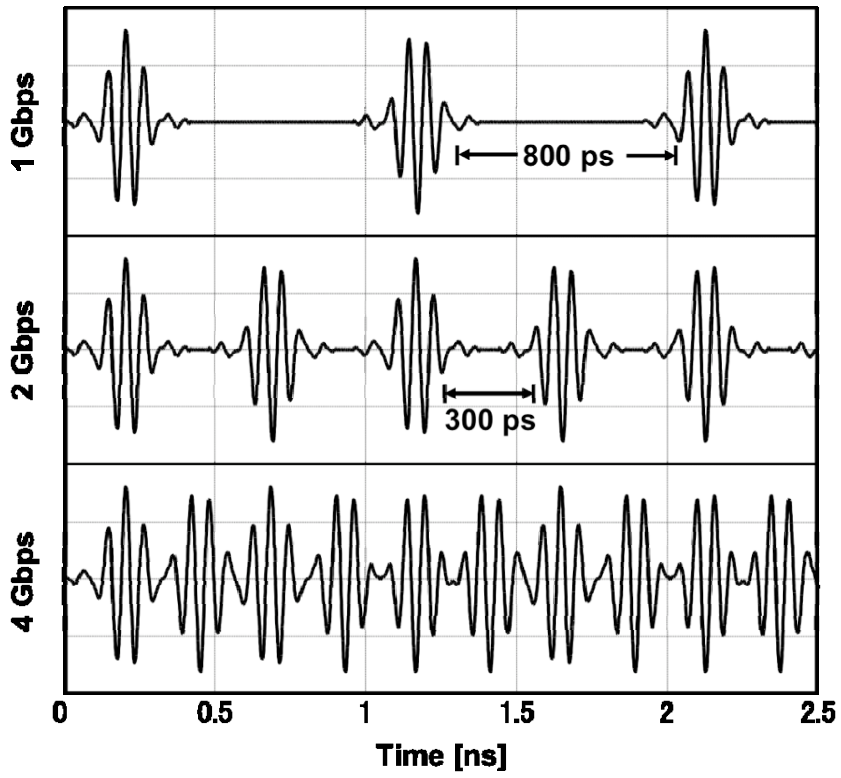

Figure 4.2 Time interval between pulses for different data rates.

4.2.2 Receiver Architecture

Figure 4.3 shows the receiver architecture with a novel carrier and symbol timing recovery loop. The receiver uses a direct conversion coherent architecture. In the proposed receiver, the incoming RF signal is amplified by a low noise amplifier (LNA) and then multiplied with the LO signal generated by a PLL.

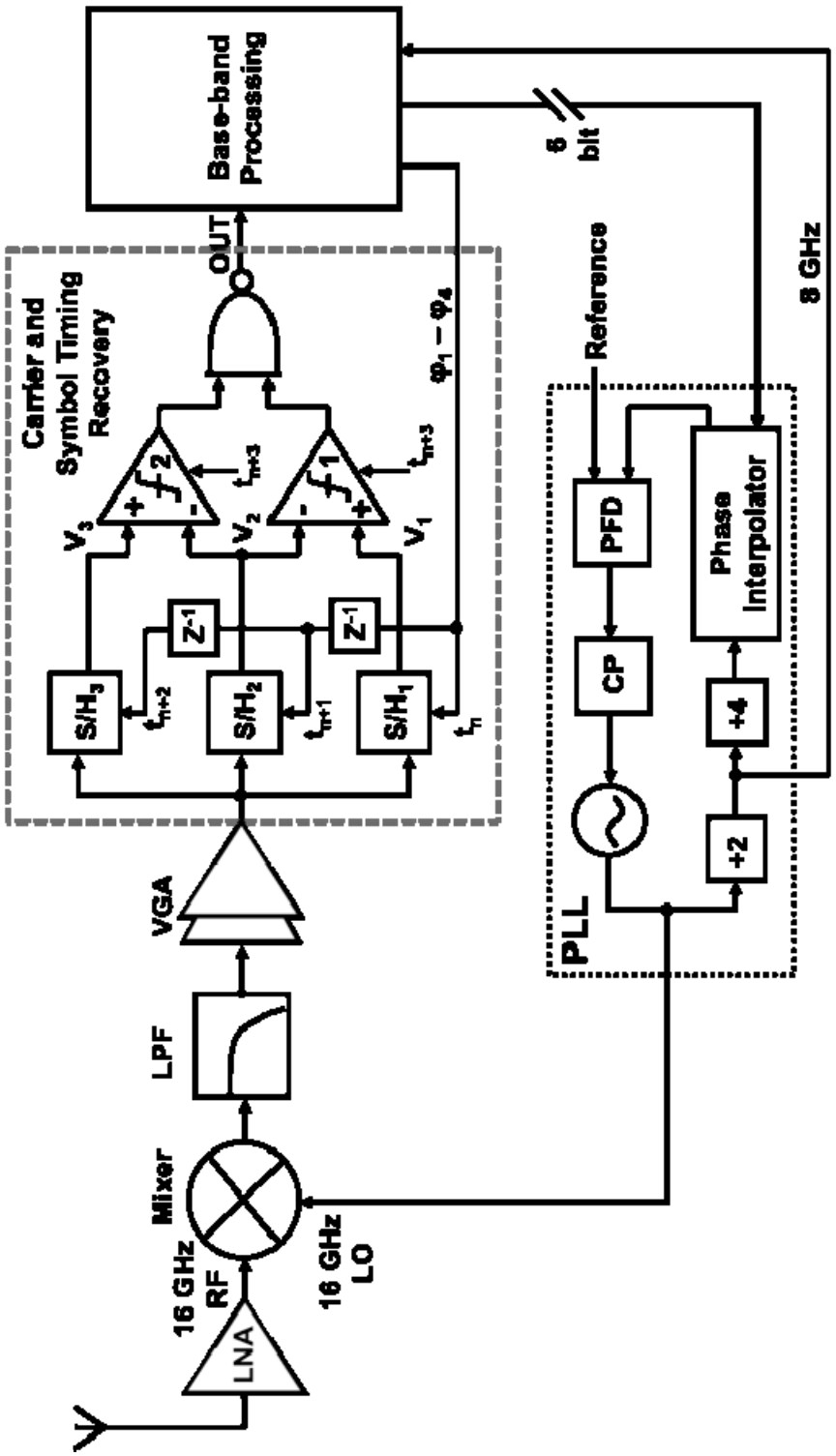

Figure 4.3 Receiver architecture. With carrier and symbol timing recovery scheme

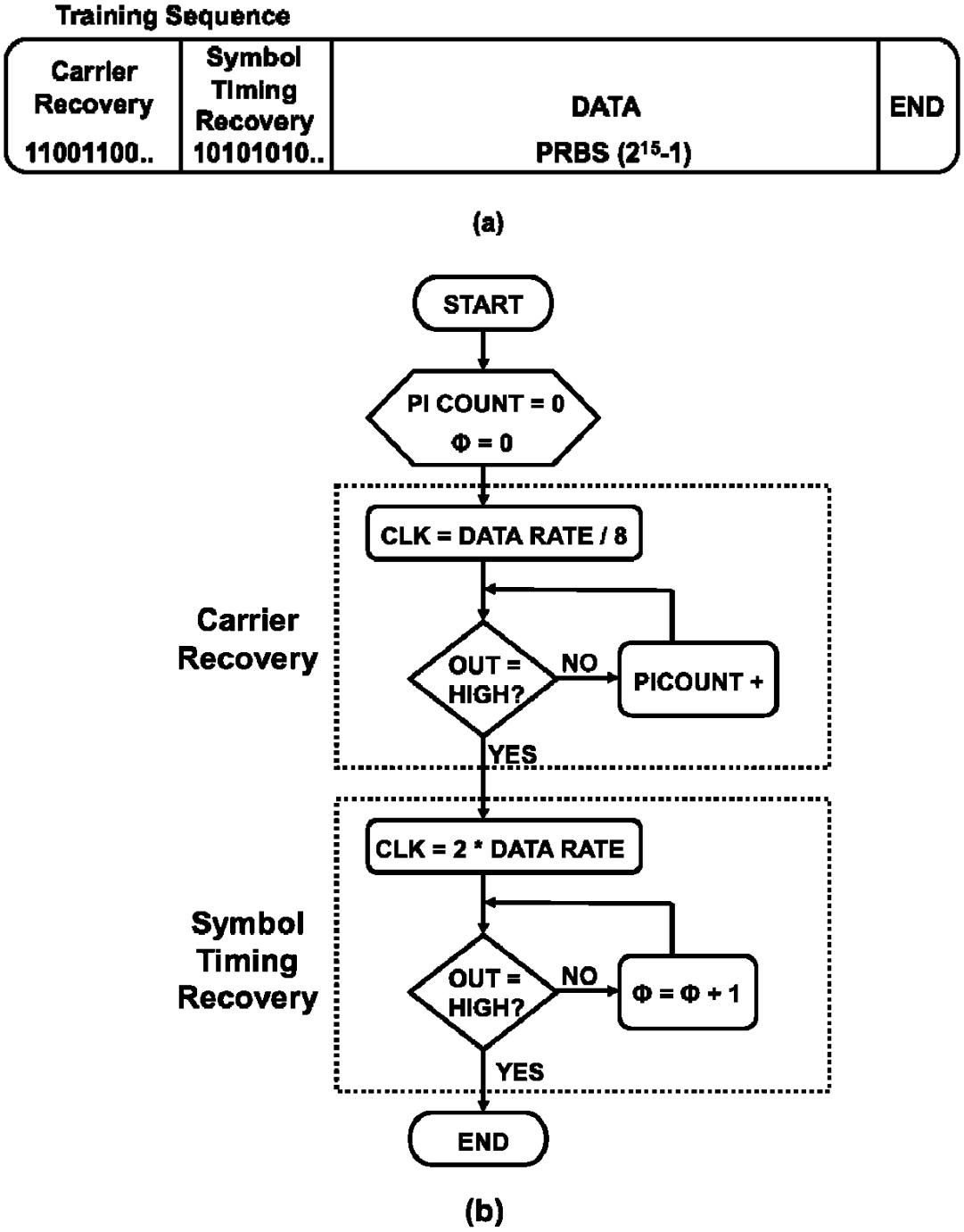

Figure 4.4 (a) Data packet structure, (b) Carrier and symbol timing recovery flow.

The carrier frequency of LO is same as that of RF, and hence the output of the direct conversion mixer after passing through a low pass filter is the demodulated base band data. The base band data is amplified by a series of amplifier stages and the DC offset is

cancelled with capacitors before being sent to the carrier and symbol timing recovery (CSTR) loop. The CSTR loop is composed of three sample and hold (S/H) circuits, two comparators, a NAND gate and a base-band processing unit. Both carrier and symbol timing recovery is carried out using the same blocks. Since the base-band data rate is 4 Gb/s, the carrier and symbol timing recovery loop needs to operate at very high speed. The next few paragraphs describe the detailed operation of the carrier and symbol timing recovery circuit.

First the data packet structure is decided. For the burst transmission, the data is sent in the form of payload preceded by a training sequence. The carrier and symbol timing recovery is carried out in the training sequence interval. The payload length is decided mainly by the time interval of constant phase by PLL. Figure 4.4(a) shows the transmitted data packet structure. It consists of a training sequence followed by a burst of data packets. Carrier and symbol timing recovery is performed in succession during the training sequence interval. The total length of the training sequence for carrier and symbol timing recovery is kept at 1/10th of the data packet length. A flow-chart in Figure. 4.4(b) shows the operation of carrier and symbol timing recovery circuit. The base band data at mixer output is first passed through the carrier synchronization loop.

Carrier synchronization is carried out with the help of receiver PLL and CSTR block. The Receiver PLL is similar to that of the transmitter in Figure 4.1 except that the phase interpolator (PI) circuit is activated for the carrier recovery. The PLL generates 16 GHz LO signal with the help of reference clock provided externally. In order to achieve correlation, the frequency as well as phase of the LO signal needs to be matched with that of the RF. This is achieved through the PI block which changes the phase of the LO signal depending upon the 6 bit control input from the base band processing unit. The base-band processing unit increments the PI control input to select a phase from one of the 64 combinations until the correlation between RF and LO is obtained. When the phases of both RF and LO match, the amplitude of base band data at mixer output reaches the maximum value (peak value in the constellation). This phase of maximum amplitude can be found with the help of the proposed CSTR block as follows.

A training sequence of alternate '11' and '00' is sent during the carrier recovery loop. The S/H circuits sample the incoming data at consecutive sampling instants. The sampling frequency is kept 1/8 times that of the data rate (500 MHz). The delay Z^{-1} corresponds to one sampling clock interval, which is 2 ns. This gives sufficient time for the PLL to lock between phase changes.

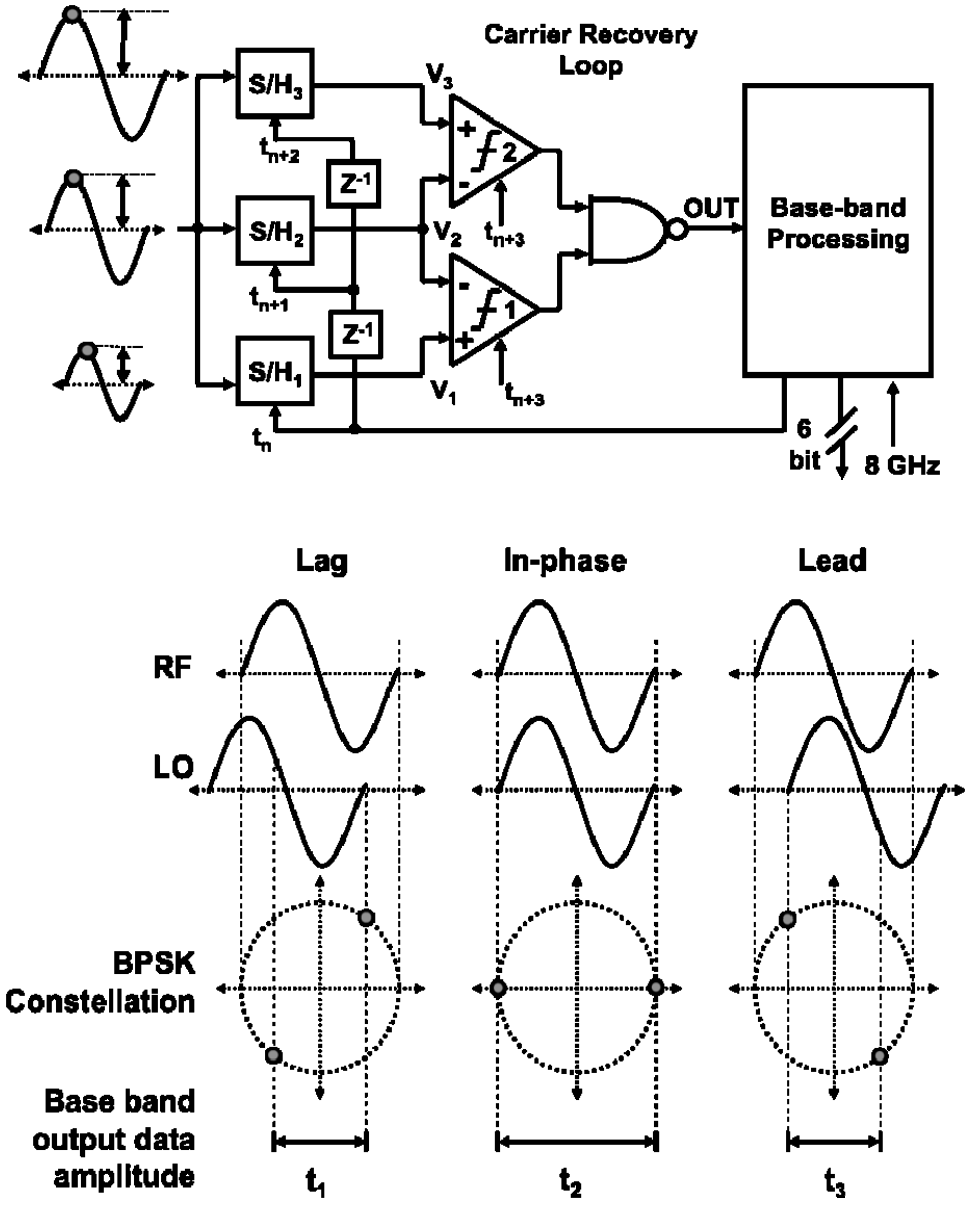

Figure 4.5 Carrier recovery concept in receiver.

Between consecutive sampling instants, the base band processing unit increments the phase of the LO by one-step by incrementing the 6 bit control input of PI. Since the LO phase changes at each sampling instant, the amplitude of base-band data envelope also changes. As a result, the three S/H circuits sample the output data at three consecutive sampling instants and have different amplitudes, which are compared with each other by the three comparators. The baseband processing unit increments the PI count until a situation as shown in Figure 4.5 is reached. At this point both RF and LO signals are in phase at sampling instant t_2 compared to that of sampling instants t_1 and t_3. As a result, the amplitude of stored data at $S/H_2(V_2)$ is higher than that of $S/H_1(V_1)$and $S/H_3(V_3)$. At this point, the outputs of both the comparators turn low and the output of NAND gate turns high. The baseband processing unit stops incrementing the LO phase and carrier synchronization is achieved. The operation of S/H circuits, comparators and NAND gate in the CSTR block is further elaborated in the symbol timing recovery loop.

Once the carrier synchronization is achieved, the data is passed through the symbol timing recovery loop. The symbol timing recovery is carried out in a similar way to that of the carrier recovery loop, except that the sampling clock is chosen to be two times the data rate (8 GHz). The sampling clock is derived from the divider circuit in receiver PLL. The base-band processing unit increments this sampling clock to choose one of the four phases from $\varphi_1 - \varphi_4$. Since the sampling frequency is two times the data rate, one of the four phases from φ_1 to φ_4 can achieve the symbol timing recovery. Figure 4.6 explains the operation of this block in detail. The S/H circuits store the output data amplitude at three consecutive sampling instants in one symbol period. The stored voltages at three sampling instants are compared with each other to find the amplitude peak of data waveform. The comparator output is high if its '+' input is higher than the '-' input. As shown in Fig. 7, at phase φ_4, the voltages at V_1 and V_3 are less than the voltage at V_2, and the outputs of comparator 1 and 2 are both low, which turn the output of nand gate high. At this point sampling instant at V_2 has the optimum timing for symbol recovery. Hence, the base band processing circuit stops incrementing the sampling clock and symbol timing recovery is achieved.

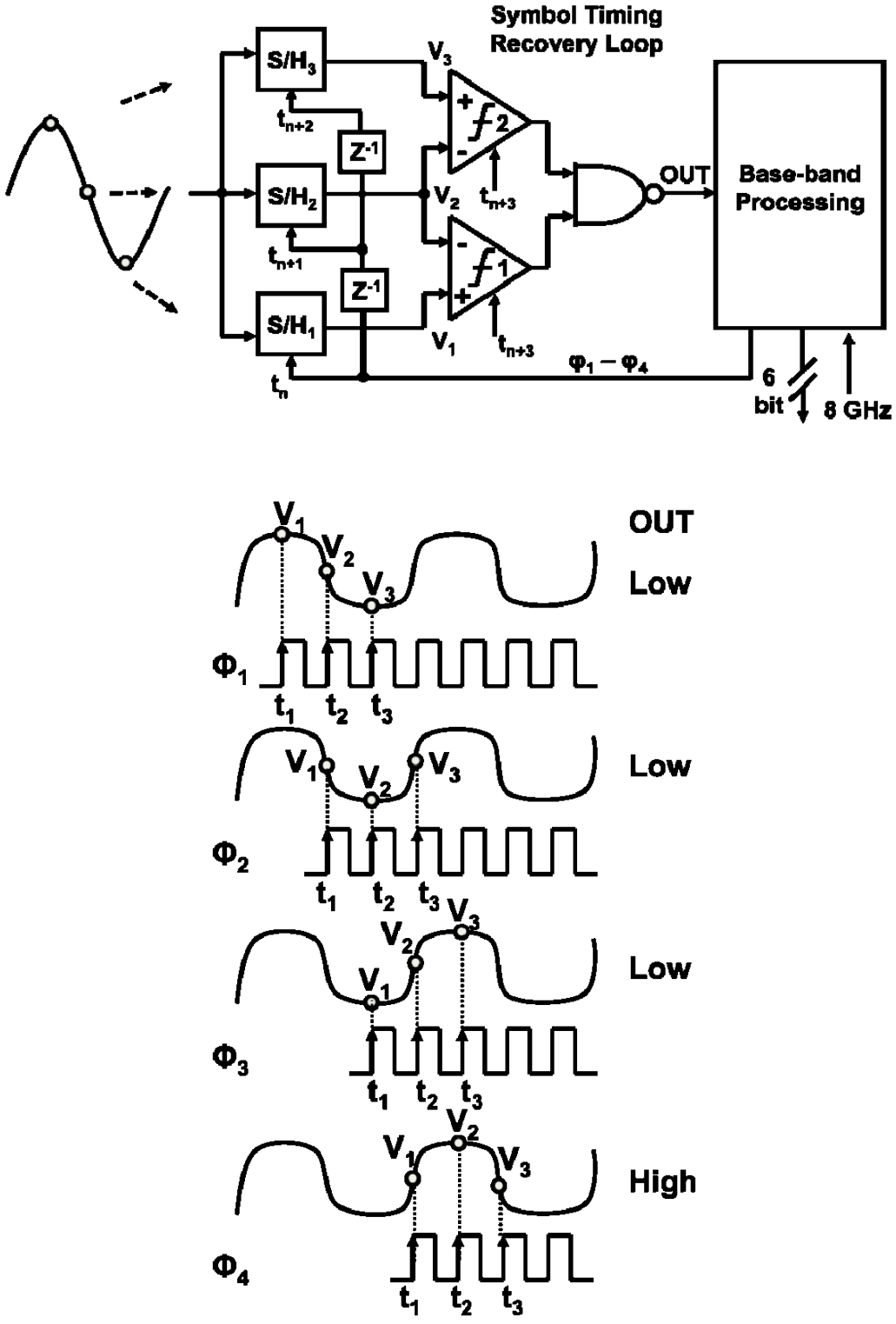

Figure 4.6 Timing diagram of symbol timing recovery in receiver.

The receiver in chapter 4 uses a high speed carrier and symbol timing recovery (CSTR) scheme. Since the data rate is 4 Gb/s and the base band processing circuit uses 8 GHz clock, the digital circuitry in the CSTR loop has a very short time of 125 ps for decision making. Furthermore, the PLL and phase interpolator must change phase within the time interval of 2 ns. Implementing this carrier and symbol timing recovery loop with the required timing precision is the most challenging part in the receiver design.

4.2.3 System Simulation

A link-budget estimation was carried out in order to check the feasibility of the transceiver system. The link budget estimation involves calculating the received signal power based on the transmitted power and path loss. A simple equation for path loss is

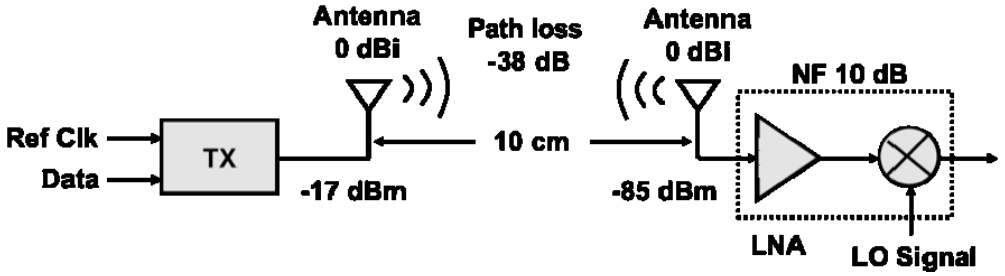

Figure 4.7 Link budget estimation for the transceiver front-end over a communication distance of 10 cm.

$$PL = 20\log_{10}\left(\frac{4\pi f_c d}{c}\right)\Lambda \quad (4.1)$$

Where, f_c is the frequency of the signal and d is the communication distance. For a distance of 10 cm, and center frequency of 16 GHz, the path loss is approximately -38 dB. With the transmitted power and path loss known, a rough estimation of received power can be obtained with the following equation.

$$\mathrm{P_r} = P_t + G_t + G_r - PL - NF - S - M\,\Lambda \quad (4.2)$$

Where, P_r and P_t are the received and transmitted signal powers, and G_t and G_r are the transmitter and receiver antenna gains respectively. *NF* is the combined noise figure of

the first two stages of receiver, S is the required SNR at the receiver and M is the link margin. The total transmitted power is limited by the FCC spectrum mask. The limit for maximum allowed transmitted power by FCC for UWB systems in the frequency range of 12-19 GHz is -51.3 dBm/MHz. Integrating it over a bandwidth of 4 GHz, the total transmitted power comes to be approximately -17 dBm. The required SNR at the last stage for BPSK modulation is 9 dB for BER of 10^{-5} and the link margin is assumed to be 10 dB. As shown in Figure 4.7, if the transmitter and receiver antennas are assumed to have a gain of 0 dBi each, and the combined noise figure of LNA and mixer is assumed as 10 dB, which is a reasonable assumption, then from equation 1 and 2, the received power at LNA input is roughly -85 dBm. This received power is well above the noise floor of -108 dBm for 4 GHz of bandwidth of BPSK signal. For a typical RF front-end circuit employing BPSK modulation, this power level is high enough for detection of the signal.

In BPSK modulation, the information in modulated signal is stored only in the phase of the waveform. In order to recover the data with minimum number of errors, it is important to preserve the phase of the carrier. In the transmitters based on BPSK modulation, the use of a PLL is thus apparent. However, PLLs usually have a finite phase noise which introduces jitter in the generated waveform. A simulation of the whole transceiver system was carried out in Matlab to see the effect of phase noise on the performance of the system. Simulink models of transmitter and receiver of Figure 4.1 and Figure 4.3 were created and the channel was modeled by the white Gaussian noise and path loss.

Figure 4.8 shows the effect of phase noise in PLL on the BER of system. It can be observed that the BER has sharp cutoff below the phase noise of 0.3 rms rad. The phase noise of 0.3 rms rad corresponds to 3 ps of jitter at 16 GHz. In order to limit the BER to less than 10^{-5}, the phase noise must be kept under 0.3 rms rad. Figure 4.9 shows the simulated eye diagram of recovered data at the rate of 4 Gb/s with phase noise of 0.3 rms rad. Due to their large bandwidths, ultra-wideband systems are robust to interference. Furthermore, since target communication distance is 10 cm, the interference from

surrounding environment can be neglected. Taking above factors into consideration, a transceiver system with requirement specifications as shown in Table 4-I is targeted.

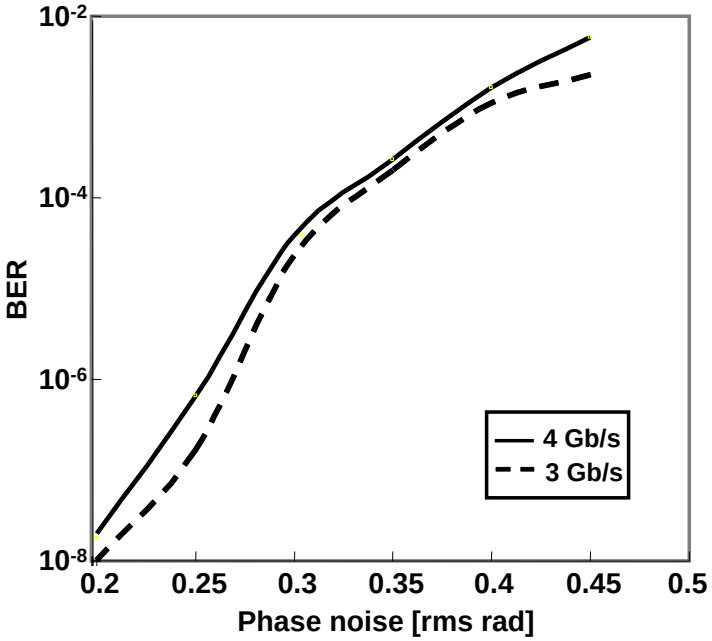

Figure 4.8 Effect of PLL phase noise on BER of system.

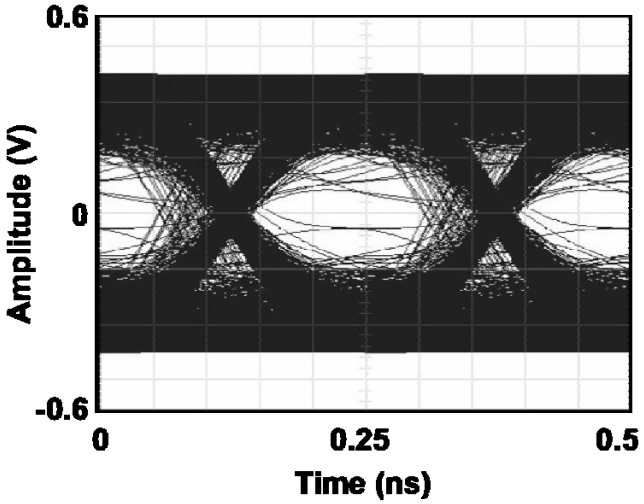

Figure 4.9 Simulated eye pattern of recovered data when PLL phase noise is 0.3 rms rad.

Table 4-I Transceiver requirement specifications.

Transmitter	Data rate	4 Gb/s
	Maximum power	-17 dBm
	RMS Phase jitter (@ 16 GHz)	3 ps
	Ramp-up time	40 ns
Receiver	Sensitivity	-85 dBm
	Front end (LNA + Mixer) noise figure	10 dB
	Front end gain	20 dB
	PLL lock time	40-50 ns
	Carrier recovery lock time	2 ns

4.3 Transmitter Implementation

As a first step towards the implementation of the transceiver discussed in section 4.2, a transmitter with PLL and an up-conversion mixer was designed and a test chip was fabricated to verify the transmitter performance.

4.3.1 Phase Locked Loop (PLL)

PLL is the most critical block in deciding the performance of the transmitter. Figure 4.10 shows the block diagram of 16 GHz charge-pump based phase locked loop. It includes a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a 16 GHz VCO and a 1/8 static frequency divider. The phase frequency detector compares a fed back frequency with a divided-down version of the reference frequency. The PFD's output current pulses are filtered and integrated to generate a voltage. This voltage drives an external voltage controlled oscillator (VCO) to increase or decrease the output frequency so as to drive the PFD's average output towards zero. While designing the PLL, parameters such as phase noise, lock time and reference spurs should be taken into consideration.

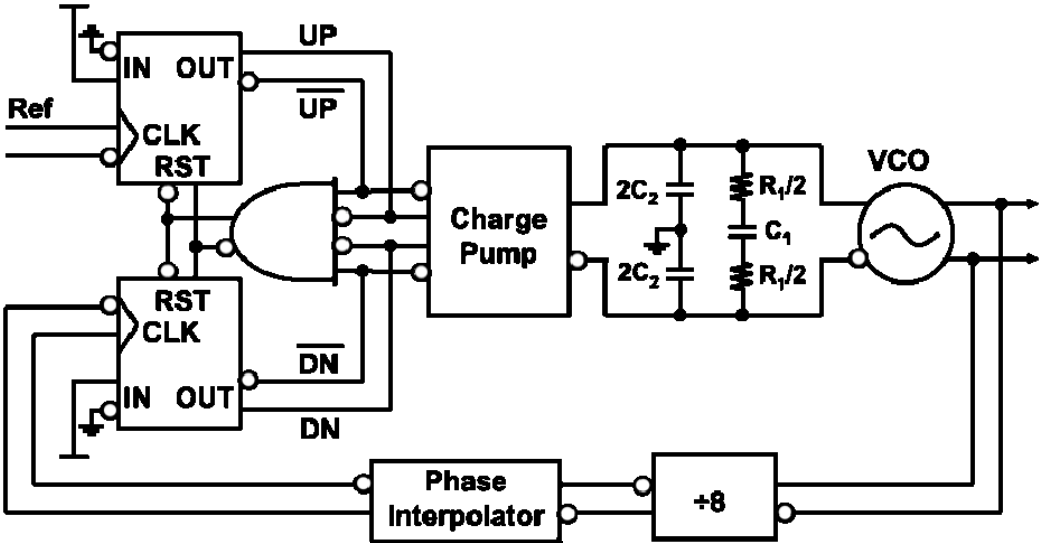

Figure 4.10 PLL schematic with phase frequency detector and loop filter.

In the PLL in proposed transmitter, all the blocks are designed using differential circuits as differential circuits are robust to noise compared to the single ended circuits. Furthermore, since the PLL is required to operate at high speed, all the logic gates in the PFD and frequency divider are designed with current-mode logic (CML) to obtain high-speed performance. The phase frequency detector is built using two D flip-flops and one Nand gate as shown. If the reference signal arrives first, the Up signal will be high and if the signal from VCO arrives first, the Dn signal will be high. The differential charge pump is similar to that reported in [14]. Figure 4.11 depicts the circuit schematic of the differential charge pump.

The differential Up and Down signals from PFD are converted into currents by the transistors M_4-M_5 and M_{17}-M_{18} respectively. When the UP signal is active, the current is pumped into the loop filter from VDD and when the Dn signal is active, the current is pumped to ground from the filter. When the loop is locked, no current flows through the output. This keeps charge pump from producing excessive noise. When the Up signal is high, transistor M_1 turns on. Current will then flow through M_4, M_1 and M_3 to ground. If the Dn signal is inactive, M_7 is off. The replica current is forced to leave the charge pump from the V_{out}+ terminal and then passes differentially through the loop filter and returns to the V_{out}- terminal.

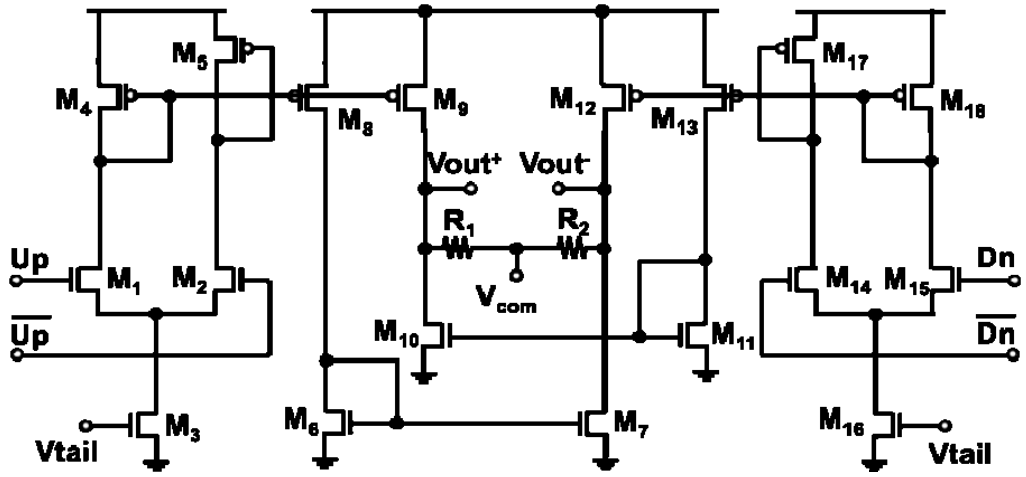

Figure 4.11 Circuit schematic of differential charge pump.

On the V_{out}- terminal, M_{12} is off, so the current has to flow to ground through M_{16}. Consequently, a differential voltage is present across the loop filter. A similar situation occurs when the down pulse is active.

V_{com} sets the common mode voltage at the loop filter through the resistors connected at the output. This helps in maintaining the differential voltage across the loop filter to a constant value when the PLL is in locked state. If the PLL is in the locked state, the differential voltage across the loop filter will be constant to maintain a stable output frequency from VCO. However, due to avoidable current drifts or mismatches in the charge pump, the common mode control voltage level of VCO control voltage will rise or fall. V_{com} prevents this from happening by pulling the average value of control voltage back to the right value through the resistors R_1 and R_2. The charging current is one of the factors that affect the loop bandwidth and it can be adjusted through V_{tail}. The current mirror transistors M_3 and M_{16} are kept long in order to obtain good control of tail current.

The low pass filter is second-order which makes the PLL a third-order type-II loop. A differential loop filter is required for the differential charge pump output. The values of C_1, C_2 and R_1 decide the loop bandwidth of the filter and are decided by the following equations.

$$C_1 = \frac{IK_{VCO}}{2\pi N\omega_n^{\,2}}\Lambda \quad (3)$$

$$R = 2\xi\sqrt{\frac{2\pi N}{IK_{VCO}C_1}}\Lambda \quad (4)$$

Where, N is the ratio of the two frequencies, I is the current from charge pump and ξ is the damping constant. The value of C_2 is kept 1/10 times that of C_1. The values of the MIM capacitors used in the loop filter are chosen so as to have a larger loop bandwidth and smaller chip area. The maximum dimensions of the MIM capacitor are kept less than 100 μm. Larger loop bandwidth is desirable since it allows faster lock time. With data rate of 4 Gb/s, a faster lock time reduces the training period in receiver for carrier synchronization. The loop bandwidth of 50 MHz is chosen for this reason. The loop filter output is connected to the voltage-controlled oscillator (VCO).

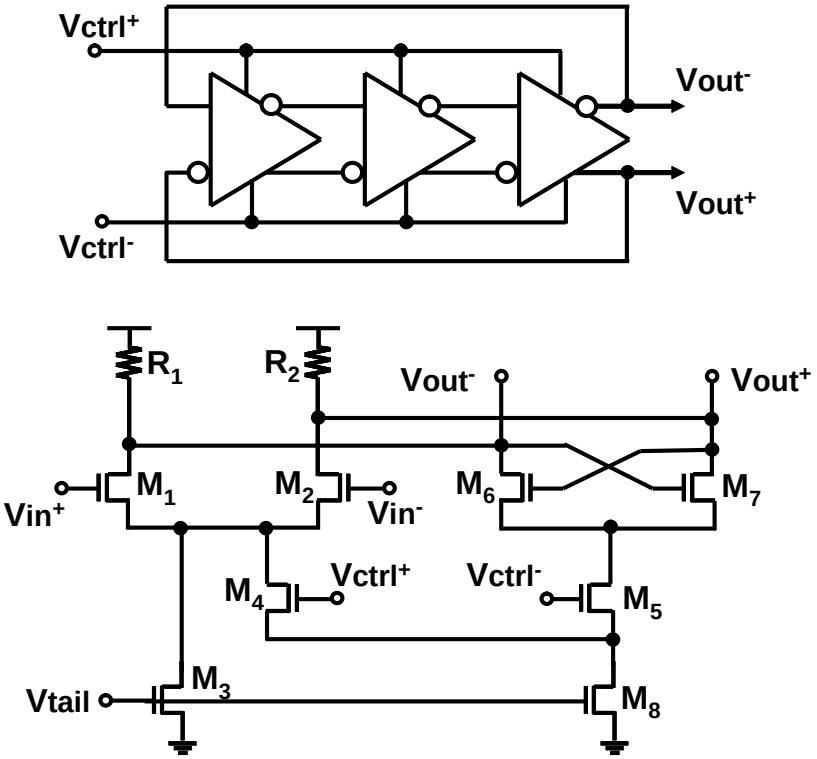

Figure 4.12 Ring oscillator block diagram and circuit schematic of delay buffer.

VCO is an important block in the PLL. As discussed in section 4.2.1, ring oscillator topology is used in this PLL instead of LC oscillator since the oscillator is required to operate at a very high speed. Also, with the use of ring oscillators, the need for high Q resonant elements is eliminated in addition to the reduction in on-chip area. Furthermore,

the ring oscillators have a wider tuning range which is very useful in design of UWB systems as they operate over a wide frequency range. Usually, the ring oscillator design requires connecting of number of inverters and feedback from the output of the last one to the input of the first one. The oscillation frequency is determined by the number of stages and delay in each stage. The VCO used in this transmitter is a fully differential ring oscillator composed of three variable delay inverters as shown in Figure 4.12. Differential circuit has a better immunity to common mode disturbances, and improved spectral purity. The circuit schematic of the differential variable delay inverter is similar to that reported in [15]. The oscillation frequency can be controlled by controlling the current flowing through transistors M_1 and M_2. This is done by changing the gate control voltages V_{ctrl}+ and V_{ctrl}-. The output voltage of loop filter is connected to these nodes. Transistors M_3 and M_8 provide tail current and resistors R_1 and R_2 form the load. The oscillation frequency of this VCO can be varied from 12 GHz to 19.5 GHz depending upon the control voltage and the tail current.

4.3.2 Up-conversion Mixer

The output of PLL is a constant frequency, which is mixed with base band data and converted to the BPSK, modulated output. The up-conversion mixer does this operation.

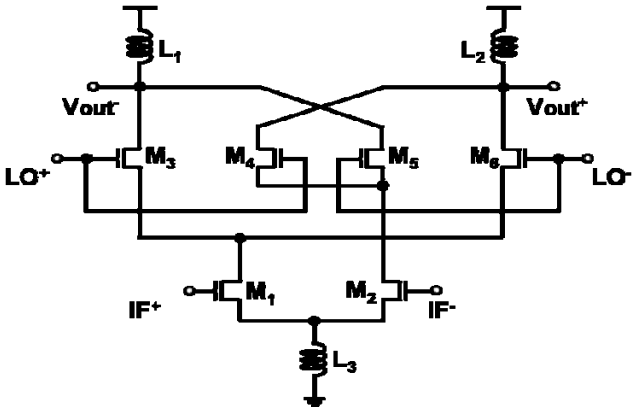

Figure 4.13 Differential mixer circuit schematic.

Figure 4.13 shows the circuit schematic of differential mixer. Since the base band data rate is very high, of the order of 4 Gb/s, a fast switching, highly linear mixer is

desirable. The mixer used in the transmitter has double balanced Gilbert cell topology. The upper and lower transistors in the Gilbert cell were sized such that they are fully switched to get maximum possible output swing. Transistors M_1 and M_2 are connected to the base band data and act as switches. The 16 GHz frequency signal from PLL is given to the LO port formed by transistors M_3-M_6. Inductors L_1 and L_2 form the load. The output of mixer is directly connected to the antenna. Since no power amplifier is used, the output impedance of mixer was designed to match the antenna (50 ohms).

4.4 Experimental Setup and Measured Results

Figure 4.14 shows chip micrograph with PLL and up-conversion mixer. The test-chip for transmitter was fabricated in 65nm CMOS technology with 12 metal layers and a supply voltage of 1.2 V. The die area of the transmitter is 0.29 mm^2.

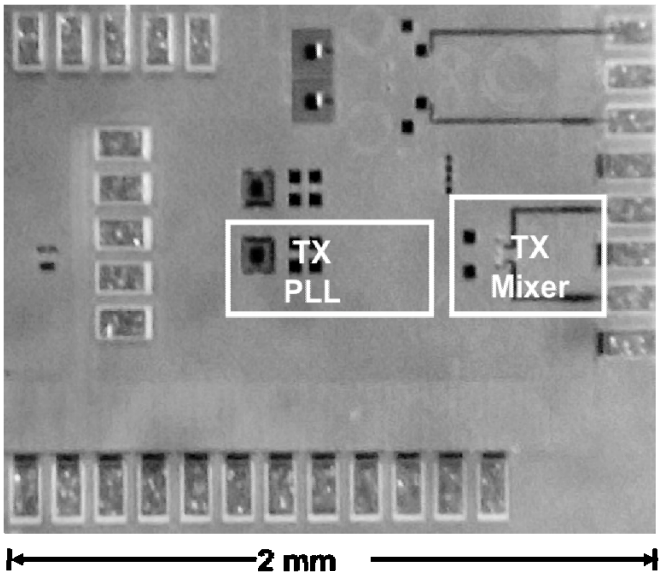

Figure 4.14 Chip photomicrograph.

The transmitter was tested on wafer and the output was measured using a 26.5 GHz spectrum analyzer. The maximum output power of PLL is -22 dBm at 16 GHz. The PLL has a wide locking range from 13.1 to 18.2 GHz. Figure 4.15 shows the frequency spectrum of PLL output measured using spectrum analyzer when PLL is locked at 16 GHz.

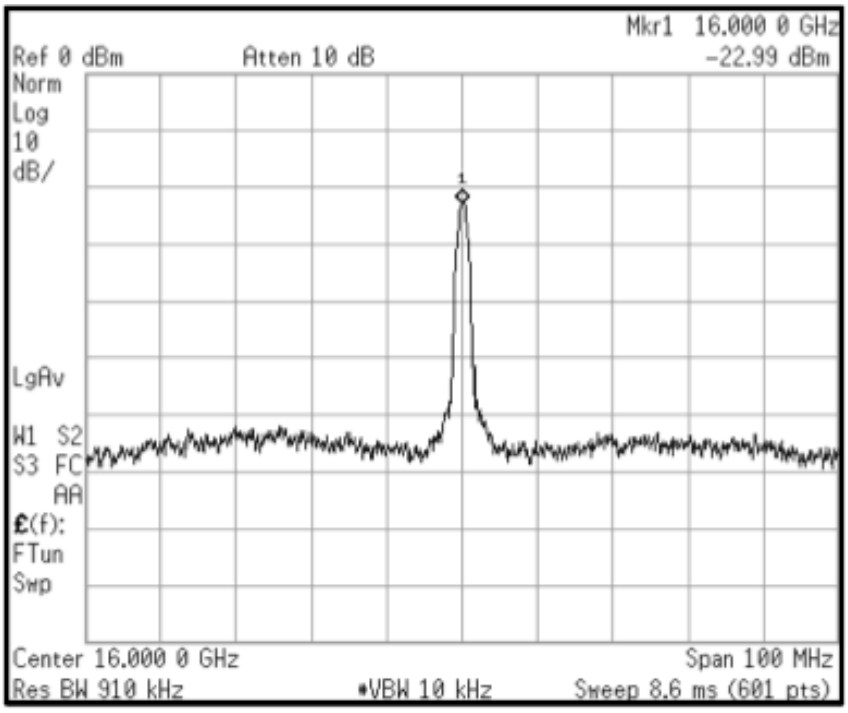

Figure 4.15 Measured frequency spectrum of PLL output.

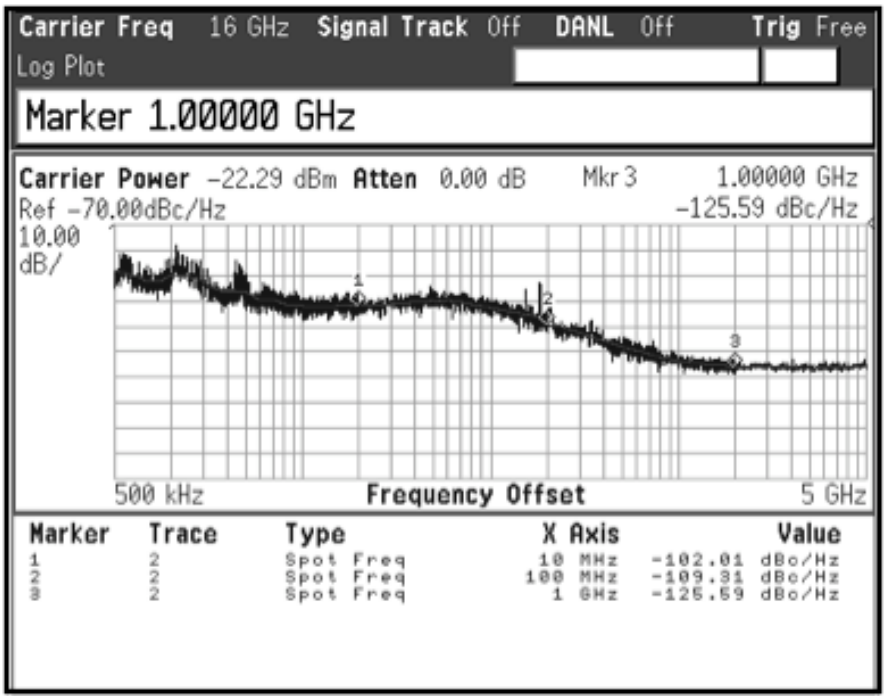

Figure 4.16 Measured PLL phase noise at 16 GHz.

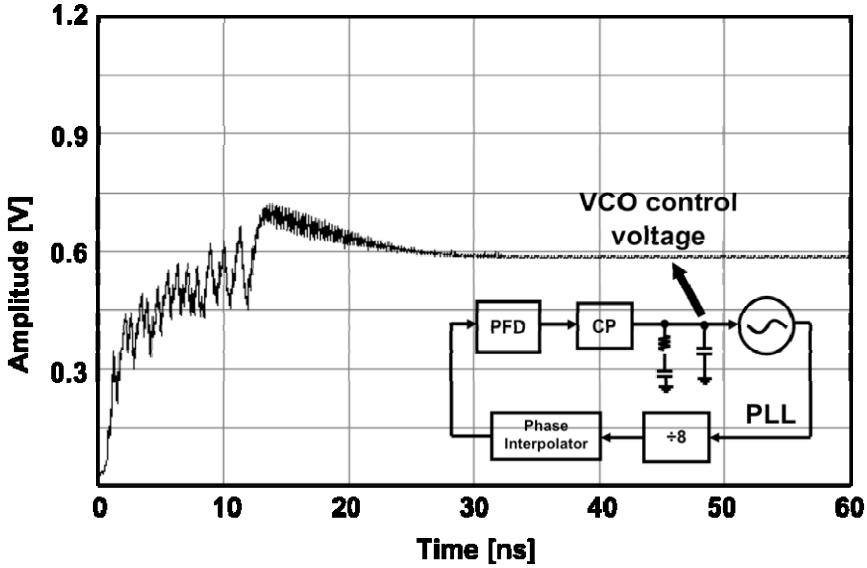

Figure 4.17 Simulated lock-up time of loop filter.

Figure 4.16 depicts the measured phase noise plot of the PLL. As there is no supply rejection circuit on chip, the noise from DC supplies also appears as phase noise. Phase noise greater than the offset of $1/100^{th}$ data rate is of importance because phase noise before this mark can be recovered by the symbol timing recovery circuit. The phase noise at 10 MHz, 100 MHz and 1 GHz offset from the carrier is about -102, -109 and -125 dBc/Hz respectively. This corresponds to less than 2 ps of rms phase jitter, which is low enough to maintain the BER lower than 10^{-5} as estimated in the system simulation in section 2.3.

The VCO core startup time found out by simulation was 0.8 ns. The simulated initial lock time for the PLL is about 40 ns, which corresponds to 160 symbols and the simulated time to lock after the phase interpolator output change (carrier recovery lock time) is approximately 2 ns, corresponding to 4 symbols. Figure 4.17 shows the simulated control voltage amplitude vs time. The PLL is locked when the control voltage presumes a constant value. From the figure, it can be seen that this stage reaches after 30 ns implying the locked state of PLL. The carrier recovery lock time in PLL is an important parameter since it decides the length of the training sequence for the carrier and symbol timing recovery loop. Lower lock time helps achieve carrier and symbol timing recovery faster reducing the training sequence length and increasing data rate

Figure 4.18 shows the time domain waveforms of the BPSK modulated signal for data rate of 4 Gb/s at mixer output. PRBS data pattern (2^{15}-1) was applied to the mixer input and the BPSK modulated output waveform was observed on the oscilloscope..

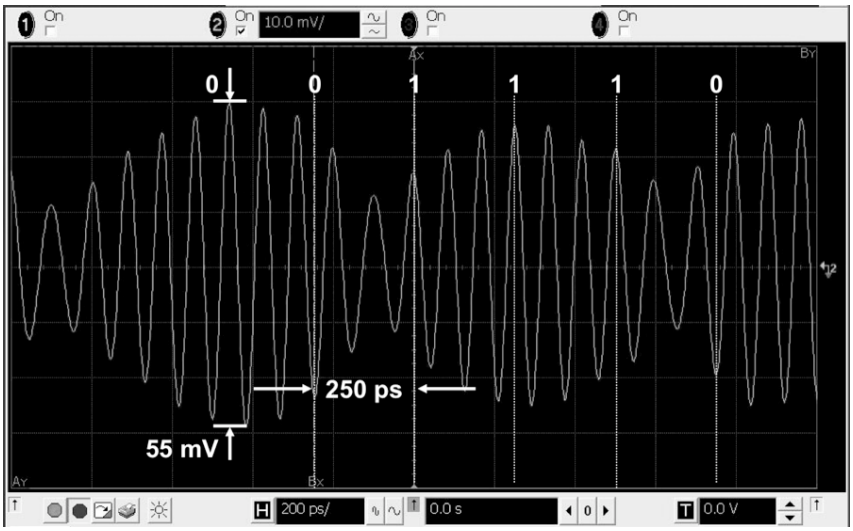

Figure 4.18 Measured time-domain waveform of transmitter output at 4 Gb/s.

The peak-to-peak amplitude of the measured waveform is 55 mV. Due to the bandwidth limitations of oscilloscope, the center frequency was changed to 12 GHz. Since the bandwidth of the oscilloscope is limited to 13 GHz, the output waveform has the effect of inter symbol interference (ISI).

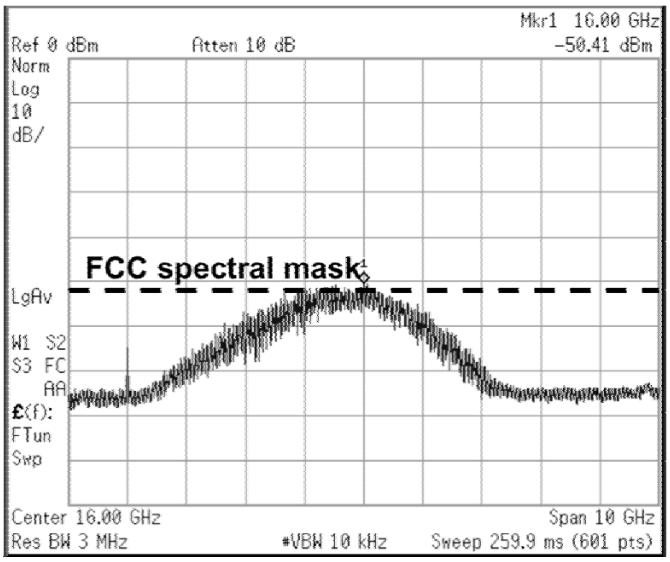

Figure 4.19 Measured BPSK modulated frequency spectrum of transmitter output at 4 Gb/s.

The frequency spectrum of BPSK modulated signal occupies 4 GHz of bandwidth with a peak at 16 GHz and maximum amplitude of -50.4 dBm as shown in Figure 4.19.

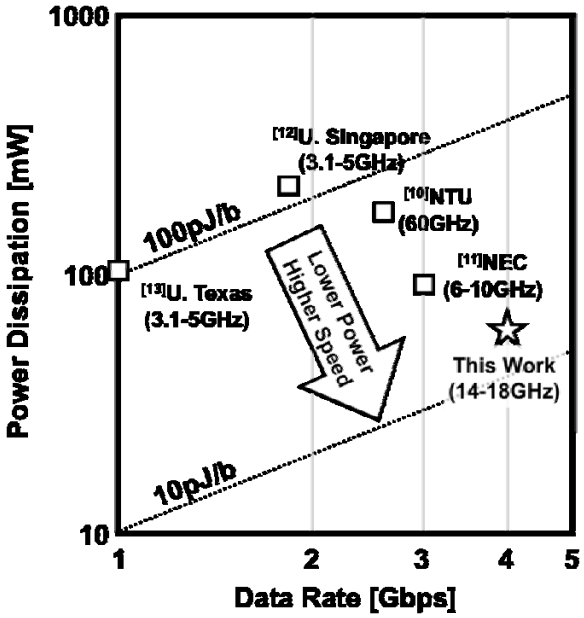

Figure 4.20 Comparison of transmitters operating over 1 Gb/s data rate within the communication distance of few cm.

Table 4-II Performance summary.

Technology	65nm CMOS
Layout area	0.29 mm^2
Supply voltage	1.2 V
Center frequency	16 GHz
Band of operation	14-18 GHz
PLL phase noise	-102 dBc/Hz @ 10MHz -122 dBc/Hz @ 1GHz
Maximum data rate	4 Gb/s
Power consumption	61 mW (at 4Gb/s) PLL : 55 mW VCO : 9 mW

The power consumption of the transmitter is 61 mW at 4 Gb/s with a 1.2 V supply. Figure 4.20 shows the comparison of transmitter in this work with the transmitters reported recently that operate at data rates exceeding 1 Gb/s, within a communication distance of few centimeters. The transmitter in this work has the lowest energy consumption of 15 pJ/b while reaching a maximum data rate of 4 Gb/s. The ring oscillator VCO consumes 9 mW while the PLL consumes 55 mW of power. Table 4-II summarizes the performance of the transmitter test chip.

4.5 Conclusion

A transceiver operating in the 14-18 GHz band is proposed. The transmitter uses a PLL and an up-conversion mixer to generate BPSK modulated signal. A receiver with direct conversion architecture and a high-speed carrier and symbol timing recovery scheme is proposed. The transceiver is designed to operate over a communication distance of 10 cm and its operation was verified by system simulation. The transmitter test chip was fabricated and its operation was verified with measured results. The effect of PLL phase noise on overall system performance was evaluated. The transmitter generated bi-phase modulated signal with a center frequency of 16 GHz at a maximum data rate of 4 Gb/s. The measured transmitter power consumption was 61 mW at the data rate of 4 Gb/s.

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Chapter 5 Summary

5.1 Summary

Short range, high-speed wireless is certainly the surging trend in communication systems today. The increasing demands of customers for higher data rate with more convenient platforms are forcing the development of new applications such as the UWB system and multi-band, multimode applications. Ultra-wideband (UWB) is a revolutionary approach for short-range wireless communications in that it has the potential for high data rates and low power systems. Unlike conventional wireless communication systems, UWB systems transmit and receive pulse-based waveforms compressed in time rather than sinusoidal waveforms compressed in frequency and offer data rates of several Gb/s over a communication distance of few cm. Furthermore, CMOS UWB transceiver achieves low power low cost compared with discrete component solution. UWB transceiver are classified into two categories namely, impulse radio (IR) UWB and multi-band OFDM. IR-UWB systems have simple architecture and are easy to implement than MB-OFDM systems and are well suited for low power operation.

Although UWB systems (3-10GHz) can reach several meters with data rates of up to 480 Mb/s and the millimeter wave systems have potential to reach up to several Gb/s, the front end circuits itself in these systems consume hundreds of milliwatts. Design of a transceiver that operates at a data rate of several Gb/s, while consuming power in the order of few tens of millwatts is essential. The dissertation addresses various design aspects of circuit design for the design of ultra-wideband transceivers and presents two major contributions in high-speed low-power short-range transceivers.

In chapter 2, design theory and issues for impulse radio ultra-wideband transceivers are discussed. Different UWB architectures and modulation schemes are investigated for high-speed low-power operation. It is observed that a coherent architecture with direct conversion and BPSK modulation scheme is best suitable for the realization of high-speed low-power IR-UWB transceiver since it has lower BER than PPM or OOK schemes. The possibilities of using an on-chip antenna as a future low cost solution for short distance wireless communication are investigated and design requirements of on-chip antenna are discussed. Due to the wavelength shortening effect the actual size of the antenna on

silicon substrate can be reduced. Various antenna topologies and structures such as dipole, monopole, and loop antenna are modeled with the help of 3-D field solvers. A test chip with three dipole antennas is fabricated and the antenna characteristics were measured. From measured results, it is observed that simple folded dipole has the highest efficiency and is best suitable for wideband operation in IR-UWB transceivers.

Chapter 3 demonstrates a 750 Mb/s CMOS IR-UWB transceiver with an optional embedded on-chip antenna, which is developed based on the design theory of chapter 2. The transceiver is designed to operate within 6-10 GHz band over a communication distance of 10 cm. The transmitter has a simple architecture consisting of a pulse generator and power amplifier. A novel pulse generator circuit is proposed which generates FCC compliant BPSK modulated pulses of 500 ps duration without any necessity of additional filter circuits resulting in extremely low power operation. Direct-conversion coherent receiver architecture is proposed in which a low noise amplifier amplifies the incoming RF signal, which is then mixed with the template pulses generated locally. The integrator and comparator follow the mixer, which process the signal further to obtain base-band data. The receiver operation is verified with simulation while the low-power transmitter is realized in 0.18 μ m CMOS process. The transmitter operation is verified with measured results. The transmitter operates at highest data rate of 750 Mb/s with energy consumption as low as 12 pJ/b. A monopole on-chip antenna is fabricated on chip and demonstrated for the operation over the 6-10 GHz band and a power amplifier is designed to drive the on-chip antenna.

Chapter 4 demonstrates a 4 Gb/s CMOS IR-UWB transceiver that operates over the quasi-millimeter-wave frequency band of 14-18 GHz. The transceiver uses coherent architecture. The transmitter uses a PLL an up-conversion mixer to generate BPSK modulated signal. Since the time interval between consecutive data bits is less for 4 Gb/s, the sinusoidal signal of 16 GHz is directly mixed with base-band data to generate the BPSK modulated signal. The receiver with direct conversion architecture and a novel high-speed carrier and symbol timing recovery scheme is proposed. Since the PLL is the common block in both transmitter and receiver and its phase noise has an impact on the overall performance of the system, a system simulation is carried out to estimate the

phase noise requirements of the PLL. A link-budget estimation is carried out to estimate the required power at transmitter and receiver sides. The transmitter power needs to be -17 dBm for the successful communication within a distance of 10 cm. The transmitter with PLL and up-conversion mixer was fabricated in 65 nm CMOS and its operation was verified with experimental results. The PLL generated 16 GHz center frequency with phase noise of -102 dBc/Hz at 10 MHz offset. The transmitter generates BPSK modulated signal at the maximum data rate of 4 Gb/s. The generated signal satisfies the FCC spectrum mask. The maximum power dissipation of the transmitter is 61 mW and consequently, for the data rate of 4 Gb/s, the energy per bit is 14 pJ/b. This is the highest data rate and lowest energy consumption among the transmitters reported at the publication of this work.

5.2 Scope of Future Work

Although the dissertation focuses on the UWB transceiver design, in both the transceivers proposed in this study only transmitter test chip was fabricated and its results were measured. Although, the receiver was designed and the successful operation of the transceivers was confirmed by simulation, the physical implementation of the receiver was not carried out. Since the receiver implementation is necessary to measure factors such as BER or the eye pattern of the recovered data, which are critical in deciding the performance of the transceiver, the test-chip implementation of the receiver remains part of the future work. Also, it would be interesting to implement the carrier and symbol timing recovery circuit proposed in the quasi-millimeter-wave transceiver.

The dissertation also discusses about the usage of on-chip antennas for the future low cost solution as a single chip system implementation. The performance of the on-chip antennas designed in this research was verified by simulation results like far field simulation and measured results such as return loss. However, parameters such as antenna gain and directivity, which are necessary to evaluate the overall performance of the antenna, were not evaluated due to the limitations in the measuring environment. The measurement of these parameters and the experiment of communication using on-chip antennas remain part of the future work.

List of Publications

1. Articles on periodicals

[1] V. V. Kulkarni, M. Muqsith, K. Niitsu, H. Ishikuro and T. Kuroda, "A 750Mb/s 12pJ/b 6-to-10GHz CMOS IR-UWB Transmitter with Embedded On-chip Antenna," *IEEE Journal of Solid-State Circuits*, Vol. 44, No. 2, pp. 394-403, Feb. 2009.

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2. Articles on international conference proceedings

[1] V. Kulkarni, M. Muqsith, H. Ishikuro and T. Kuroda, "A 12pJ/b 750Mb/s 6-t0-10GHz Digital UWB Transmitter," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 647-650, Sep. 2007.

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