SUMMARY OF Ph.D. DISSERTATION

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Title

Degradation characteristics of low-temperature polycrystalline silicon TFTs under electrical stress

Abstract

The demand for high-resolution displays is rising with the spread of multifunctional mobile phone (smart phone). Polycrystalline-silicon (poly-Si) TFTs produced by a low temperature processing are suitable for the high-resolution displays because electron mobility is several orders of magnitude higher in poly-Si TFTs than in amorphous silicon TFTs. This feature allows fabrication of a pixel array and peripheral circuits on the same glass substrate and, consequently, reduces the number of external LSIs. Due to the low process temperature, i.e., below 600 °C, numerous trap states remain at the poly-Si/gate-oxide interface and poly-Si grain boundaries. These trap states cause severe device degradation. In this study, degradation mechanism in n- and p-channel TFTs under dc and ac stress was analyzed and, degradation characteristics of poly-Si TFTs under actual circuit operation were clarified.

Chapter 1 summarizes the background and previous studies.

Chapter 2 describes feature and issue of poly-Si TFTs by comparing the fabrication process and device structure of poly-Si TFTs with that of single-crystalline Si MOSFET.

Chapter 3 describes the degradation characteristics of n-channel TFTs under dc and ac stress. In single drain (SD) structure, pronounced device degradation under ac stress was clarified. This degradation is incurred by drain-avalanche hot-carrier (DAHC) stress, which is accelerated by emitted electrons from trap states when a TFT is turned off. On the other hand, in regard to lightly doped drain (LDD) structure, the degradation is not accelerated by ac stress and is dominated by accumulated dc-DAHC stress.

Chapter 4 describes the degradation characteristics of p-channel TFTs under dc and ac stress. In dc stress, the degradation characteristics of poly-Si TFTs under negative-bias-temperature (NBT) stress were explained by a reaction-diffusion model as same as that of single-crystalline Si MOSFET. In ac stress, the device degradation was pronounced by repetition between electron injection and hole injection. Effective gate voltage negatively increases due to electron injection. As a result, NBT stress degradation caused by hole injection is locally accelerated.

The degradation characteristics of n- and p-channel TFTs under CMOS inverter operation are described in chapter 5. As for a high-speed circuit, suppression of the device degradation in p-channel TFTs becomes important. An increase in duty ratio of input pulse, which corresponds to a decrease in NBT-stress time, is required. Based on this result, an OLED display that integrates CMOS circuits was demonstrated.

Chapter 6 describes a technique for integration of reliability with high current drivability. A method called selectively enlarging laser crystallization (SELAX) is the effective way to improve TFT performance. It is shown that SELAX technique can improve both current drivability and reliability of TFTs by reducing power supply voltage.

Chapter 7 summarizes the results of this study.