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Keio University

Thesis Abstract

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Thesis Title

A Study on Energy-and-Area-Efficient Charge Redistribution Successive Approximation Analog-to-Digital Converters

Thesis Summary

In battery-powered mixed-signal applications including data communication and image processing systems, high performance analog-to-digital converters (ADC) are in great demand. This work aims to design medium resolution and moderate sampling rate ADCs with very low power consumption and small footprint. Energy and area savings are realized in several aspects. In architecture selection, charge redistribution based successive-approximation-register (SAR) architecture shows the highest power efficiency, benefiting from the structure containing only one active analog component. In circuit design, each of ADC building blocks is simplified and optimized to reduce power consumption and area. Split capacitor digital-to-analog converter (CDAC) is used to reduce input load capacitance and area. This work proposes a split CDAC calibration scheme to improve linearity performance. A bridge capacitor larger than conventional design is implemented so that a tunable capacitor can be added in parallel with the lower-weight capacitor array to compensate for mismatches. A tri-level charge redistribution scheme is proposed to reduce the CDAC switching energy and improve the settling speed. Differential capacitor bottom-plate charge-sharing technique is used to realize the third reference level without consuming extra power. The tri-level scheme also helps simplifying the SAR control logic circuits by eliminating the need for set-and-reset function. To avoid on-chip reference generation and therefore save power and cost, any reference voltage different from the supply voltage is removed. Asynchronous processing technique is used to eliminate power-hungry GHz clock generation and speed up the SAR algorithm as well.

The thesis is organized as follows:

Chapter 1 is an introduction of the overall study, starting from the data converter history and a variety of architectures. The trend in ADC design and the motivation of this research is summarized.

Chapter 2 presents the split CDAC calibration scheme. The issues of conventional split CDACs are analyzed, followed by the principle and implementation of the proposed calibration method. The feasibility is proved by the test chip measurement results.

Chapter 3 presents the tri-level charge redistribution scheme. The switching energy inefficiency and settling problem of the conventional method are first analyzed. Then the tri-level method and differential capacitor bottom-plate charge-sharing technique are introduced in details. The improvement of energy efficiency and settling speed are shown in simulation results.

Chapter 4 gives a high performance SAR ADC design, which combined the split CDAC calibration and the tri-level charge redistribution techniques. Circuit design details of each building block are provided. The ADC test chip implemented in a stand CMOS process is measured and compared with other state-of-the-art converters.

Chapter 5 summarizes the thesis and provides a prospect of future work.