A Study on Energy-and-Area-Efficient Charge Redistribution Successive Approximation Analog-to-Digital Converters

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Abstract

In battery-powered mixed-signal applications including data communication and image processing systems, high performance analog-to-digital converters (ADC) are in great demand. This work aims to design medium resolution and moderate sampling rate ADCs with very low power consumption and small footprint. Energy and area savings are realized in several aspects. In architecture selection, charge redistribution based successive-approximation-register (SAR) architecture shows the highest power efficiency, benefiting from the structure containing only one active analog component. In circuit design, each of ADC building blocks is simplified and optimized to reduce power consumption and area. Split capacitor digital-to-analog converter (CDAC) is used to reduce input load capacitance and area. This work proposes a split CDAC calibration scheme to improve linearity performance. A bridge capacitor larger than conventional design is implemented so that a tunable capacitor can be added in parallel with the lower-weight capacitor array to compensate for mismatches. A tri-level charge redistribution scheme is proposed to reduce the CDAC switching energy and improve the settling speed. Differential capacitor bottom-plate charge-sharing technique is used to realize the third reference level without consuming extra power. The tri-level scheme also helps simplifying the SAR control logic circuits by eliminating the need for set-and-reset function. To avoid on-chip reference generation and therefore save power and cost, any reference voltage different from the supply voltage is removed. Asynchronous processing technique is used to eliminate power-hungry GHz clock generation and speed up the SAR algorithm as well.

The thesis is organized as follows:

Chapter 1 is an introduction of the overall study, starting from the data converter history and a variety of architectures. The trend in ADC design and the motivation of this research is summarized.

Chapter 2 presents the split CDAC calibration scheme. The issues of conventional split CDACs are analyzed, followed by the principle and implementation of the proposed calibration method. The feasibility is proved by the test chip measurement results.

Chapter 3 presents the tri-level charge redistribution scheme. The switching energy inefficiency and settling problem of the conventional method are first analyzed. Then the tri-level method and differential capacitor bottom-plate charge-sharing technique are introduced in details. The improvement of energy efficiency and settling speed are shown in simulation results.

Chapter 4 gives a high performance SAR ADC design, which combined the split CDAC calibration and the tri-level charge redistribution techniques. Circuit design details of each building block are provided. The ADC test chip implemented in a stand CMOS process is measured and compared with other state-of-the-art converters.

Chapter 5 summarizes the thesis and provides a prospect of future work.

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Chapter 1 Introduction

1.1 Background

1.1.1 ADC History

It is difficult to define the exact time when the first data converter was invented. According to [1], the earliest recorded data converter may be traced back to 18th century. Instead of being electronic, it was hydraulic. At that time, Turkey had problems with its public water supply and designed sophisticated water-metering systems. Binary-weighted nozzles were used to control the water output from reservoirs, which was functionally a DAC with manual (rather than digital) input and a wet output. There may be other examples of early data converters, but this thesis will focus attention on electronic data converters.

The most significant driving force behind the development of electronic data converters has been the field of communication. The proliferation of telegraph and telephone in late 19th century, and the rapid demand for more capacity, led to the need for multiplexing more than one signal onto a single pair of conductors. Pulse code modulation (PCM) was first proposed in a patent by P. M. Rainey of Western Electric in 1921 [2]. An electro-optical-mechanical fax telegraph system was proposed in this patent, which illustrated the fundamentals of PCM including quantization using a flash ADC, serial data transmission and reconstruction of the quantized data using a DAC. However, the invention generated little interest until several years later many other PCM patents had been issued. In 1939, PCM was re-invented by A. H. Reeves of the International Telephone and Telegraph Corporation taking full advantage of vacuum tube technology, which covered a design of the first all-electronic ADC and DAC on record [3]. Both the ADC and DAC were based on 5-bit counters. Starting from 1940 and during World War II, researches were conducted on speech encryption systems that made PCM techniques crucial and many significant developments came out of several groups at Bell Laboratories. The first mention of the successive approximation ADC architecture in the context of PCM was by J. C. Schelleng in a patent filed in 1946 [4]. Despite of the rather cumbersome and impractical vacuum tube design, the operation of the ADC followed the fundamental successive approximation algorithm. A more elegant implementation of successive approximation ADC was described

by Goodall in a 1947 article [5]. The ADC digitized the entire voice band to 5-bits, sampling at a rate of 8-kS/s. The invention of electron beam coding tube by R. W. Sears in 1948 significantly improved ADC technology [6]. The tube was the first electronic flash converter delivering a parallel output, capable of sampling at 96-kS/s with 7-bit resolution. The electron tube coding technology reached its peak in the mid-1960s with an experimental 9-bit and 12-MS/s coder [7].

Data converters were very expensive, bulky and hungry for power because of the vacuum tube technology, and they had no commercial use until the advent of the digital computer. Although the early driving force behind digital computers were military applications such as ballistic trajectory computation, as time went on, other applications in the area of data analysis, measurement and industrial process control created more general interest in data processing, and therefore the need for data converters. As electronic circuit designs migrated from vacuum tubes to transistors, there was more and more interest in solid-state designs of data conversion products.

It is interesting to find that all the fundamental ADC architectures used today had been discovered and published in one form or another by the mid-1960s. Because of the complexity of constructing an all-parallel flash converter using either vacuum tube or transistors, subranging architecture was proposed to simplify conversion process by R. Staffin and R. D. Lohman in a 1956 patent [8]. In order to reliably achieve higher than 8-bit resolution using the subranging approach, a digital error correction technique was disclosed in literature as early as 1964 by T. C. Verster [9] and quickly became widely known and utilized. A 7-bit 9-MS/s pipelined converter using three individual 3-bit stages with error correction was proposed in 1966 [10]. Even the sigma-delta ($\sum$-Δ) ADC architecture had been explored in the early development phases of PCM systems, specially those related to transmission techniques called delta modulation and differential PCM. In 1954 C. C. Cutler of Bell Laboratories filed a significant patent which introduced the principle of oversampling and noise shaping with the specific intent of achieving higher resolution [11]. In 1962, Inose, Yasuda, and Murakami elaborated on the single-bit oversampling noise-shaping architecture proposed by Cutler, using solid-state devices to implement first and second-order sigma-delta modulators [12]. The paper was the first to use the name delta-sigma to describe the architecture. The name delta-sigma stuck until the 1970s when AT&T

engineers began using name sigma-delta. Since then, both names have been used. Table 1.1 shows a timeline for the development of ADC architectures. A more detailed discussion of the ADC architectures will be given in Chapter 1.1.2.

From 1970, data converter market began to be driven by a number of applications, such as high resolution digital voltmeter, industrial process control, digital video, medical imaging and vector scan display. Most of these systems had previously utilized analog signal processing technology. The increased availability of low cost computation aroused a desire to take advantage of the increased performance and flexibility offered by digital signal processing technology, and hence the interest for compatible data conversion products. The data converters of the 1970s made maximum utilization of all the technologies available: monolithic, module and hybrid. The early commercially available monolithic data converters were mainly processed by conventional bipolar linear processing techniques. In the early 1970s, 10-bit conversion had been difficult to obtain with good yields and low cost because of the finite β of switching devices, the V_{BE}-matching requirement, the matching and tracking requirements on the diffused resistor ladders, and the tracking limitations caused by the thermal gradients generated by high internal power dissipation. Most of these problems were solved or avoided with CMOS devices. The CMOS transistors have nearly infinite current gain, eliminating β problems. There is no equivalent in CMOS circuitry to a bipolar transistor's V_{BE} drop. Instead, a CMOS switch in the "on" condition is almost purely resistive, with resistance value controlled by device geometry. The temperature problems of diffused resistors were eliminated by using thin film resistors instead. Nevertheless, since the monolithic technology of the period was not yet capable of supporting the high-end converter functions in single-chip form, hybrid and module techniques were developed to manufacture lower cost more compact high performance data converters. There were a variety of components from which hybrid and module data converter designers could choose, including IC op amps, IC DACs, comparators, discrete transistors, various logic chips, and etc.

Table 1.1 ADC Architecture Timeline.

Year	ADC architecture
1939	Counting [3]
1946	Successive approximation [4]
1948	Flash (electron tube coders) [6]
1956	Subranging [8]
1962	Sigma-delta [12]
1966	Pipeline [10]

The 1980s represented high growth years for data converters. The driving market forces were instrumentation, data acquisition, medical imaging, professional and consumer audio and video, computer graphics, and a lot of others. Relatively low-cost microprocessors, high-speed memory, digital signal processors (DSP), and the emergence of IBM-compatible PCs increased the interest of all areas of signal processing. The emphasis in ADCs began to rapidly shift to include ac performance and wide dynamic range, and hence the demand for sampling ADCs at all frequencies. Specification such as signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), effective number of bits (ENOB), spurious-free dynamic range (SFDR), aperture time jitter, etc., began to appear on most ADC data sheets. Time interleaving of multiple ADCs was first introduced by Black and Hodges in 1980, which offers a conceptually simple method for multiplying the sampling rate of existing high performance ADCs [13]. The monolithic sampling ADC emerged in the mid-1980s. The addition of sample-and-holds, references, and buffer amplifiers was made considerably easier with the addition of bipolar capability to the CMOS process (BiCMOS). The first commercial monolithic delta-sigma ADC was actually offered in 1988, despite the fact that the basic delta-sigma architecture had been well known since the 1960s. The demand for hybrid and module data

converters peaked in the 1980s, mainly because they held lead time of 3~5 years compared to single-chip monolithic converters with equivalent performance. A large number of flash converters and other components served as building blocks for higher resolution subranging ADCs.

The markets influencing data converters in the 1990s were even more diverse and demanding. Communications became an even larger driving force for low-cost, low-power, high-performance data converters in modem, cell phone handsets, and wireless infrastructures. Other trends were the emphasis on lower power and single supply voltages for portable battery-powered applications. While the reduced power supply voltages were compatible with the higher speed, lower voltage processes, the reduced signal range and headroom made the converter designs more sensitive to noise. In the 1990s, CMOS became the process-of-choice for general purpose data converters, with BiCMOS reserved for the high-end devices. A major process technology shift occurred in the 1990s, when parasitics ultimately became the performance-limiting factor for high-speed chip-and-wire hybrid data converters. The newer ICs, with their smaller feature size and reduced parasitics, allowed them to achieve higher level performance than attainable in a chip-and-wire hybrid or a module, which was opposite to the situation that existed throughout the 1970s and most of the 1980s. Monolithic pipelined subranging ADCs virtually replaced the high power flash ADCs of the 1980s in frequency-domain signal processing applications. Because of the ease with which digital functionality can be added to BiCMOS or CMOS data converters, there have been an increasing number of highly integrated application-specific ICs during the 1990s and continuing to this day.

The trends of data converters started in the 1990s have continued to the 2000s. Power dissipation has dropped, and along with it, power supply voltages. Supplies of 5-V, 3.3-V, 2.5-V, 1.8-V and 1.2-V parts have followed as CMOS line spacing shrank to 0.6μm, 0.35μm, 0.25μm, 0.18μm, 90nm and 65nm, which has made data converter designs more and more challenging.

1.1.2 ADC Architectures

As introduced in the previous section, large numbers of signal types to be digitized have led to a diverse selection of data converters in terms of architectures. A 1-bit ADC is simply a comparator. If the input is above a threshold, the output has one logic output, below it has another. There is no ADC architecture which does not use at least one comparator of some sort.

Flash ADC

Flash ADCs, sometimes also called parallel ADCs, are the fastest type of ADC and use a large number of comparators [14-16]. An *N*-bit flash ADC consists of 2^N-1 comparators arranged in parallel. Each comparator has a reference voltage generated from a resistor string which is 1LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a "1" logic output, and all the comparators above that point will have the input voltage smaller than their reference voltage and a "0" logic output. The 2^N-1 comparator outputs therefore behave in a way similar to a mercury thermometer, and the output code at this point is sometimes called a thermometer code. Since 2^N-1 data outputs are not really practical, they are processed by a decoder to generate an *N*-bit binary output.

The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder *N*-bit output by only a few gate delays on top of that, so the process is very fast. However, the architecture uses large numbers of resistors and comparators, and is limited to low resolutions. If it is to be fast, each comparator must run at relatively high power levels. Therefore, the problems of flash ADCs include limited resolution, high power dissipation because of the large number of high speed comparators, and relatively large chip size and thus high cost. In addition, the resistance of the reference resistor chain must be kept low to supply adequate bias current to the fast comparators, so the voltage reference has to source quite large currents. Figure 1.1 shows a 3-bit flash ADC example.

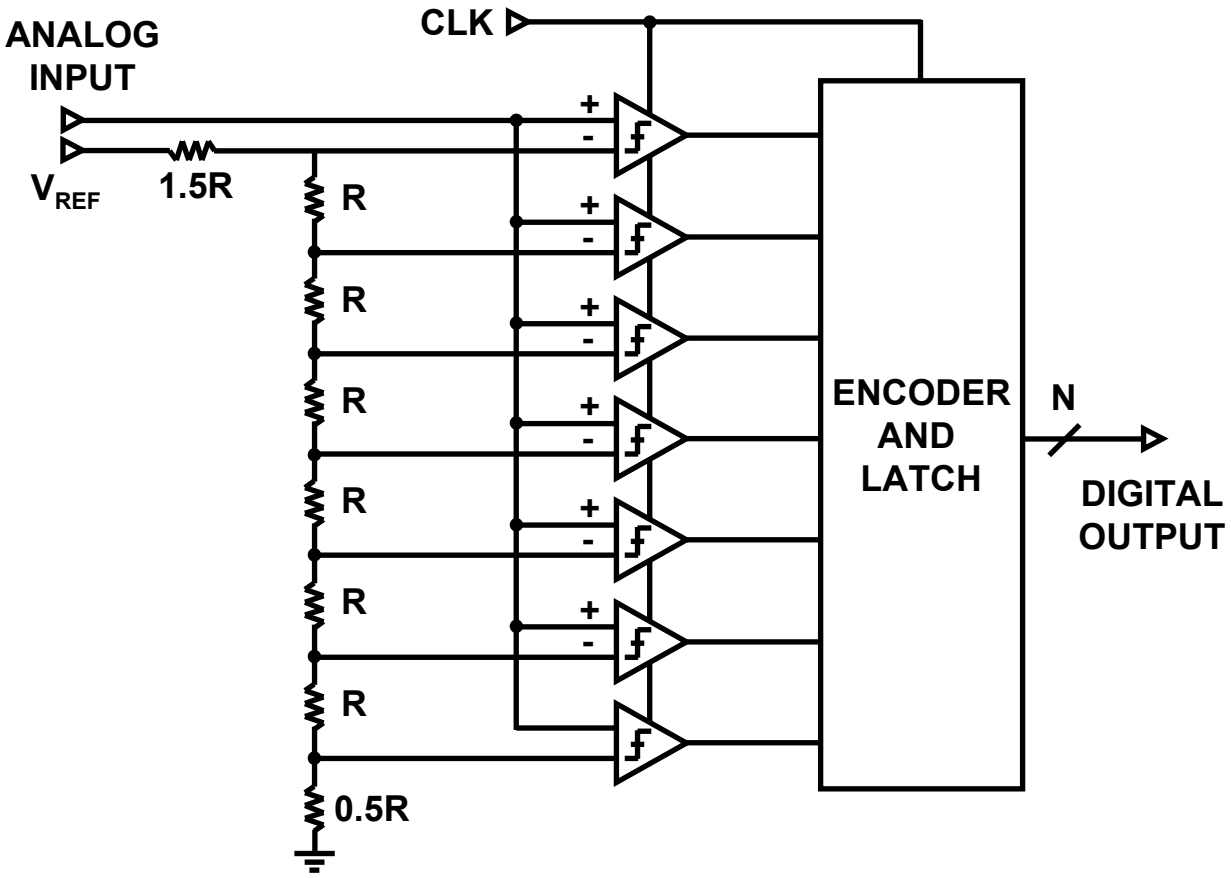


Figure 1.1 3-bit Flash ADC.

Subranging ADC

Subranging architecture has been used to reduce the component count and power of flash ADCs [17-19]. A basic two-stage *N*-bit subranging ADC is shown in Figure 1.2. The ADC is based on two separate conversions, a coarse conversion (*N1*-bit) in the MSB sub-ADC (SADC) and a fine conversion (*N2*-bit) in the LSB sub-ADC. The conversion process begins with the sample-and-hold circuit in the hold mode followed by a coarse *N1*-bit SADC conversion of the MSBs. The digital outputs of the MSB converter drive an *N1*-bit sub-DAC (SDAC) which generates a coarsely quantized version of the analog input signal. The output of the *N1*-bit SDAC is subtracted from the held analog input, amplified and applied to the *N2*-bit LSB SADC. The amplifier provides gain, *G*, sufficient to make the residue signal exactly filled the input range of the *N2*-bit SADC. The output data from the *N1*-bit SADC and *N2*-bit SADC are latched into the output registers yielding the *N*-bit digital output code, where $N = N1 + N2$.

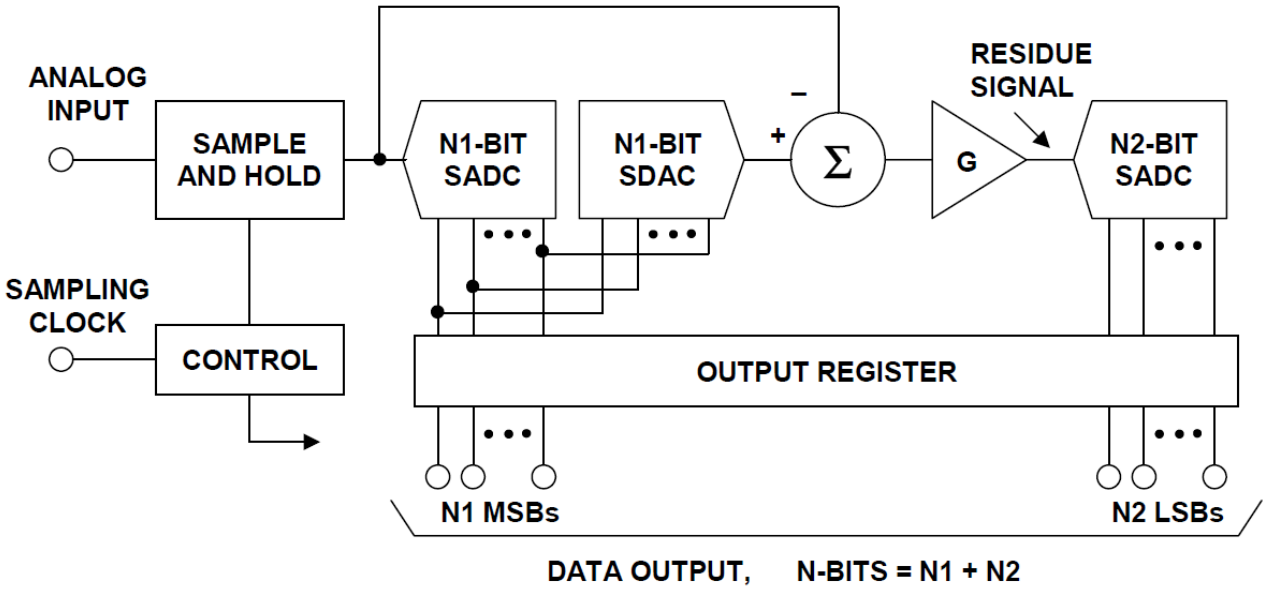
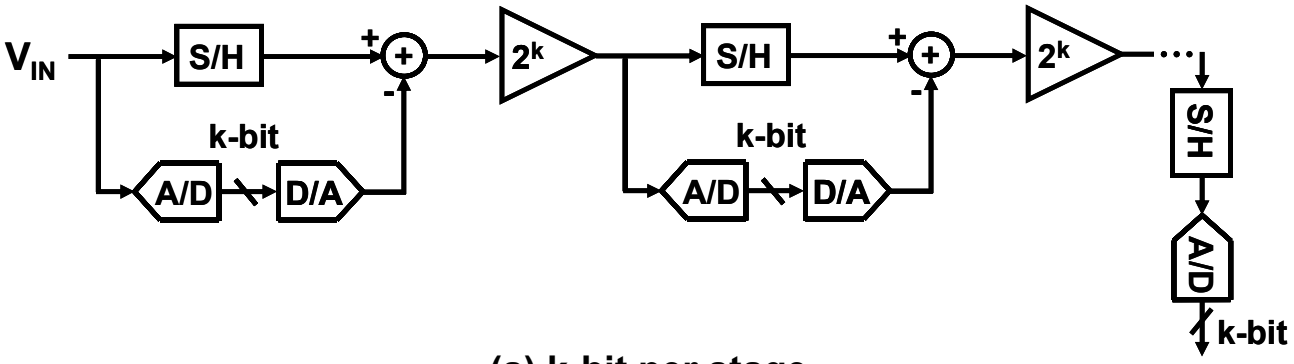


Figure 1.2 N-bit Two-Stage Subranging ADC.

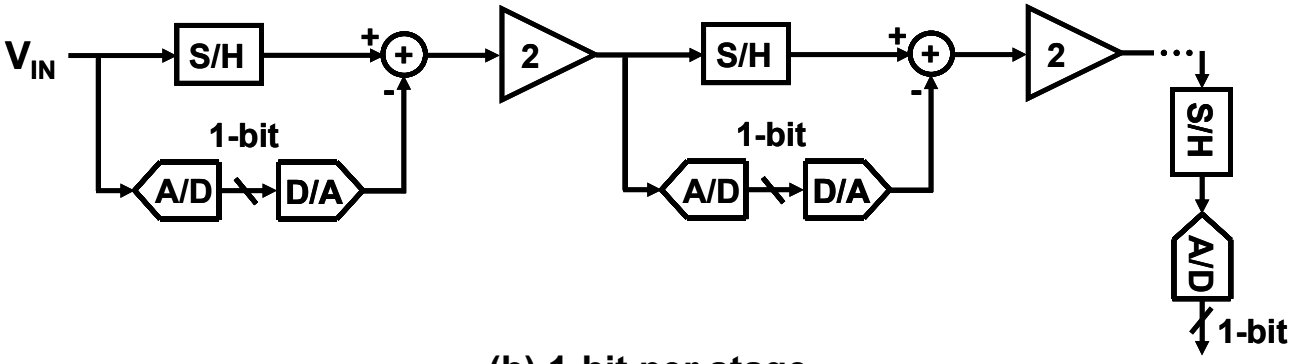
Pipelined ADC

The term "pipelined" architecture refers to the ability of one stage to process data from the previous stage during any given clock cycle. At the end of each phase of a particular clock cycle, the output of a given stage is passed on to the next stage using the sample-and-hold (S/H) functions and new data is shifted into the stage. Figure 1.3 (a) shows a pipelined ADC designed with identical stages of *k*-bit each. This architecture uses the same core hardware in each stage. Figure 1.3 (b) shows the simplest form of this architecture where $k = 1$. Design complexity of the pipelined ADC increases linearly, rather than exponentially, with the number of bits [20].

It is often erroneously assumed that all subranging ADCs are pipelined. While it is true that most modern subranging ADCs are pipelined in order to achieve the maximum possible sampling rate, they don't necessarily have to be pipelined if designed for use at much lower speed.



(a) k-bit per stage



(b) 1-bit per stage

Figure 1.3 Basic Pipelined ADC with Identical Stages.

Successive Approximation ADC

Figure 1.4 shows the basic successive approximation architecture [21-23]. It performs conversion on command. The "CONVERT START" command places the sample-and-hold (SHA) in the hold mode, and all the bits of the successive approximation register (SAR) are reset to "0" except the MSB which is set to "1". The SAR output drives the internal DAC. If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The next most significant bit is then set to "1". If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The process repeats with each bit in turn. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the value of the analog input and the conversion is complete. The end of conversion is generally indicated by an end-of-convert (EOC) signal.

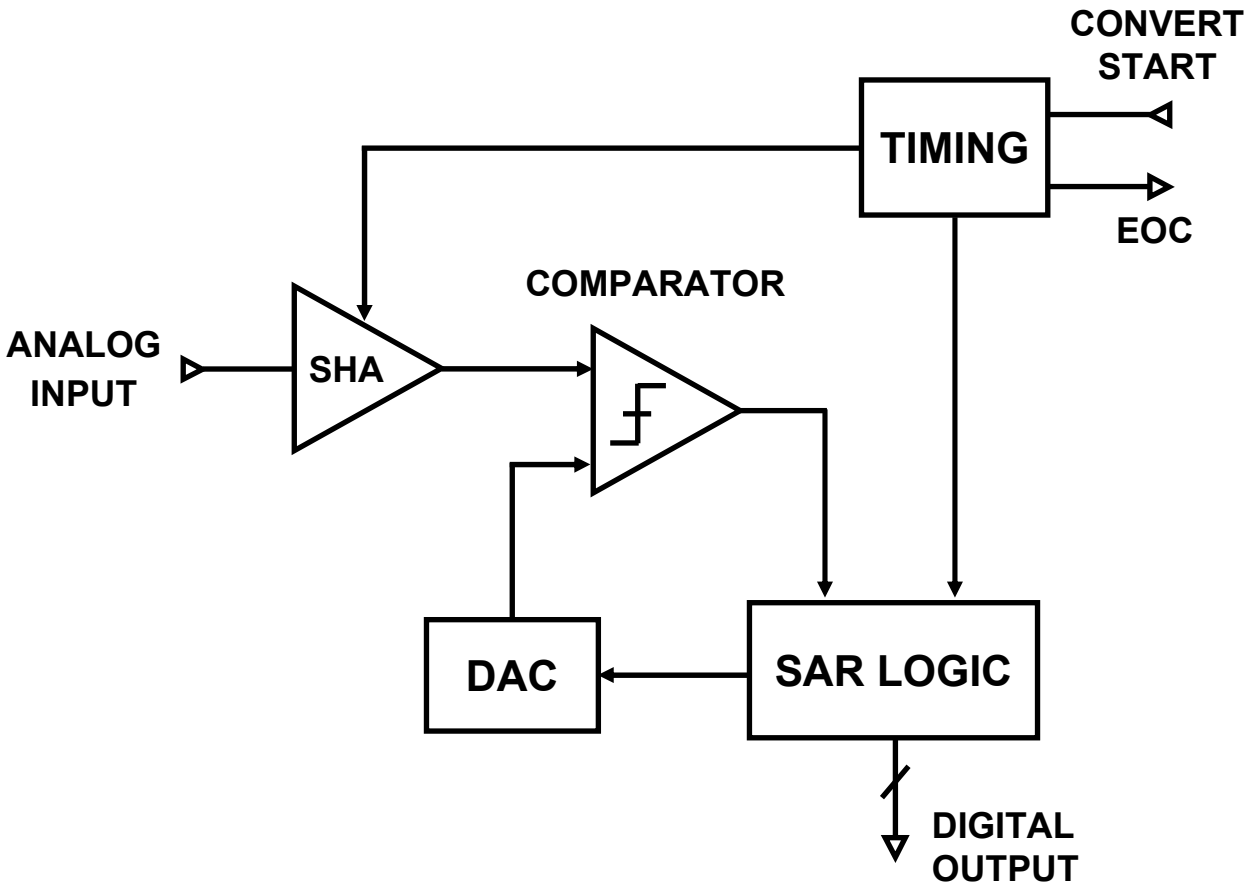
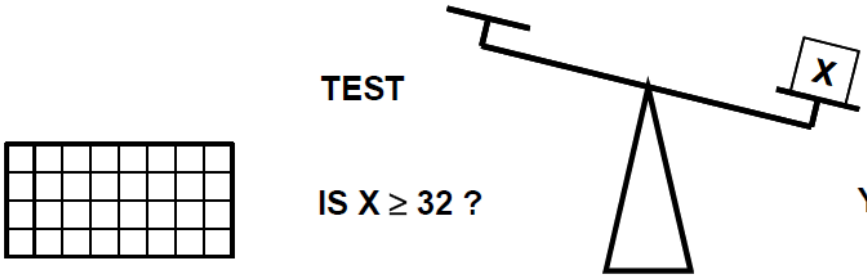


Figure 1.4 Basic Successive Approximation ADC.

The basic algorithm used in the successive approximation ADC conversion process dates back to the 1500s relating to the solution of a certain mathematic puzzle relating to the determination of an unknown weight by a minimal sequence of weighing operations [24]. In this problem, the object is to determine the least number of weights which would serve to weigh an integral number of pounds from 1 lb to 40 lb using a balance scale. One solution put forth by the mathematician Tartaglia in 1556, was to use the series of weights 1 lb, 2 lb, 4 lb, 8 lb, 16 lb, and 32 lb. The proposed algorithm is the same as used in modern successive approximation ADCs. This solution will actually measure unknown weights up to 63 lb rather than 40 lb as stated in the problem. The algorithm is shown in Figure 1.5 where the unknown weight is 45 lb. The balance scale analogy is used to demonstrate the algorithm.



	TEST	ASSUME X = 45	
▦	IS X ≥ 32 ?	YES → RETAIN 32 →	1
▥	IS X ≥ (32 +16) ?	NO → REJECT 16 →	0
▤	IS X ≥ (32 +8) ?	YES → RETAIN 8 →	1
▣	IS X ≥ (32 +8 + 4) ?	YES → RETAIN 4 →	1
▢▢	IS X ≥ (32 +8 + 4 + 2) ?	NO → REJECT 2 →	0
▢	IS X ≥ (32 +8 + 4 + 2 + 1) ?	YES → RETAIN 1 →	1

TOTALS: X = 32 + 8 + 4 + 1 = 45_{10} = 101101_2

Figure 1.5 Successive Approximation ADC Algorithm.

Sigma-Delta ADC

The basic single and multi-bit first order sigma-delta ADC architecture is shown in Figure 1.6 (a) and (b), respectively. The comparator output is converted back to an analog signal with a 1-bit DAC (a comparator), and subtracted from the input signal. The error signal passes through an integrator. The basic oversampling sigma-delta modulator increases the overall signal-to-noise ratio at low frequencies by shaping the quantization noise such that most of it occurs outside the bandwidth of interest. The digital filter then removes the noise outside the bandwidth of interest, and the decimator reduces the output data rate back to the Nyquist rate [25, 26].

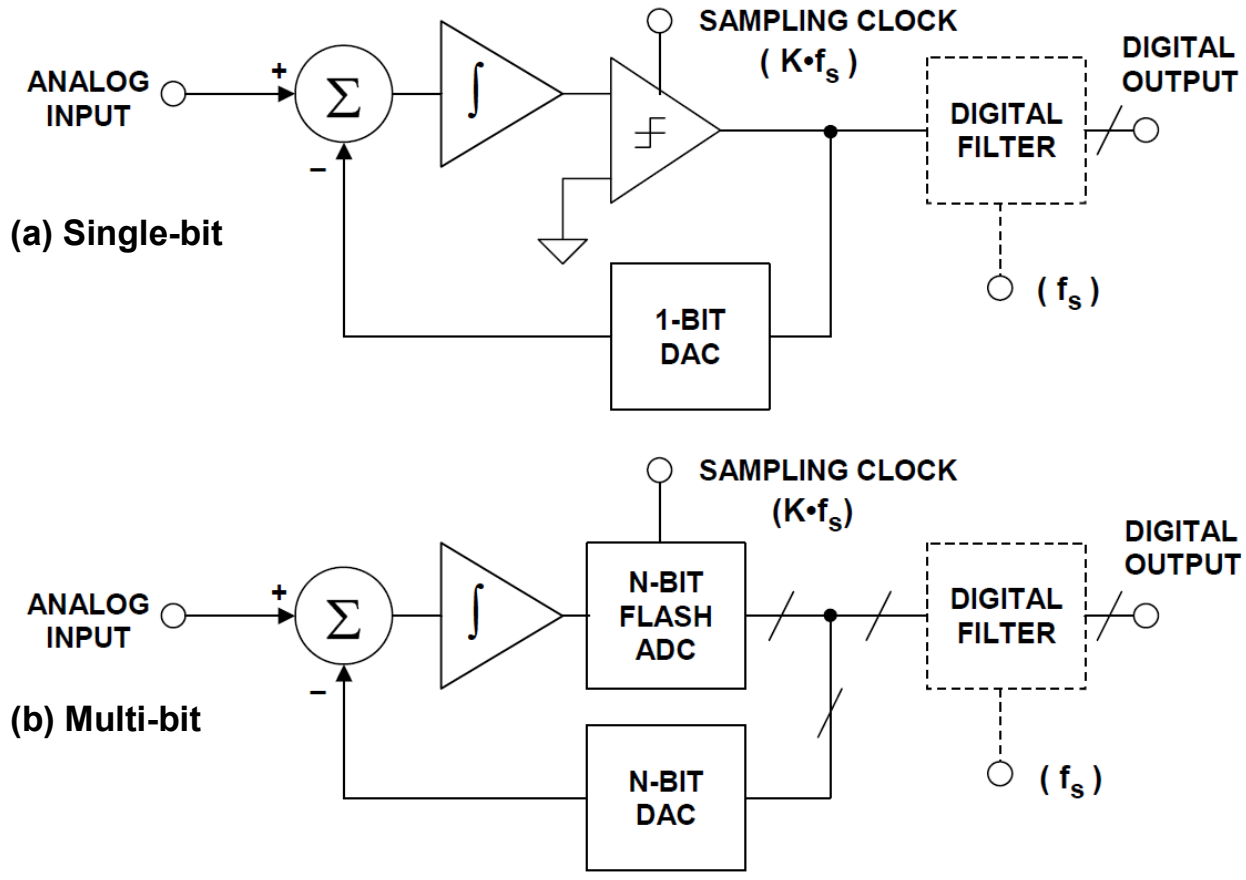


Figure 1.6 Single and Multi-bit Sigma-Delta ADC.

Each of the ADC architectures has its merit and demerit since there always exist tradeoffs between conversion speed, resolution, power consumption, size, static performance, dynamic performance and cost. Depending on applications, some performance features may be more significant than others. For example, precision sensor conditioning requires high-resolution high-accuracy and low-cost ADCs, but speed and power requirements can be quite loose. Serial link communication system requires very high sampling rate but resolution and power consumption are not first concerns. Figure 1.7 shows a number of applications which have different requirements of ADC sampling rate and resolution.

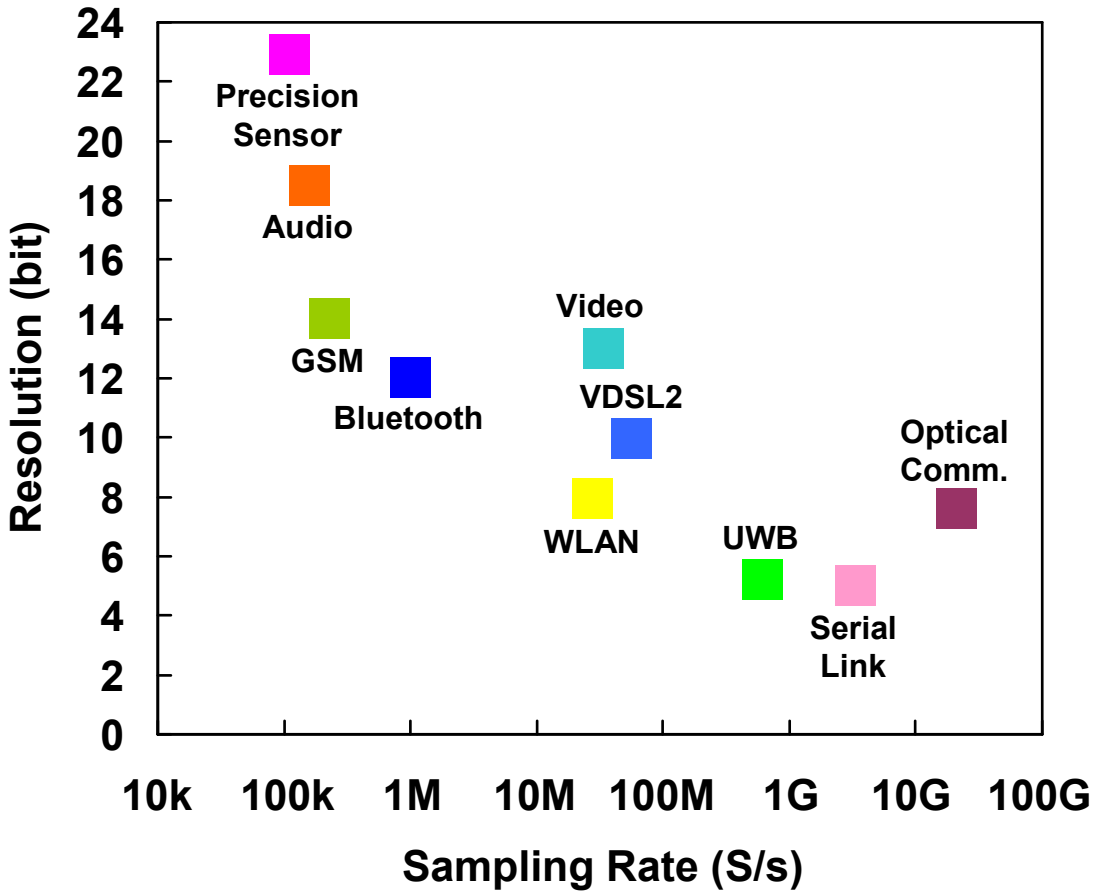


Figure 1.7 ADC Applications.

Figure 1.8 shows each ADC architecture's dominating area in terms of sampling rate and resolution. Sigma-delta ADCs are used predominantly in low speed applications, trading speed for resolution by oversampling. Successive-approximation-register (SAR) ADCs are frequently the architecture of choice for medium-to-high-resolution applications, typically with low-to-medium sampling rates. Pipelined ADC has become the most popular ADC architecture for sampling rates from a few MS/s up to a hundred MS/s, with medium-to-high resolutions. Subranging architecture is a cross between the pipelined and flash architectures. Flash ADCs are suitable for applications requiring very large bandwidths yet low resolutions. Time interleaving (TI) architecture is used to combine with other architectures to multiply the sampling rate.

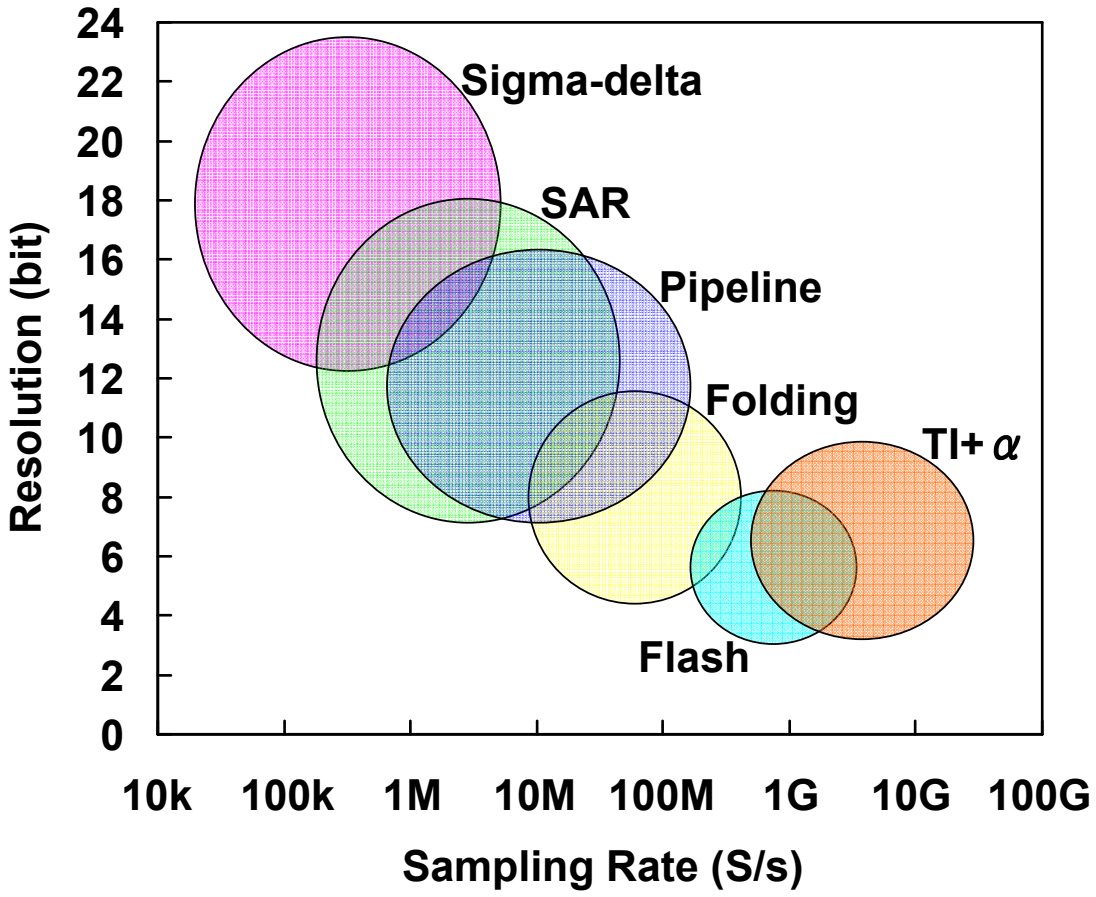


Figure 1.8 ADC Architectures Domain Area.

1.2 Research Motivation

Despite the variety of ADC architectures utilized in diverse applications, their performances are usually summarized by a relatively small number of parameters: stated resolution, signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), effective number of bits (ENOB), sampling rate, and power consumption. In 1999, Walden's survey of more than 150 converters concluded ADC performance limitations [27]. For low speed ADCs, resolution appears to be limited by thermal noise. For medium-to-high speed ADCs, approximately one bit of resolution is lost for every doubling of the sampling rate. For very high speed ADCs, the speed of device technology is a limiting factor due to comparator ambiguity. In the survey paper, an ADC figure of merit (FOM) was firstly defined as $2^{ENOB} \times f_{sampling} / Power$. A modified version of the Walden FOM has been more widely accepted, which is shown as follows.

$$FOM = \frac{Power}{2^{ENOB} \times f_{sampling}} \tag{1.1}$$

Figure 1.9 plots the experimental ADCs which have been presented in the world's top two solid-state-circuit conferences in the past decade [28]. Many ADC architectures and integrated circuit technologies have been proposed and implemented to push back performance limits. Although different metrics and interpretations of ADC performances may be used in different research work, an overall trend is not affected in a significant way. The trend that cuts across nearly all resolutions and sampling rates is "low power". The average FOM becomes smaller and smaller, indicating lower energy consumed in each effective conversion step. In this work a 9-bit 100-MS/s ADC has been designed and implemented with power consumption of only 1.46 mW, resulting in an FOM of 39 fJ/conv-step, which is one of the best-performing converters in the world.

This work targets battery-powered data communication and imaging processing systems. ADCs with medium resolution (8-bit to 10-bit) and moderate sampling rate (several tens to hundred of MHz) are required for applications such as one-segment digital TV receiver in cell phones, high definition camcorders, and etc. Today's portable consumer electronics devices require designs of professional-quality sound, display and high definition video with lower power consumption, smaller area, more functions and lower cost. Therefore,

energy efficient and area efficient ADCs with high performance are in great demand.

Pipelined and SAR architectures are most commonly selected for in the range of moderate resolution and speed. As introduced in the previous section, pipelined ADCs rely on inter-stage amplifiers, which are usually operational amplifiers (op-amp), to accurately amplify the residue signal in each stage. However, with technology scaling, low power design of pipelined ADC with op-amps has become more challenging, because the achievable gain per stage is limited by transistor short-channel effects and reduction of power supply voltage. On the other hand, in SAR architecture, only one single comparator decides the digital outputs bit by bit. Since the only active analog component is the comparator, which does not need to be linear, the major power consumption is in the digital circuits. Digital power and speed benefit from the technology scaling, making SAR architecture a power-efficient selection. However, a problem with SAR architecture is that they usually cannot deliver the best possible performance when considering about absolute speed, resolution and input capacitance simultaneously. The hundreds of ADCs in Figure 1.9 are filtered by selecting the pipelined and SAR architectures with moderate speed and resolution and re-plotted in Figure 1.10. As shown in Figure 1.10(a), the SAR ADCs have achieved much higher energy efficiency than the pipelined ones, but they all operate at sampling rates lower than 50MS/s. On the other hand, the pipelined architecture is able to achieve sampling rates higher than 100MS/s. This work has focused attention on SAR architecture and proposed several techniques to improve the speed while keeping high energy efficiency. This work has also made efforts to minimize the ADC area to meet the requirements of portable electronic devices, as shown in Figure 1.10(b).

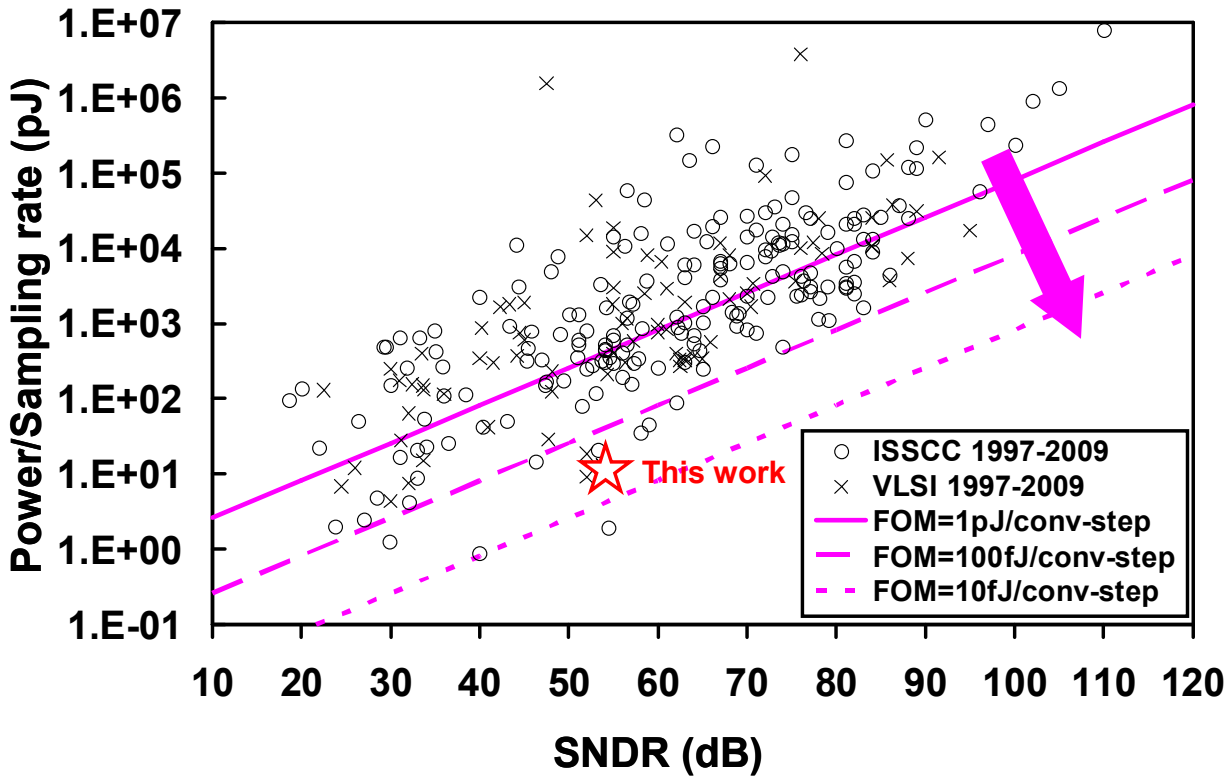


Figure 1.9 Trend of ADC Performance in the Past Decade.

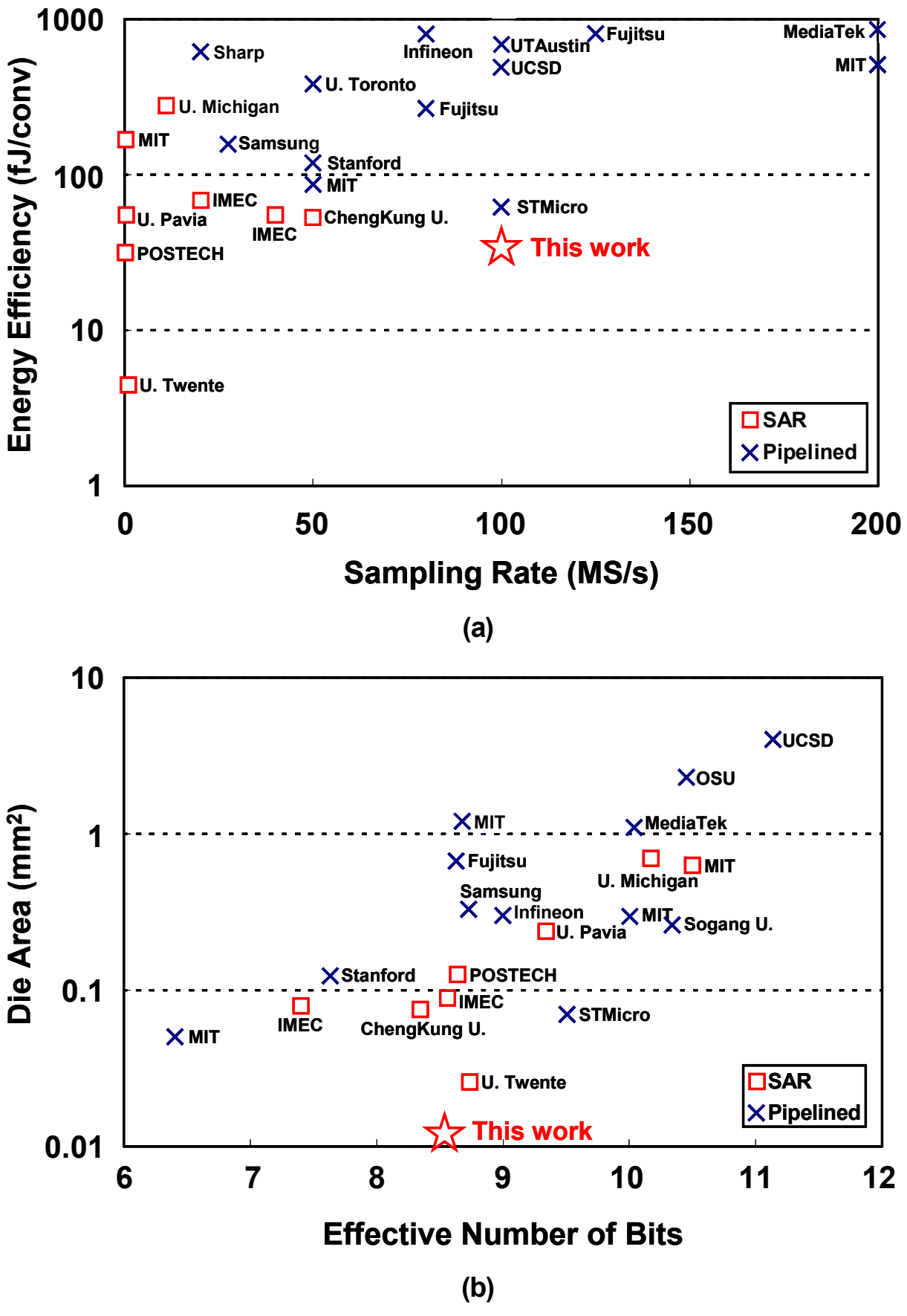


Figure 1.10 Target ADC Performance (a) Energy Efficiency vs. Sampling Rate (b) Die Area vs. ENOB.

1.3 Dissertation Organization

This thesis is organized as shown in Figure 1.11.

Chapter 1 is an introduction of the study, which includes the data converter background, research motivation and dissertation organization.

Chapter 2 presents a split capacitive DAC calibration scheme, which can be used to reduce area and input load capacitance while keeping good linearity performance. The issues of conventional split CDACs are analyzed, followed by the principle and implementation of the proposed calibration method. The feasibility is proved by the test chip measurement results.

Chapter 3 presents the tri-level charge redistribution scheme. The switching energy inefficiency and settling problem of the conventional method are first analyzed. Then the tri-level method and differential capacitor bottom-plate charge-sharing technique are introduced in details. The improvement of energy efficiency and settling speed are shown in simulation results.

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Chapter 5 summarizes the thesis and provides a prospect of future work.

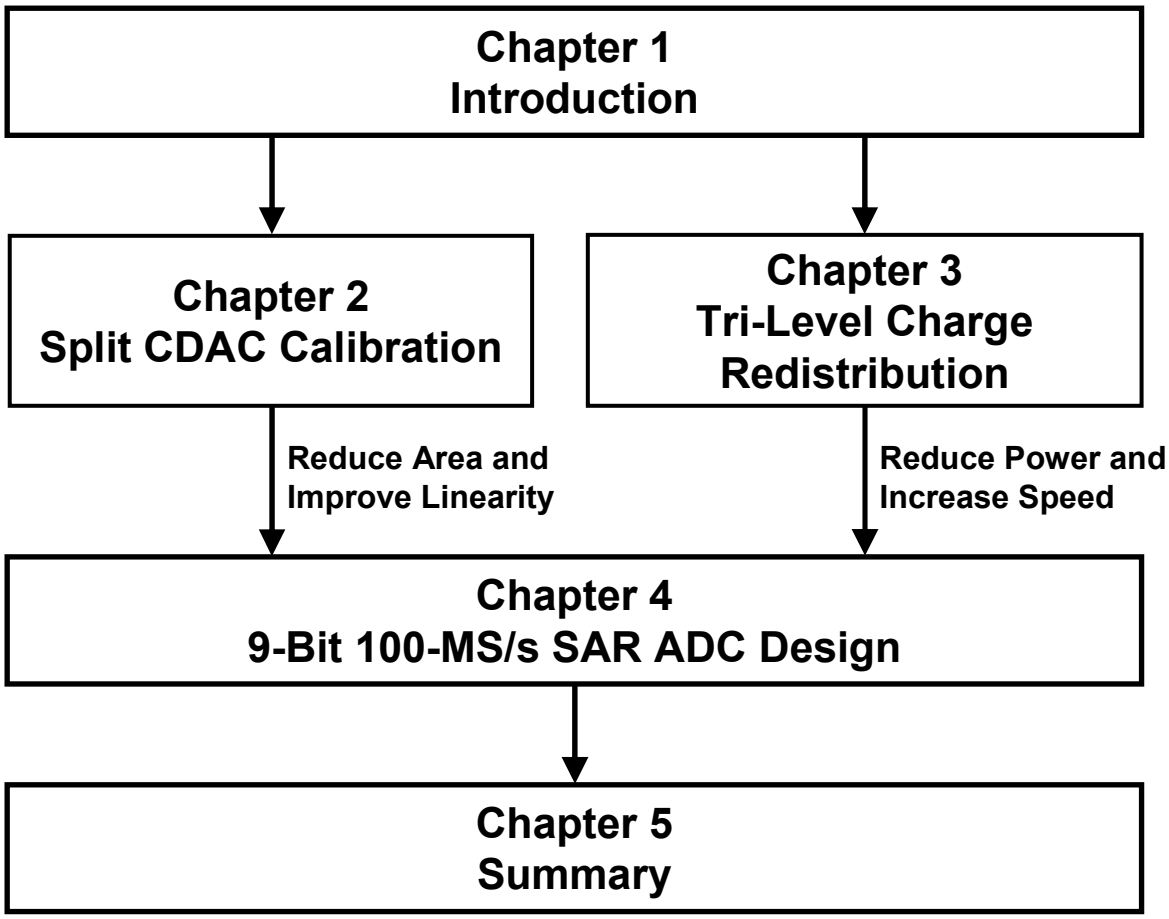

Figure 1.11 Dissertation Organization.

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Chapter 2 Split Capacitor DAC Calibration

2.1 Charge Redistribution SAR ADC

Successive approximation ADC has a simple structure, low power consumption and reasonably fast conversion rate. The overall accuracy and linearity of the successive approximation ADC is determined primarily by the internal DAC. Until recently, most precision SAR ADCs used laser-trimmed thin-film resistor DAC to achieve the desired accuracy and linearity [1]. The thin-film resistor trimming process makes the chip larger and more expensive, and the thin-film resistor values may be affected when subjected to the mechanical stresses of packaging. The development of sub-micron CMOS process has made possible very small, cheap and accurate switched-capacitor (or charge redistribution) DACs, which have become popular in successive approximation ADCs [2-5]. The advantage of the charge redistribution DAC is that the accuracy and linearity is mainly determined by high-accuracy photolithography, which in turn controls the capacitor plate area and the capacitance as well as matching. In addition, small capacitors can be placed in parallel with the main capacitors which can be switched in and out under control of auto-calibration routines to achieve high accuracy and linearity without the need for thin-film laser trimming. The use of capacitive charge redistribution DAC offers another advantage as well. The DAC itself serves as a sample-and-hold (SHA) circuit, and therefore neither an external SHA nor allocation of chip area for a separate internal SHA is required.

An *N*-bit charge redistribution SAR ADC is shown in Figure 2.1. The switches are shown in the sampling mode where the analog input voltage V_{IN} is constantly charging and discharging the parallel combination of all the capacitors. The conversion mode is initiated by opening switch S_C, storing the voltage $V_{BIAS}-V_{IN}$ on the capacitor array. The voltage at node P is allowed to move as the bit switches are manipulated. Then the MSB capacitor is connected to V_{REF} while the rest capacitors are connected to ground, causing the node P to settle to

$$V_P = V_{BIAS} - V_{IN} + \frac{V_{REF}}{2} \tag{2.1}$$

The comparator then makes the decision of the MSB, and the SAR logic leaves the MSB capacitor connected

to V_{REF} or connects it to ground depending on the comparator output, which is low or high depending on whether the voltage at node P is negative or positive.

$$MSB = \begin{cases} 1 & V_{IN} > \dfrac{V_{REF}}{2} \\ 0 & V_{IN} < \dfrac{V_{REF}}{2} \end{cases} \tag{2.2}$$

A similar process is followed for the remaining two bits. At the end of the conversion interval, all the capacitors are connected to V_{IN}, S_C is connected to ground, and the converter is ready for another cycle.

The extra LSB capacitor (dummy capacitor) as shown in Figure 2.1 is required to make to total value of the capacitor array equal to $2^N \cdot C$ in the case of the *N*-bit DAC so that the binary division is accomplished when the individual bit capacitors are manipulated.

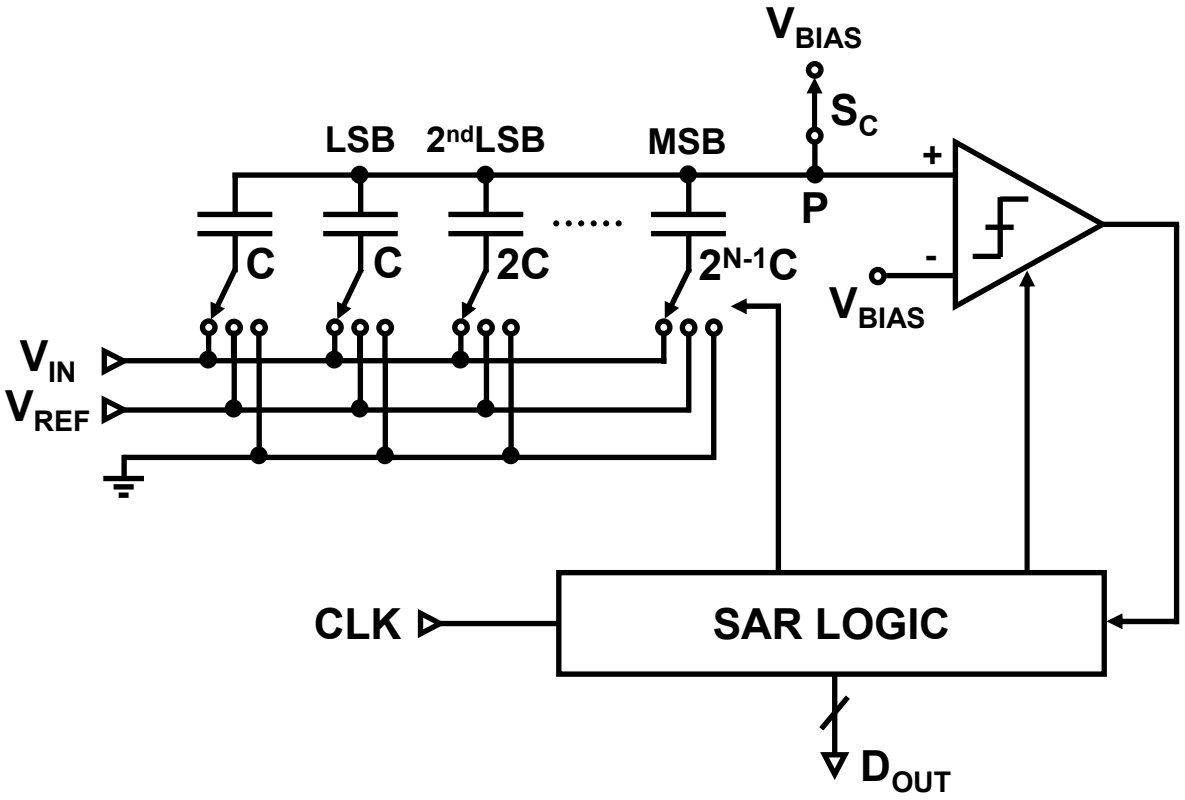


Figure 2.1 Charge Redistribution SAR ADC.

2.2 Split Capacitor DAC

Charge redistribution SAR ADC has an inherent sample-and-hold function. However, the input load capacitance and area of a binary-weighted capacitor DAC (CDAC) increase exponentially with the number of bits. Split capacitor arrays have been proposed as solutions to reduce both input capacitance and area [6-9]. Figure 2.2 shows an 8-bit example. Figure 2.2(a) is a binary-weighted CDAC, where C represents the unit capacitance. The total input capacitance is equal to $256C$ and the total area is 256 times the unit capacitor area. The asymmetric symbol of capacitors indicates that top and bottom capacitor plates have different parasitic capacitance. Generally speaking, it is preferable to connect the capacitor plate with smaller parasitic capacitance to the comparator input.

In Figure 2.2(b), a bridge capacitor is implemented to connect two split capacitor arrays which have the same scaling. The left array is the lower weight side (LSB-side) and the right array is the higher weight side (MSB-side). The bridge capacitor has a fractional value equal to $(16/15)C$ which is determined by the resolution of the LSB-side capacitor array [6]. In the charge-redistribution process, the total weight of the LSB-side capacitor array is ideally equal to the weight of the lowest bit in the MSB-side capacitor array. Note that the dummy capacitor C is only implemented in the L-side array. During the sampling mode, all the capacitors in the LSB-side and MSB-side arrays are connected to the analog input signal V_{IN}, and both switches S_{C1} and S_{C2} are connected to an ac ground (a dc bias voltage determined by the comparator input common mode voltage). The total input load capacitance is equal to $31C$, which is about 8 times smaller than the binary-weighted capacitor array. The area reduction is also 8 times. However, the bridge capacitor being fractional causes poor matching with the other capacitors. Parasitic capacitance at node Q affects the charge coupling ratio of the LSB-side array and the bridge capacitor. Both above problems degrade the DAC linearity and thus the overall ADC linearity performance.

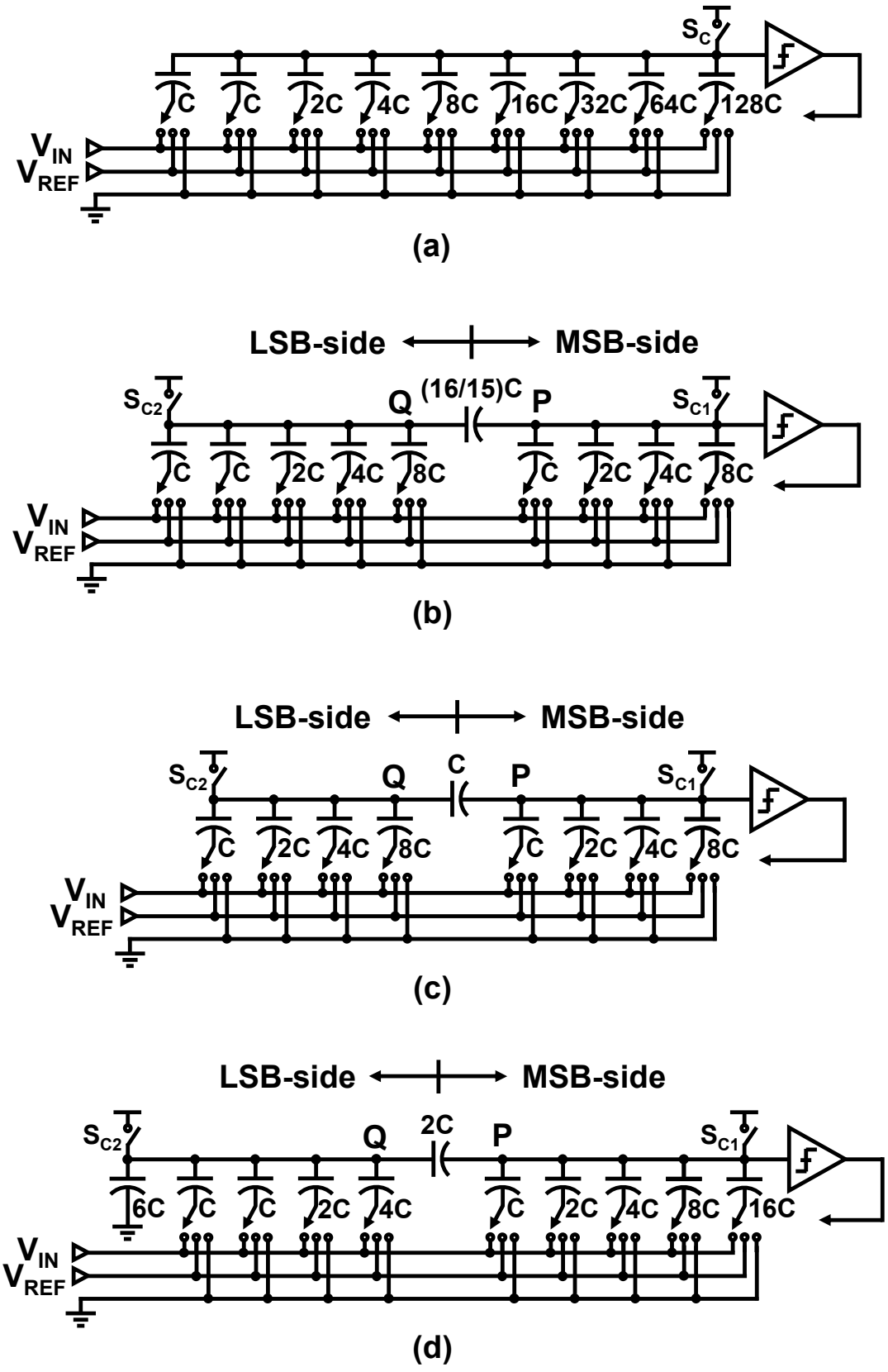
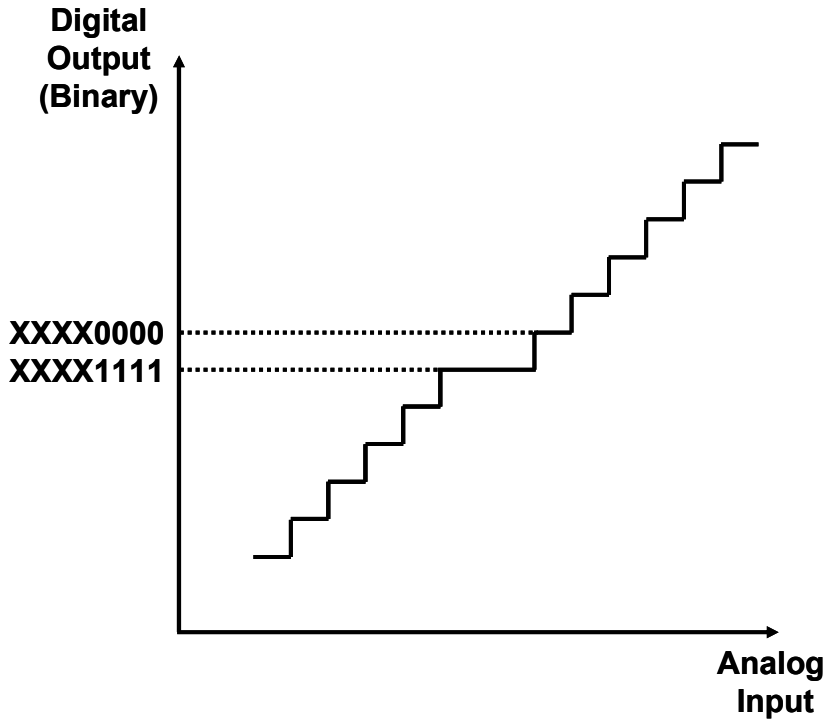


Figure 2.2 8-Bit CDACs (a) Binary-Weighted Array (b) Split Array with Fractional Bridge Capacitor (c) Split Array with Unit Bridge Capacitor (d) Split Array with Two Unit Bridge Capacitor.

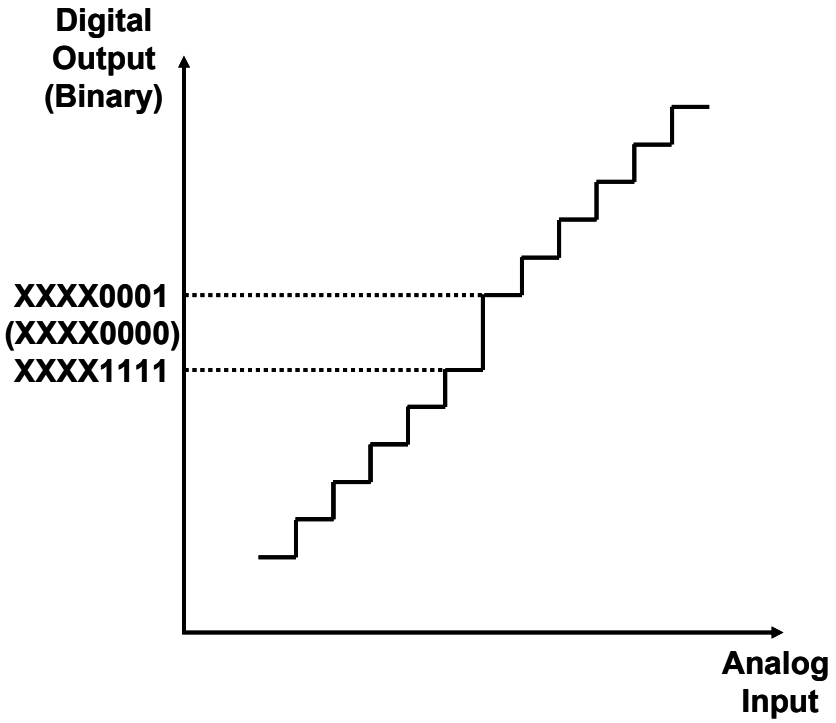
The fractional-value bridge capacitor is replaced with a unit capacitor in Figure 2.2(c). The dummy capacitor is removed from the LSB-side array so that the total weight of the LSB-side array keeps the same as the lowest bit in the MSB-side array. However, due to the lack of the dummy capacitor, 1LSB gain error occurs [7].

In Figure 2.2(d), a bridge capacitor equal to 2C is implemented [8]. A compensation capacitor having fixed capacitance of 6C is added to the 3-bit LSB-side array. However, with the increase of the LSB-side array resolution, the bridge capacitor being 2C leads to larger compensation capacitor. For a 4-bit LSB-side array, the compensation capacitor needs to be 14C. The CDACs in Figure 2.2(c) and Figure 2.2(d) eliminate the mismatch caused by the fractional value bridge capacitor. However, they are still vulnerable to the parasitic capacitance in node Q and between nodes Q and P, which leads to mismatches between the LSB-side and MSB-side capacitor arrays. Since parasitic capacitance is sensitive to process options, such as the number of metal layers, which varies according to system-on-chip (SoC) applications, the split CDAC linearity performance cannot be well controlled. In [9] an extra CDAC is implemented for calibrating the main CDAC linearity, however all control logic circuits are realized by using an off-chip FPGA rather than on-chip implementation.

Figure 2.3 displays part of the output code transitions in the case that mismatches exist between the LSB-side and the MSB-side capacitor arrays in the split CDAC based SAR ADCs. Mismatches between each unit capacitors are ignored here. The same nonlinearity repeats every 16 output codes because of the 4-bit resolution of the LSB-side capacitor array. Figure 2.3(a) indicates that the total weight of the LSB-side capacitors is smaller than the lowest-weight capacitor in the MSB-side array while Figure 2.3(b) shows the opposite situation. The LSB-side capacitors have 1LSB larger weight than the lowest-weight capacitor in the MSB-side array, resulting in one output missing code. Figure 2.4 depicts the ADC gain error in terms of the code transition.



(a)



(b)

Figure 2.3 ADC Code Transitions with Nonlinearity.

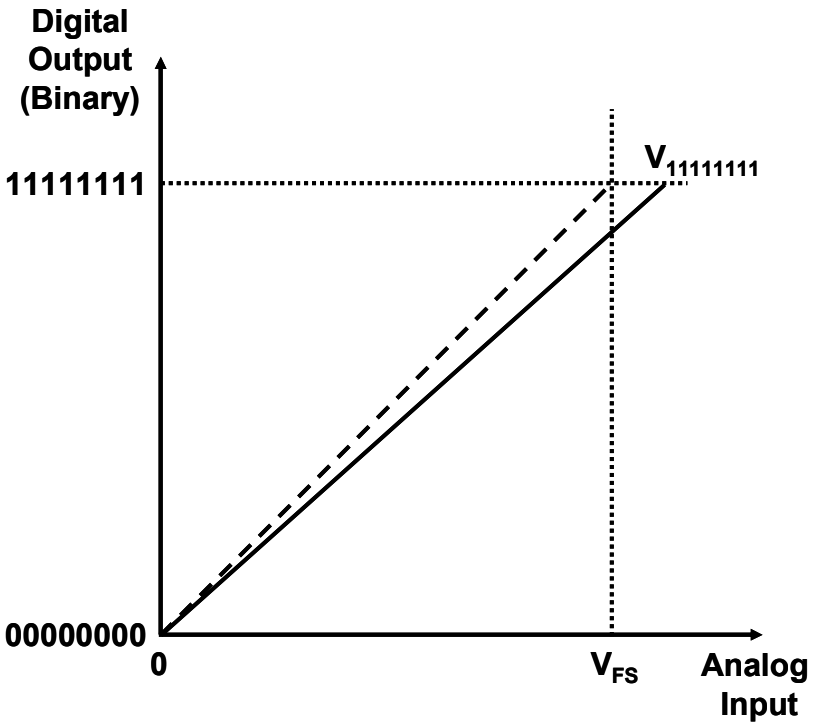


Figure 2.4 ADC Code Transition with Gain Error.

2.3 Split CDAC Calibration

This work proposes an on-chip calibration scheme to improve the split CDAC linearity performance and avoid the gain error as well [10]. As shown in Figure 2.5, C_{P1} and C_{P2} stand for the parasitic capacitance in node *Q* and between nodes *P* and *Q*. They are separated from the CDAC array, and thus all capacitors can be considered to be ideal (shown in symmetric capacitor symbol). The bridge capacitor C_B is designed to be slightly larger than the ideal fractional value (16/15)*C* and a tunable calibration capacitor C_C is introduced in parallel with the LSB-side capacitor array to compensate for mismatches caused by either the fractional value bridge capacitor or parasitic capacitance. An extra unit capacitor is added to the MSB-side array to further reduce the input load capacitance to 16*C*. To guarantee appropriate operation of the CDAC calibration, the comparator offset is cancelled by using a digital timing-control charge compensation method before the CDAC calibration.

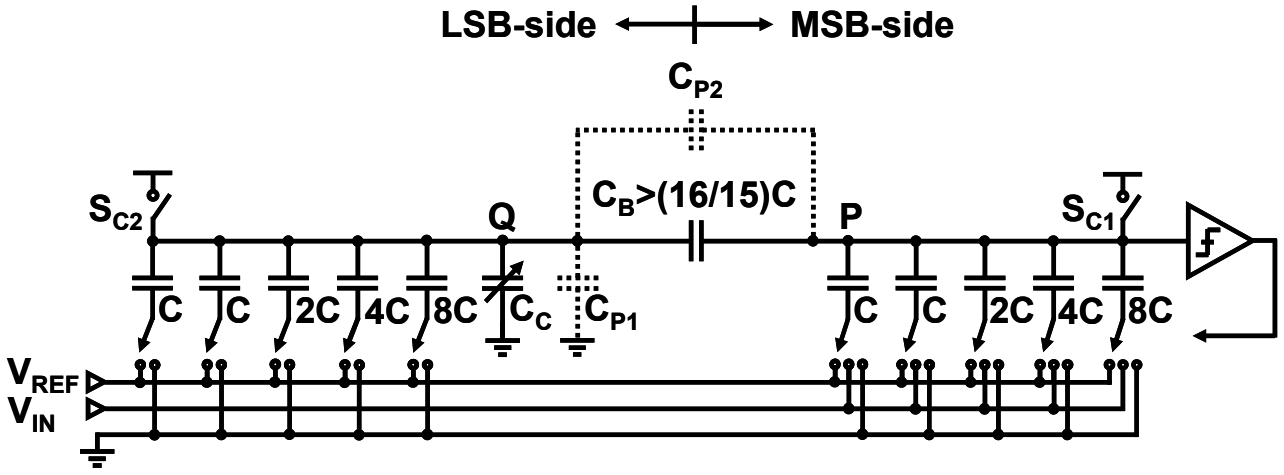


Figure 2.5 Split Capacitor Array with Mismatch Calibration.

2.3.1 Principle

The CDAC mismatch calibration is to adjust the total weight of the LSB-side capacitor array until it is equal to that of the lowest bit capacitor in the MSB-side array even if there exist fractional value capacitance variation of C_B and parasitic capacitance C_{P1} and C_{P2}. The effective weight of the LSB-side array can be calculated using the equivalent circuits shown in Figure 2.6. Node P is the CDAC output and connected to the comparator input. It is biased to the comparator input common-mode voltage V_{CM} during the sampling phase and returns to V_{CM} in the end of conversion phase. Therefore, node P can be considered a virtual ground, which means the parasitic capacitance in node P doesn't affect the charge redistribution. Suppose the bottom plates of all LSB-side capacitors are connected to a certain voltage V_X, according to voltage division principle, V_Q (the voltage at node Q) can be calculated as follows.

$$V_Q = \frac{16C}{16C + C_C + C_{P1} + C_B + C_{P2}} \cdot V_X \tag{2.3}$$

Then the charge contributed to node *P* can be calculated.

$$Q = (C_B + C_{P2}) \cdot V_Q = \frac{(C_B + C_{P2}) \cdot 16C}{16C + C_C + C_{P1} + C_B + C_{P2}} \cdot V_X \tag{2.4}$$

Therefore, the contribution of the total L-side array to node P is equivalent to a capacitor with capacitance C_{EF}, which is directly connected to node P.

$$C_{EF} = \frac{(C_B + C_{P2}) \cdot 16C}{16C + C_C + C_{P1} + C_B + C_{P2}} \tag{2.5}$$

The compensation capacitor C_C can be adjusted until C_{EF} is equal to the unit capacitor C and the L-side capacitor array has the correct weight in the charge redistribution. The required capacitance of C_C can be easily calculated as follows.

$$C_C = 15(C_B + C_{P2}) - 16C - C_{P1} \tag{2.6}$$

For a more general case, the L-side array is a *k*-bit binary-weighted capacitor array. The equivalent capacitance to node P can be calculated as follows.

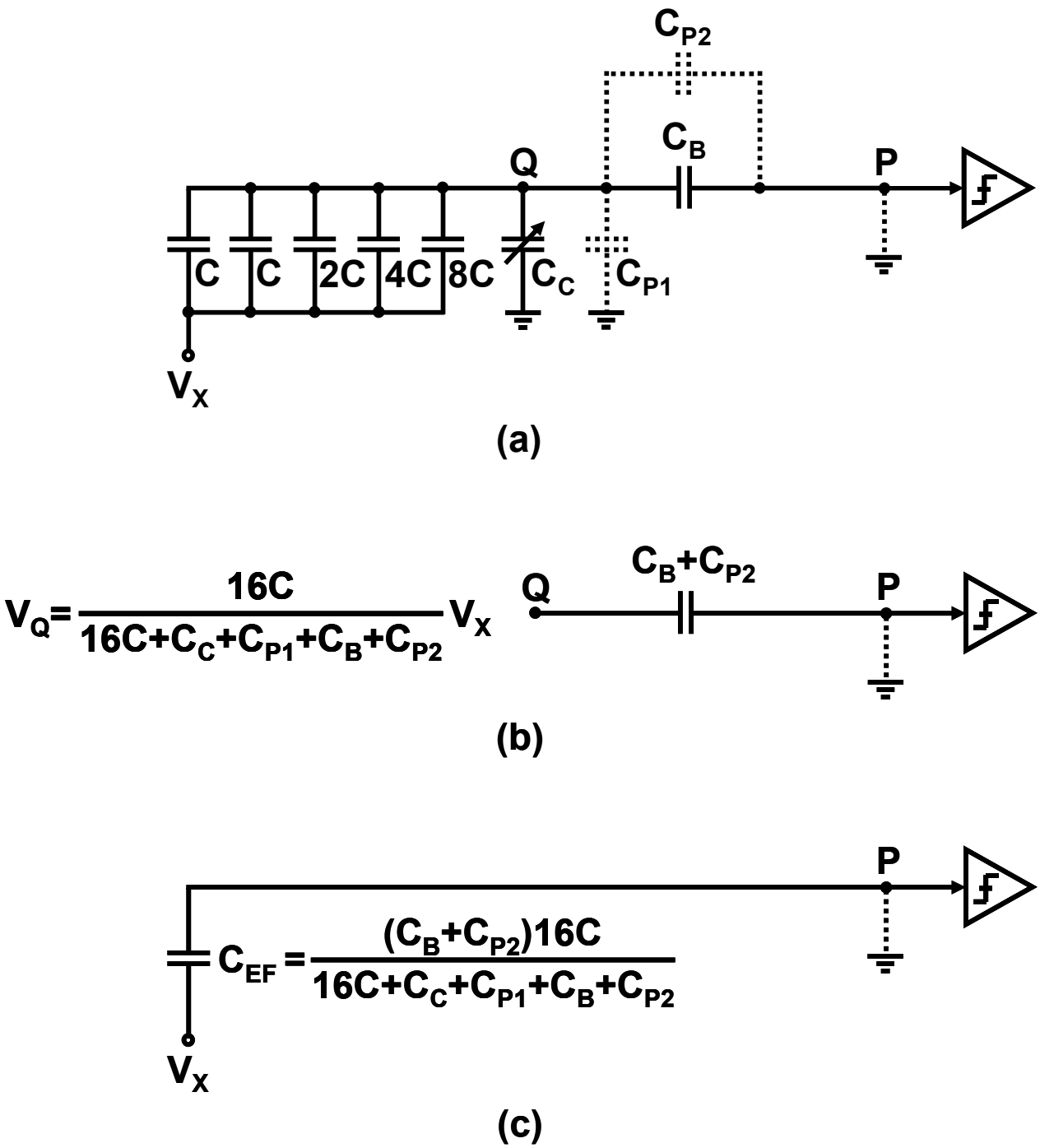


Figure 2.6 Equivalent Circuits of the L-side Capacitor Array.

$$C_{EF} = \frac{(C_B + C_{P2}) \cdot 2^k C}{2^k C + C_C + C_{P1} + C_B + C_{P2}} \tag{2.7}$$

The required capacitance of C_C for the L-side array to achieve the correct weight is as follows.

$$C_C = (2^k - 1) \cdot (C_B + C_{P2}) - 2^k \cdot C - C_{P1} \tag{2.8}$$

In the proposed calibration scheme, both the fractional value bridge capacitor mismatch and the parasitic capacitance effects to linearity performance can be well controlled.

2.3.2 Implementation

A. CDAC

The split CDAC calibration implementation with a timing diagram is shown in Figure 2.7. Single-ended circuit is shown for simplicity while fully differential circuit is actually implemented for good common-mode noise rejection and low distortion.

During calibration period, all MSB-side capacitors except for one lowest bit are connected to ground. When ϕS="1", both nodes P and Q are biased to common mode voltage V_{CM}. The lowest bit of the MSB-side array is set to "0" and the LSB-side array is set to "11111". When ϕS="0", nodes P and Q become floating. Then the lowest bit of the MSB-side array is set to "1" and the LSB-side array is set to "00000". The compensation capacitor C_C is initially set to the smallest value in its tunable range and therefore the total weight of the LSB-side array is initially larger than the lowest bit of the MSB-side array. Since the charge in node P has to keep constant during ϕS="0", V_P (the voltage at node P) becomes smaller than V_{CM}. The comparator compares V_P and V_{CM} and feeds back its output to control logic to increase C_C so that the weight of the LSB-side array becomes smaller. The process repeats until V_P is equal to V_{CM} and the comparator output changes. The LSB-side array has the same weight as the lowest bit of the MSB-side array and the calibration is finished.

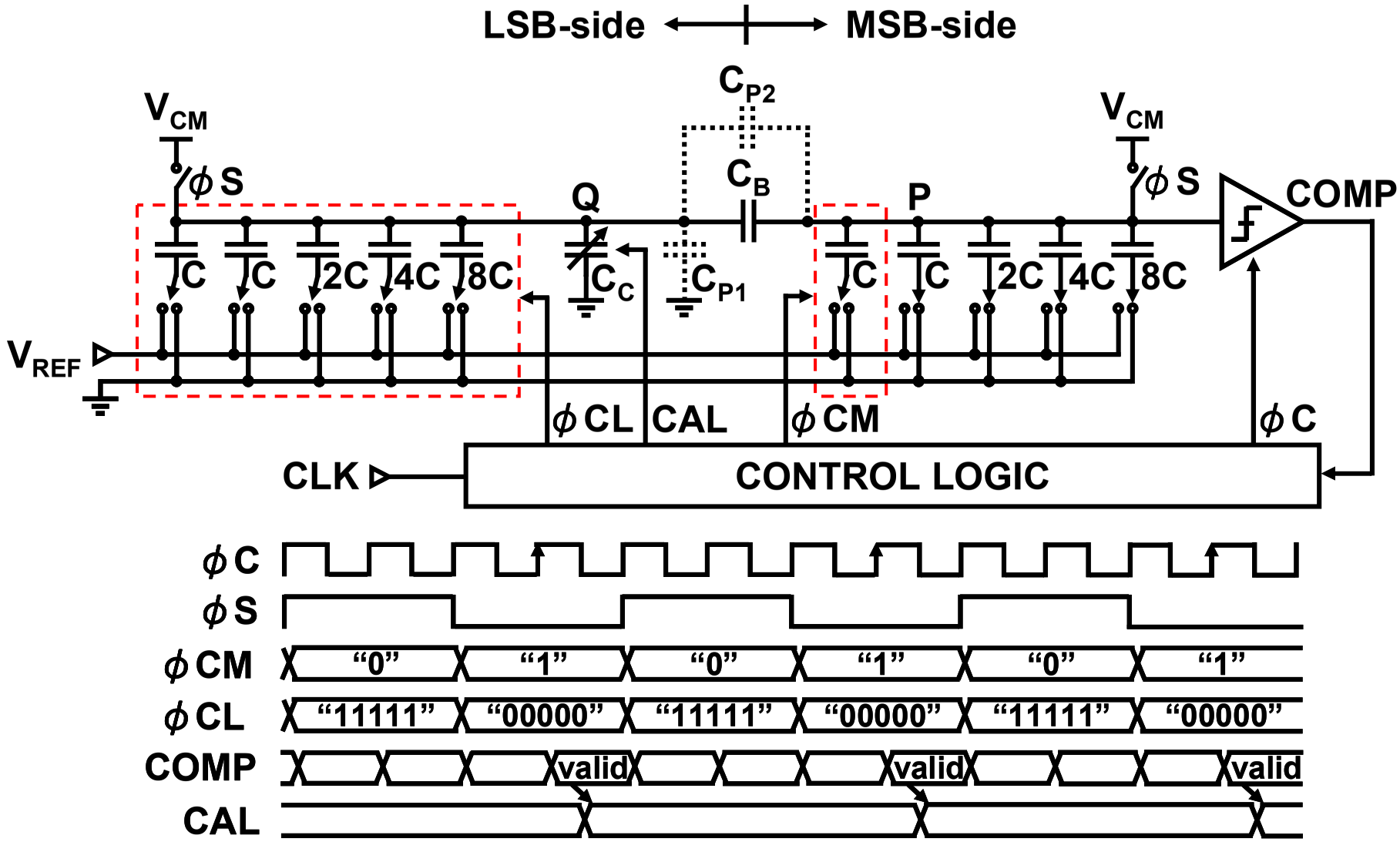


Figure 2.7 Split CDAC Calibration Implementation with Timing Diagram

For the 4-bit + 4-bit split CDAC implementation, if the bridge capacitor C_B is ideally equal to (16/15)C and there is no parasitic capacitance, C_C being zero satisfies Equation (2.6). Since the parasitic capacitance varies with process options, it is desirable to adjust C_C in a wide enough range. Therefore in this work C_B is designed to be 1.4C. The adjustment range of C_C is 8C and the minimum step is 0.5C. Dummy capacitors around the core CDAC array have been implemented for symmetry. Making use of these dummy capacitors, no extra area is required to implement C_C. As shown in Figure 2.8, two unit capacitors are connected in series to achieve 0.5C-step control. When the upper switch turns on, the capacitance is C. When the upper switch turns off and the lower switch turns on, the capacitance becomes 0.5C. When both switches are turned off, the capacitance becomes zero. Totally 8 groups of the series capacitors are connected in parallel, working as C_C. Thermometer control is implemented for simplicity.

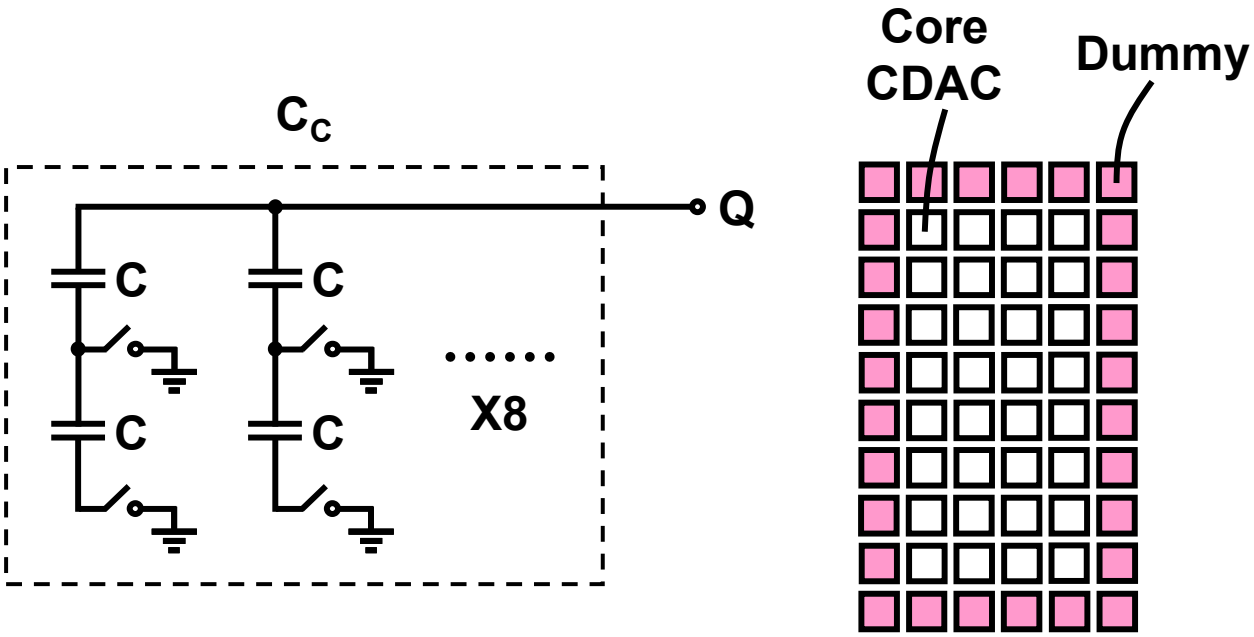


Figure 2.8 Implementation of C_C.

Correct CDAC calibration requires the comparator offset to be small enough, because the offset would affect the weight comparison between the LSB-side and MSB-side arrays. Therefore, before the CDAC calibration starts, node P is biased to V_{CM} and the comparator offset calibration is performed. This will be discussed in detail in the next sub-section.

Since the capacitor mismatches are due to process variation, the calibration is performed in foreground. After the calibration, the normal ADC function starts. During sampling phase, both nodes P and Q are biased to V_{CM}. In conventional split CDAC designs, Figure 2.2 (b) and (c), both MSB-side and LSB-side arrays sample the input signal, and therefore the input capacitor load is $31C$ and $30C$, respectively. In the proposed scheme, Figure 2.5, an extra unit capacitor is added to the MSB-side array. Only the MSB-side array is used to sample the input. The LSB-side is grounded during sampling phase. During conversion phase, the extra unit capacitor is grounded while the remaining capacitors are connected to either ground or V_{REF} depending on their respective data bits. Thus, the input load capacitance is reduced to $16C$, which is half of the conventional split CDAC.

In this work, capacitor mismatches inside the MSB-side array and the LSB-side array are ignored. The unit capacitor is set to be 11fF to meet matching requirements for less than 10-bit resolution. According to parameters provided by semiconductor manufacturing foundry, the relative deviation between two unit capacitors is 0.3% while the absolute capacitance deviation is as large as 15%. Each unit capacitor has the same parasitic capacitance. Therefore inside the MSB-side array and the LSB-side array, capacitance ratio between capacitors does not change due to the parasitic capacitance. In charge redistribution, what affects the linearity performance is the ratio between capacitors rather than the absolute capacitance. In a high resolution ADC of more than 10-bit, unit capacitor should be sized larger to meet both kT/C noise and matching requirements. More than two sub-array split CDAC can be implemented to reduce total input load capacitance and area. The proposed calibration technique can be used to remove mismatches between each two sub-arrays.

B. Comparator

A comparator with small enough offset is required to guarantee correct CDAC calibration. An offset reduction technique is preferred to be used in the comparator to avoid using large-size transistors, which leads to high power dissipation [11-13]. Among recent comparator offset calibration techniques, an approach applying a static correction with current sources to compensate for offset causes static power dissipation [14]. Another approach implementing a dynamic offset control with capacitors to adjust output capacitive loads results in degradation of response speed [15]. This comparator employs a dynamic offset correction with timing control charge compensation based on [16]. It has been improved by implementing a two-step digital control method.

Figure 2.9 shows the dynamic comparator schematic, based on [17]. A differential input pair feeds currents into a cross-coupled CMOS regenerative pair. A reset switch *M*1 helps recovering from overdrive as well as allowing offset calibration. Two sets of PMOS transistors, *MC*1 and *MC*2, with source-drain connected are implemented in nodes *N*1 and *N*2, respectively. Both *MC*1 and *MC*2 consist of coarse and fine calibration transistors *MCC* and *MCF*. *MCC* is controlled by a tunable timing clock *OCC*, while *MCF* is controlled by a fixed timing clock *OCF*.

During the reset phase, two output nodes are pulled up to the supply voltage. Nodes *N*1 and *N*2 are connected through *M*1. Both *MC*1 and *MC*2 are turned on to save charges in the channels. When the regeneration phase starts, *M*1 is turned off by signal *CLK* and *MCC* on one side is turned off by *OCC* after a delay *td*. Charges in the channel of *MCC* are injected to node *N*1 or *N*2 to generate a compensation voltage. The compensation voltage is a fixed value V_C, which is determined by the transistor size of *MCC* and the parasitic capacitance in node *N*1 or *N*2. The input-referred offset V_{OS} is amplified by the regenerative pair during the delay period *td*. The longer the delay is, the larger the voltage gain becomes, and therefore the smaller input-referred offset can be compensated. The delay time *td* is controlled by adjusting transistor sizes in an inverter delay line. The relationship between V_{OS} and *td* can be calculated as follows.

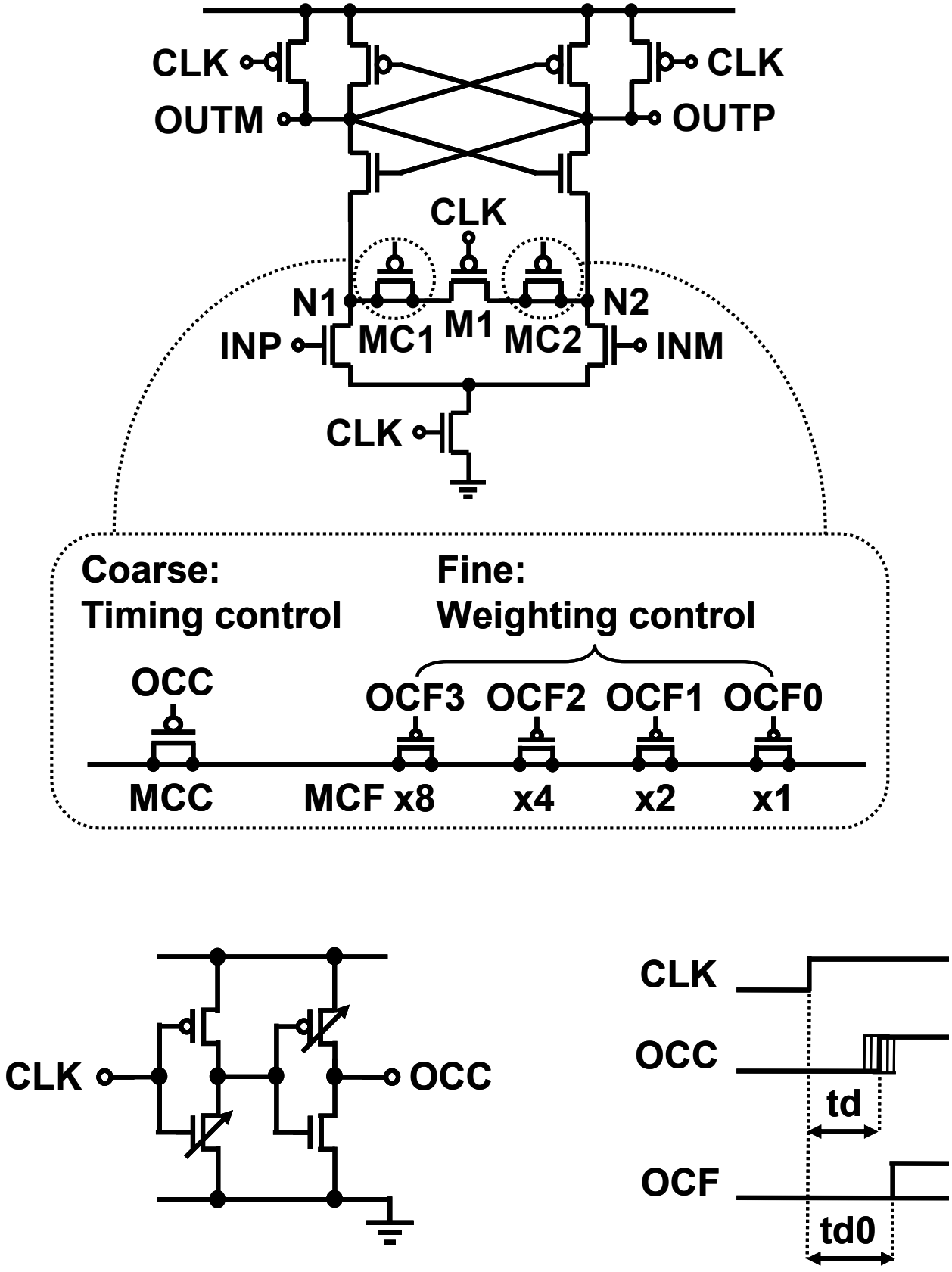


Figure 2.9 Comparator with Two-Step Digital Timing Control Charge Compensation Offset Calibration.

$$V_{OS} = \frac{1}{A} \cdot \exp(\frac{-td}{\tau}) \cdot V_C \tag{2.9}$$

where A is the voltage gain and τ is the regenerative time constant of the comparator. Figure 2.10 shows a simulation result of the relationship between the offset and delay time. Since it is difficult to precisely control the delay time in the inverter line, unlike the implementation in [16] that applies delay control to both *MC*1 and *MC*2, this comparator applies delay control only to one of them at a time. The coarse calibration covers an offset range of 40mV in 10mV steps.

Fine calibration is performed by a 4-bit array of smaller-size transistor *MCF* applied with a fixed timing clock *OCF*. *MCF* works in a similar way to *MCC*, injecting charges to node *N*1 or *N*2 a delay after *M*1 is turned off. The difference is that the delay period *td*0 is fixed. The compensation voltage generated by the *MCF* array is determined by the number of *MCF* that is chosen to operate. The fine calibration manages to control offset in 1mV steps according to the simulation result. The comparator offset calibration needs 20 clock cycles at most, 4 for the coarse calibration and 16 for the fine calibration. Once the comparator offset calibration is finished, a ready signal is generated to start the CDAC mismatch calibration.

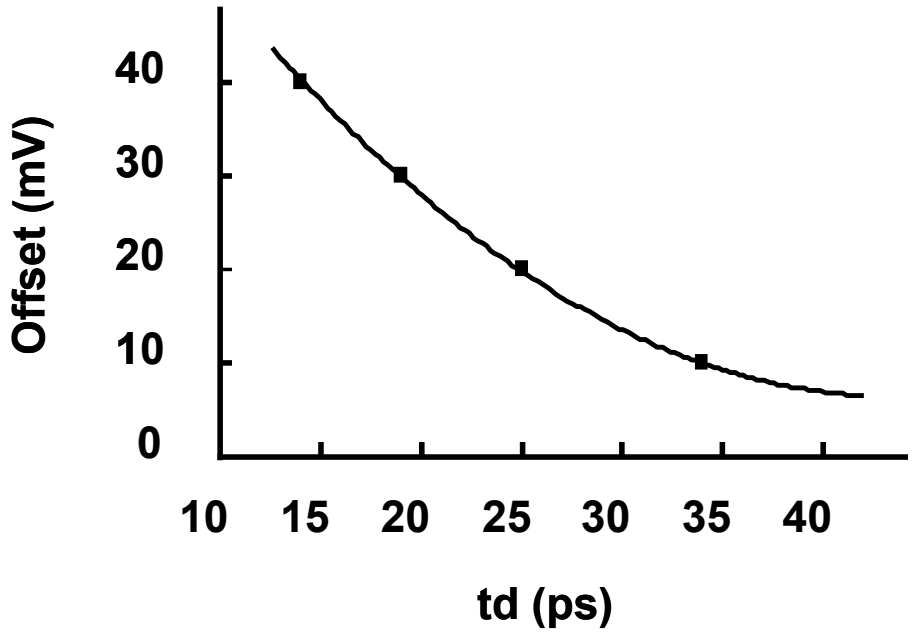


Figure 2.10 Simulated Relationship between Offset and Delay Time *td*.

There are two disadvantages of the proposed offset calibration method. First, the comparator noise is increased because the jitter of the digital timing control affects the comparator threshold voltage. Second, the implementation of the charge compensation transistors to some extent increases the comparator output loads and degrade the response speed. However, compared with the offset calibration using capacitors in [15], which makes use of the capacitance difference between channel-on and channel-off transistors, the timing control charge compensation technique can achieve the same offset control range with much smaller loading effect.

In this work, the comparator offset is calibrated before CDAC calibration to assure correct weight comparison. Since CDAC mismatches are caused by process variation, foreground calibration is selected for simplicity. In data conversion, voltage and temperature variations may change the comparator offset, which leads to the ADC offset rather than nonlinearity. Therefore, the VT variation effects are ignored here. In cases that more than one comparator are used, for example time-interleaved ADC, comparator offsets cause nonlinearity and should be calibrated in background.

2.3.3 Experimental Results

An 8-bit charge redistribution based successive approximation ADC with 4-bit + 4-bit split CDAC has been implemented in a 65 nm standard CMOS process. Figure 2.11 shows the chip micrograph. Both the split CDAC calibration circuit and the comparator offset calibration circuit have been implemented on chip. Metal-insulator-metal (MIM) capacitors are used in the CDAC arrays. The ADC occupies an active area of 0.2 mm × 0.15 mm.

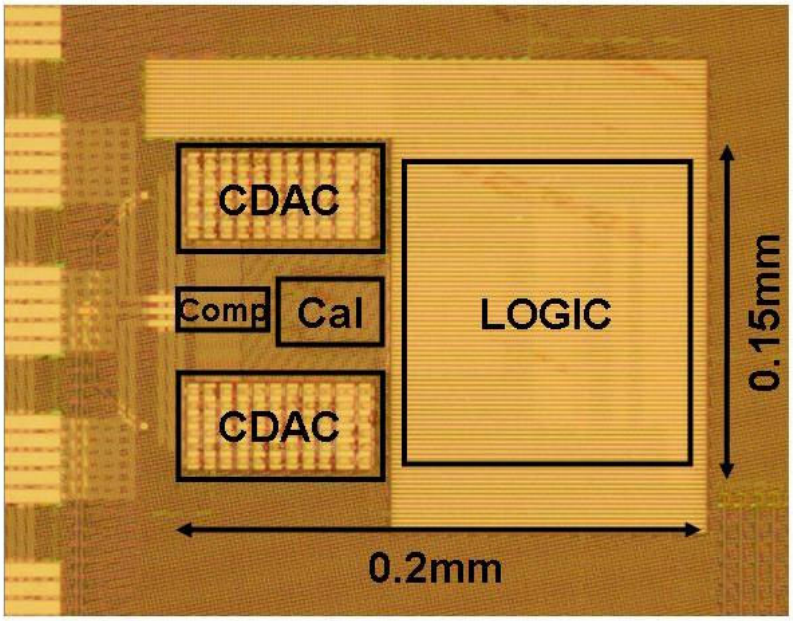


Figure 2.11 Chip Micrograph.

The static ADC performance is tested using a histogram (or code density) testing method [18, 19]. The histogram testing involves collecting a large number of digitized samples over a period of time, for a well-defined input signal with a known probability density function. The ADC transfer function is then determined by a statistical analysis of the samples. For example, a linear ramp waveform which slightly exceeds both ends of the range of the ADC is a popular histogram test signal. A large number of samples are collected for the ramp waveform input, and the numbers of occurrences of each code are tallied. If the ADC has no INL or DNL errors, all codes have equal probability of occurrence (with the exception of the end-point all "0"s and all "1"s codes), and there should be the same number of counts in each code bin. Because generating a high-precision linear ramp waveform is difficult, a much more practical method is to use a sine wave as the ADC input signal. Sine waves can be generated with extremely high linearity and low noise with appropriate filtering.

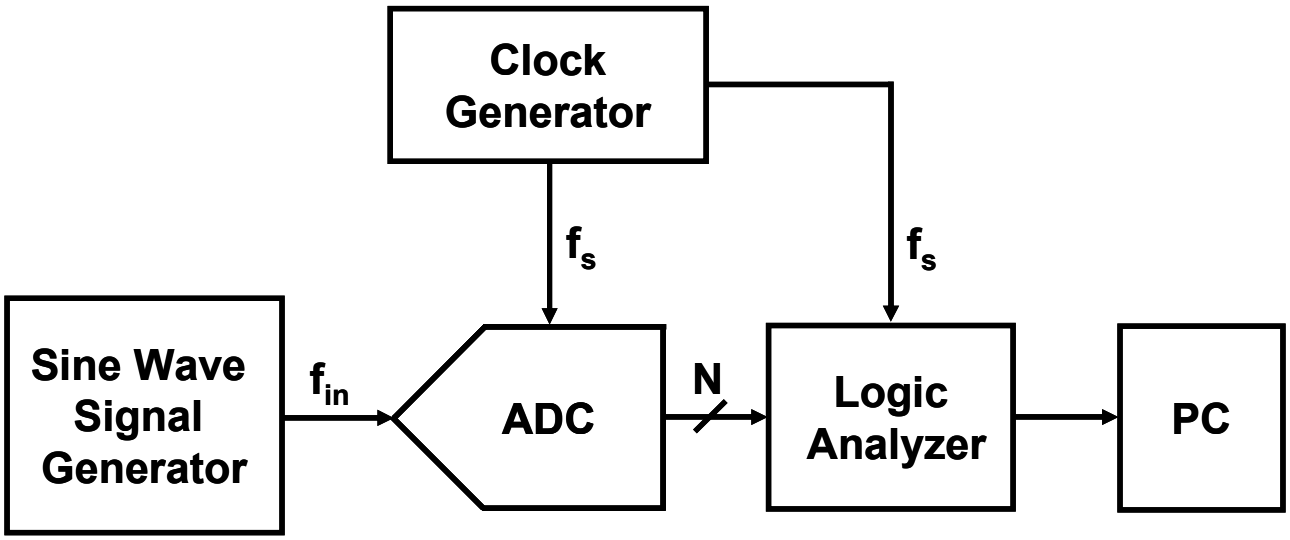


Figure 2.12 ADC Histogram Test Setup.

Figure 2.12 shows a typical histogram test setup. A sine-wave signal which slightly overdrives the ADC is applied. The frequency of the waveform should be low enough such that the ADC does not make ac-related errors, and the frequency must not be sub-harmonically related to the sampling frequency. A total of M_T samples are collected for codes 1 to $2^N - 2$. Notice that the "overflow" counts that fall in the all "0"s bin (code 0) and the all "1"s bin (code $2^N - 1$) are not included in the M_T total but still add to the total number of samples required. Therefore, the sinusoid waveform should be adjusted such that the number of overflow hits is no larger than needed to ensure that the ADC is sufficiently overdriven and that the portion of the waveform within the ADC range is linear to the required accuracy.

The sine wave input does not yield an equal probability for all codes. It can be shown [20-22] that for an N-bit ADC with a full-scale input range equal to $\pm V_{FS}$, and an input sine wave of amplitude A, the probability of occurrence of code n is given by:

$$p(n) = \frac{1}{\pi}\left\{\sin^{-1}\left[\frac{V_{FS}(n-2^{N-1})}{A\cdot 2^N}\right] - \sin^{-1}\left[\frac{V_{FS}(n-1-2^{N-1})}{A\cdot 2^N}\right]\right\} \qquad (2.10)$$

The Equation (2.10) is plotted in Figure 2.13. Notice that the probability of occurrence increases at the peaks of the sine wave near $\pm V_{FS}$ because the dv/dt is less (more hits per bin) than at the zero-crossing where the dv/dt is the highest (fewer hits per bin).

The number of occurrences ("hits"), $h(n)$, in each code bin, n, are then recorded for $n = 1$ to $n = 2^N - 2$. The theoretical number of hits in each bin (assuming perfect INL and DNL) is $h(n)_{Theoretical}$.

$$h(n)_{Theoretical} = p(n)M_T \tag{2.11}$$

If $h(n)_{Actual}$ is the actual number of hits in a bin, then the corresponding DNL of that particular code can be calculated as follows.

$$DNL(n) = \frac{h(n)_{Actual}}{h(n)_{Theoretical}} - 1 \tag{2.12}$$

Once the DNL is calculated, the INL is simply the integral of the DNL.

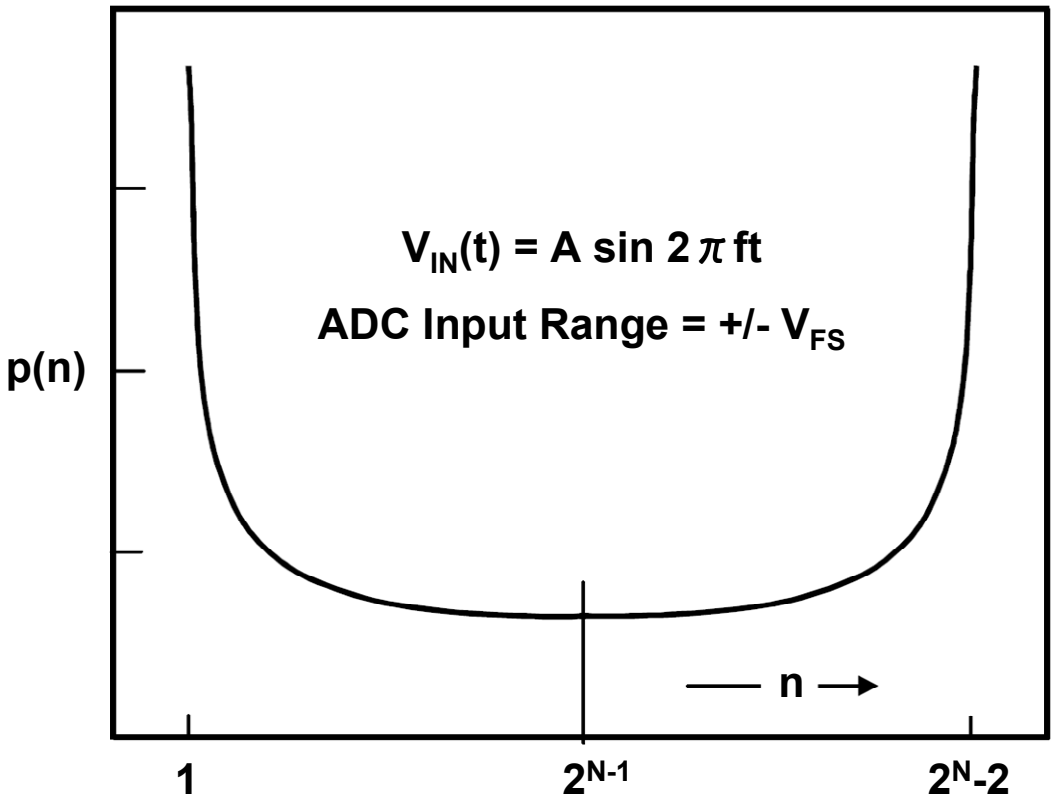
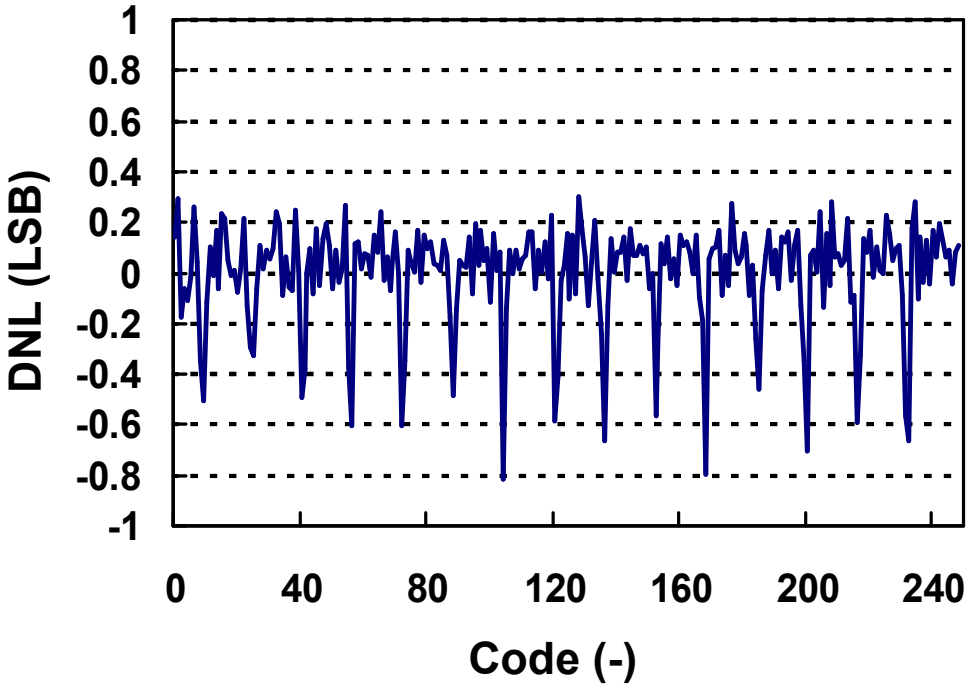


Figure 2.13 Sine-wave Probability Density Function.

Figure 2.14 and Figure 2.15 show the sine-wave histogram DNL and INL measurements of the 8-bit SAR ADC with split CDAC. The sampling rate of the ADC is 50 MS/s and the input sine-wave frequency is chosen to be 2.011 MHz, which is slow enough and is not a sub-harmonic of the sampling frequency. Figure 2.14 shows the static performance before the CDAC calibration. The DNL is +0.3/-0.8 LSB and the INL is +1.1/-0.6 LSB. The negative periodical peaks in the DNL data indicate that the LSB-side capacitor array has larger weight than the lowest bit capacitor in the MSB-side array. The INL is the integration of the DNL, and therefore peaks with the same period appear. Figure 2.15 shows the DNL and INL after the comparator offset is cancelled and the split CDAC calibration is carried out. They are improved to be +0.2/-0.3 LSB and +0.3/-0.3 LSB, respectively. Table 2.1 compares the static performance with two state-of-the-art SAR ADCs with medium sampling rates and medium resolutions.

Table 2.1 Comparison with Published Work.

Reference	[15]	[23]	This work
Technology (nm)	90	130	65
Sampling rate (MS/s)	40	50	50
Stated resolution (bits)	9	10	8
Input load capacitance (pF)	5	5.12	0.18
Core area (mm^2)	0.09	0.075	0.03
DNL (LSB)	+0.7 / -0.45	+0.88 / -1.0	+0.2 / -0.3
INL (LSB)	+0.56 / -0.65	+2.2 / -2.09	+0.3 / -0.3



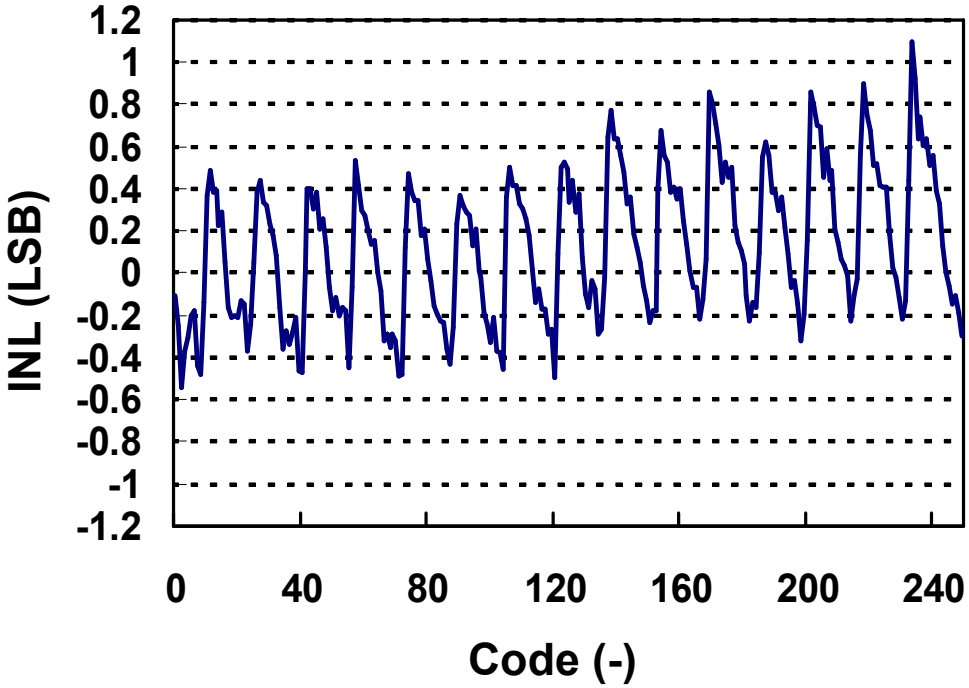
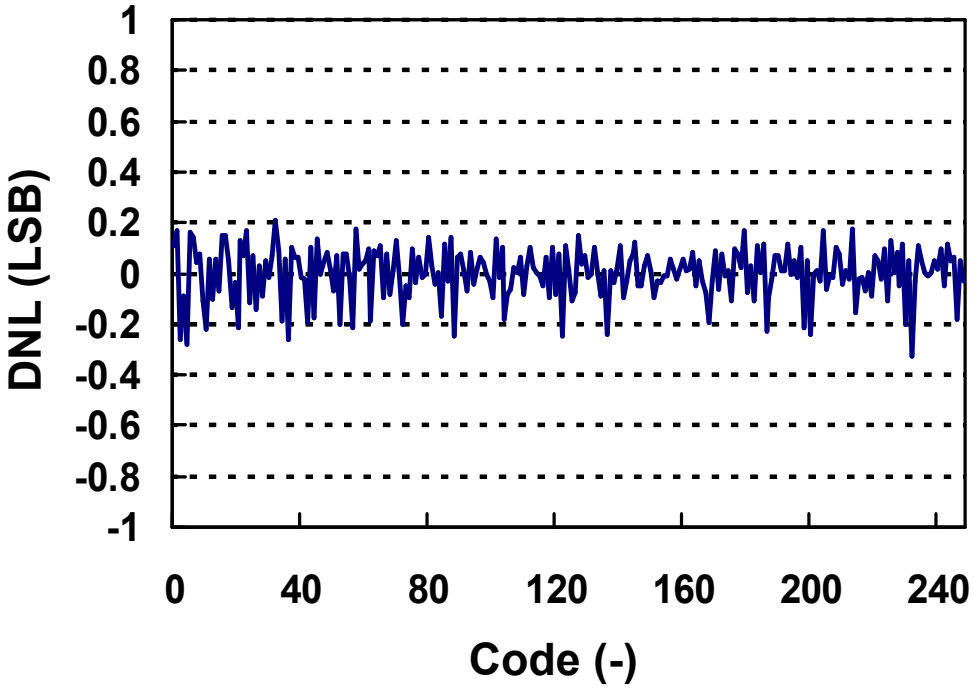


Figure 2.14 Measured DNL and INL Before Calibration.



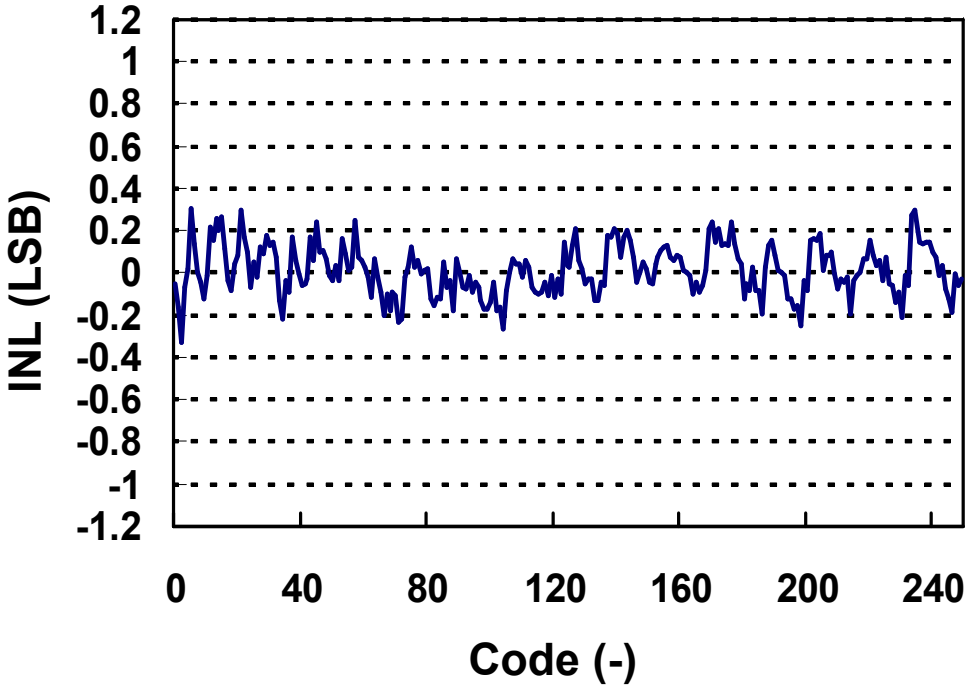


Figure 2.15 Measured DNL and INL After Calibration.

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Chapter 3 Tri-Level Charge Redistribution

3.1 Background

In the conventional charge redistribution SAR ADC, the bottom plates of the capacitor array are connected to the analog input signal during the sampling phase and switched to either a high reference voltage (V_{REF}) or a low reference voltage (ground) during the conversion phase [1,2]. The reference voltages charging and discharging the capacitor array consume energy in an inefficient way, which is demonstrated using a 2-bit charge redistribution ADC example shown in Figure 3.1 [2].

Initially, switch S_C is closed and the entire capacitor array fully stores the voltage V_{BIAS}-V_{IN}. Then at time 0, the bottom plate of the MSB capacitor, C_2 is connected to V_{REF}, and the LSB capacitor C_1 and the dummy capacitor C_0 are connected to ground. The capacitor array is charged to reach the final value in (3.2) so that the input signal is compared with $1/2V_{REF}$.

$$V_P[0] = V_{BIAS} \tag{3.1}$$

$$V_P[1] = V_{BIAS} - V_{IN} + \frac{V_{REF}}{2} \tag{3.2}$$

If the capacitor array settles in time T_1, the total energy drawn from V_{REF} is

$$E_{0\to1} = \int_0^{T_1} i_{REF}(t) V_{REF} dt = V_{REF} \int_0^{T_1} i_{REF}(t) dt \tag{3.3}$$

Since $i_{REF}(t) = -\frac{dQ_{C_2}}{dt}$, and charge continuity on a capacitor implies that $Q_{C_2}(0) = 2C(V_{BIAS} - V_{IN})$, Equation (3.3) can be calculated as

$$\begin{aligned} E_{0\to1} &= -V_{REF} \int_0^{T_1} \frac{dQ_{C_2}}{dt} dt = -V_{REF} \int_{Q_{C_2}(0)}^{Q_{C_2}(T_1)} dQ_{C_2} \\ &= -V_{REF}(Q_{C_2}(T_1) - Q_{C_2}(0)) = -V_{REF}(2C(V_P[1] - V_{REF}) - 2C(V_{BIAS} - V_{IN})) \\ &= CV_{REF}^2 \end{aligned} \tag{3.4}$$

This result matches the intuition that the effective series capacitance of the array, which is equal to C, must be charged from 0 to V_{REF}.

At the end of the first period of bit cycling, the value at the top plate of the capacitor array $V_P[1]$ is compared to V_{BIAS}. If the input signal V_{IN} is larger than $1/2V_{REF}$, C_2 keeps connected to V_{REF} and C_1 is also

connected to V_{REF}, raising the voltage at node P, called an up transition. The total energy drawn from V_{REF} in this case can be computed as follows.

$$V_P[2]_{up} = V_{BIAS} - V_{IN} + \frac{3}{4}V_{REF} \tag{3.5}$$

$$\begin{aligned} E_{1\to 2,up} &= -V_{REF}\int_{Q_{C_2}(T_1)}^{Q_{C_2}(T_2)} dQ_{C_2} - V_{REF}\int_{Q_{C_1}(T_1)}^{Q_{C_1}(T_2)} dQ_{C_1} \\ &= -V_{REF}(Q_{C_2}(T_2) - Q_{C_2}(T_1)) - V_{REF}(Q_{C_1}(T_2) - Q_{C_1}(T_1)) \\ &= -V_{REF}(2C(V_P[2] - V_{REF}) - 2C(V_P[1] - V_{REF})) - V_{REF}(C(V_P[2] - V_{REF}) - CV_P[1]) \\ &= \frac{1}{4}CV_{REF}^2 \end{aligned} \tag{3.6}$$

If, on the other hand, the input signal V_{IN} is smaller than $1/2V_{REF}$, C_2 is returned to ground and C_1 is connected to V_{REF}, called a down transition. The energy drawn from V_{REF} in this case while the capacitor array settles can be calculated as

$$V_P[2]_{down} = V_{BIAS} - V_{IN} + \frac{1}{4}V_{REF} \tag{3.7}$$

$$\begin{aligned} E_{1\to 2,down} &= -V_{REF}\int_{Q_{C_1}(T_1)}^{Q_{C_1}(T_2)} dQ_{C_1} = -V_{REF}(Q_{C_1}(T_2) - Q_{C_1}(T_1)) \\ &= -V_{REF}(C(V_P[2] - V_{REF}) - CV_P[1]) \\ &= \frac{5}{4}CV_{REF}^2 \end{aligned} \tag{3.8}$$

The ratio of (3.8) to (3.6) hints at a significant inefficiency, since it requires five times more energy to lower V_P than to raise it by the same amount. Several techniques have been developed to reduce the DAC switching energy drawn from the reference [3-5]. In [3], the MSB capacitor is split into a binary-scaled sub-capacitor array which is exactly the same as the entire capacitor array excluding the MSB, and the switching energy consumed in the down-transition process is reduced by five times and becomes the same as that consumed in the up transition. However, the digital control circuits become much more complex and consume extra power. In [4] charging and discharging capacitors are done in multiple steps to achieve ultra low switching energy. Capacitors are charged from 0 to $1/3V_{REF}$, then to $2/3V_{REF}$, and finally to V_{REF}, rather than being charged from 0 directly to V_{REF}. However, this work only targets in low sampling-rate application.

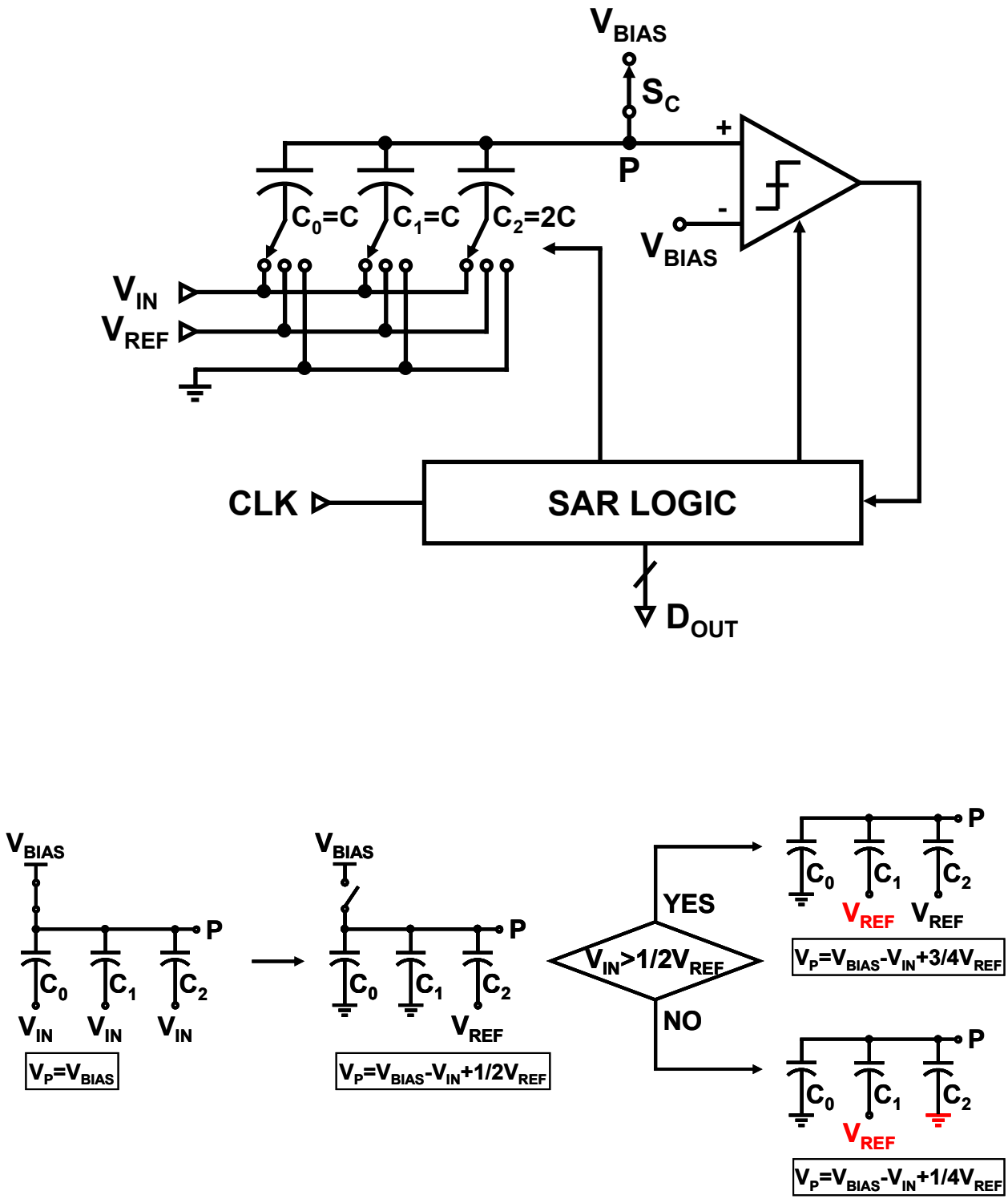


Figure 3.1 2-Bit Conventional Charge Redistribution ADC.

Set-and-down switching technique in [5] pre-charges all the capacitors to V_{REF} and only enables down transitions so as to reduce the DAC switching energy and settling time without complicating control logic circuits. Due to asymmetric capacitor settling in the differential DAC, the output common-mode voltage varies with the analog input, degrading the linearity performance. Top-plate sampling is used in [4] and [5], where the MSB does not need to be set. However, it is inevitable to implement bootstrapped sampling switches and signal-dependent charge injection distortion is likely to occur.

Besides the switching energy efficiency, another main concern of the DAC performance is the settling speed. Generally speaking, the DAC output settling time is determined by the capacitance of the capacitor array and the on-resistance of the switch array. The first bit settling of the DAC output voltage can be expressed as follows before it reaches the final value in (3.2).

$$V_P[t] = V_P[0] + (V_P[1] - V_P[0])(1 - e^{-\frac{t}{rc}}) \tag{3.9}$$

In the first bit settling, all the capacitors are disconnected form V_{IN}. The MSB capacitor C_2 is connected to V_{REF}, and the LSB capacitor C_1 and the dummy capacitor C_0 are connected to ground. The above equation assumes that the capacitors are switched exactly at the same time. However, if C_2 is switched earlier than C_1 and C_0, the DAC output settles as the upper curve plotted in Figure 3.2. If, on the contrary, C_1 and C_0 are switched earlier than C_2, V_P settles as the lower curve in Figure 3.2. Either case might occur when there are mismatches in the switch driving logic circuits and takes longer settling time than that determined by the rc constant.

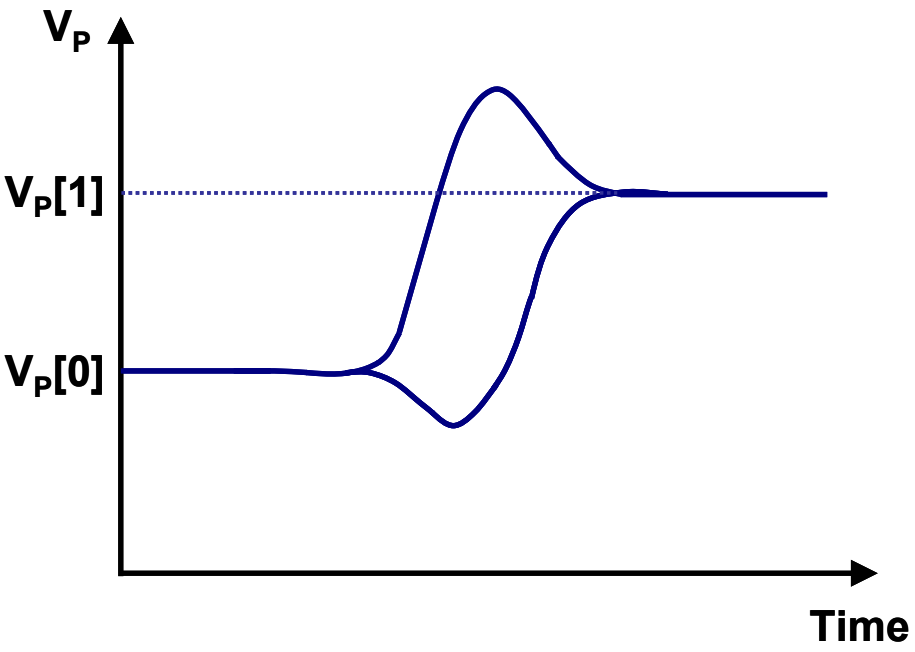


Figure 3.2 MSB Settling of DAC Output with Switch Driving Mismatches.

Similarly the second bit settling of the DAC output can be written as:

$$V_P[t] = V_P[1] + (V_P[2] - V_P[1])(1 - e^{-\frac{t}{rc}}) \tag{3.10}$$

If it is an up transition, the bottom plates of C_2 and C_0 keep the previous voltage, and only C_1 is switched from ground up to V_{REF}. So the DAC settling is not affected by switch driving mismatches. If it is a down transition, C_2 and C_1 need to be switched at the same time yet in the opposite directions. If C_1 is switched from ground to V_{REF} earlier than C_2 switched from V_{REF} down to ground, the DAC output settles as the upper curve plotted in Figure 3.3. If C_2 is switched earlier than C_1, the DAC output settles as the lower curve in Figure 3.3. Obviously, the above two cases also degrade the DAC settling speed.

To eliminate the overshooting problem in the DAC output settling and improve the speed, one method is to control the mismatches in the switch driving logic circuits, which causes larger power consumption. As will be discussed in the next section, avoiding two capacitors being switched simultaneously in the opposite directions fundamentally solves the overshooting problem.

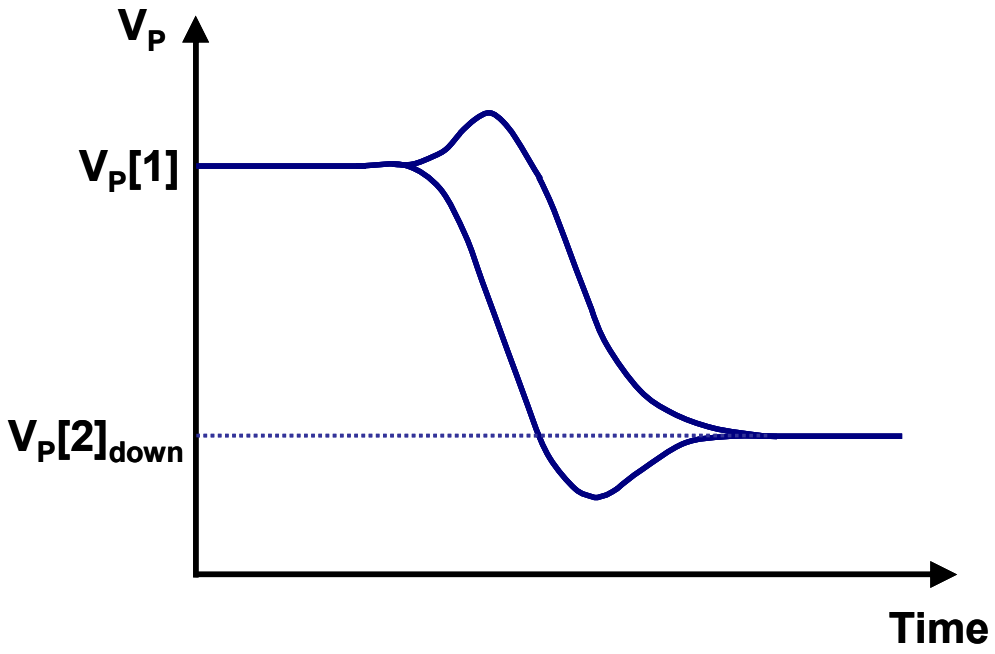


Figure 3.3 Down Transition Settling of DAC Output with Switch Driving Mismatches.

3.2 Tri-Level Charge Redistribution

This work proposes a tri-level charge redistribution technique [6] to reduce the DAC switching energy and improve the settling speed at the same time. The tri-level technique helps simplifying the SAR control logic circuits as well. Bottom-plate sampling is used, so there is no signal-dependent charge injection and bootstrapped switches are not necessary. The proposed DAC is shown in Figure 3.4. The sampling phase is exactly the same as the conventional design. Initially the top plates of the capacitor array are connected to V_{BIAS} while the bottom plates are connected to the input voltage V_{IN}. During the first bit estimation (at time 0), however, all capacitor bottom plates are switched from V_{IN} to V_{CM}, which is the middle point voltage between V_{REF} and ground (V_{CM}= V_{REF}/2). The top plates are floating and settle to V_{BIAS}-V_{IN}+V_{CM}, which is the same as Equation (3.2). Therefore, the input signal is also compared with V_{REF}/2. The voltage stored on the effective

series capacitor of the array, which is equal to C, keeps being zero. So this step does not consume any switching energy, which means:

$$E_{0\to1} = 0 \tag{3.11}$$

If the input is larger than $V_{REF}/2$, C_2 will be switched from V_{CM} to V_{REF} so that the input can be compared with $3/4V_{REF}$. The energy drawn from V_{REF} in this up-transition step can be calculated as follows.

$$\begin{aligned} E_{1\to2,up} &= -V_{REF}\int_{Q_{C_2}(T_1)}^{Q_{C_2}(T_2)} dQ_{C_2} \\ &= -V_{REF}(Q_{C_2}(T_2) - Q_{C_2}(T_1)) \\ &= -V_{REF}(2C(V_P[2] - V_{REF}) - 2C(V_P[1] - V_{CM})) \\ &= \frac{1}{2}CV_{REF}^2 \end{aligned} \tag{3.12}$$

If the input is smaller than $V_{REF}/2$, C_2 will be switched from V_{CM} to ground so that the input can be compared with $1/4V_{REF}$. In the down transition step there is no capacitor connected to V_{REF} and therefore no energy drawn from V_{REF}.

$$E_{1\to2,down} = 0 \tag{3.13}$$

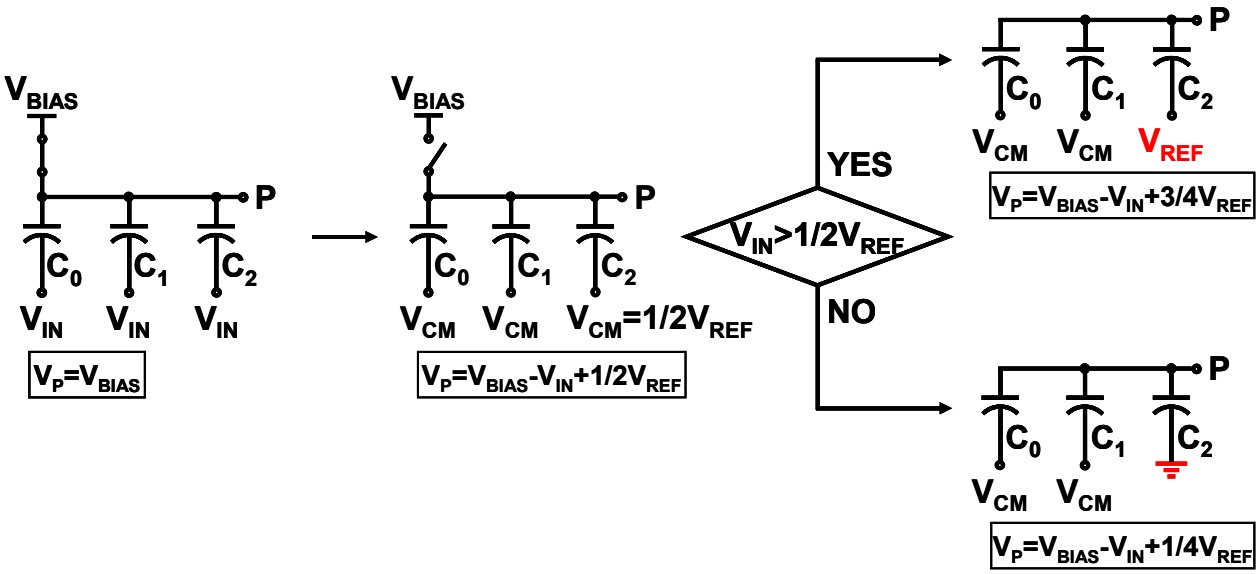


Figure 3.4 Proposed Tri-Level Charge Redistribution DAC.

Compared (3.11) ~ (3.13) with (3.4), (3.6) and (3.8), it is obvious that the tri-level DAC consumes much smaller switching energy drawn from V_{REF} than the conventional DAC on average. However, it is unfair to exclude the switching energy drawn from the extra reference V_{CM} in the comparison. Actually it is undesirable to generate the extra reference voltage on chip because it will cause extra power consumption. This work also proposes a differential DAC capacitor bottom-plate charge-sharing technique, which will be discussed later in this section, to avoid the implementation of the extra reference V_{CM} so that the tri-level charge redistribution can be realized with very low power consumption.

The tri-level charge redistribution DAC has intrinsically one more bit resolution than the conventional DAC. As shown in Figure 3.5, C_2 is switched to V_{REF} or ground based on the first bit decision. If the input signal is larger than $1/2V_{REF}$, the MSB is "1" and C_2 is switched to V_{REF}, which makes the next digital estimate become $3/4V_{REF}$. The input voltage is then compared with $3/4V_{REF}$. The next comparator result determines the second bit. If the input is larger than $3/4V_{REF}$, the second bit will be "1" and C_1 will be switched to V_{REF}. With the settling of C_1, the next digital estimate becomes $7/8V_{REF}$. If the input is smaller than $3/4V_{REF}$, the second MSB will be "0" and C_1 will be switched to ground, setting the next digital estimate $5/8V_{REF}$. The final comparator result determines the third bit. It is similar for the case that MSB is "0".

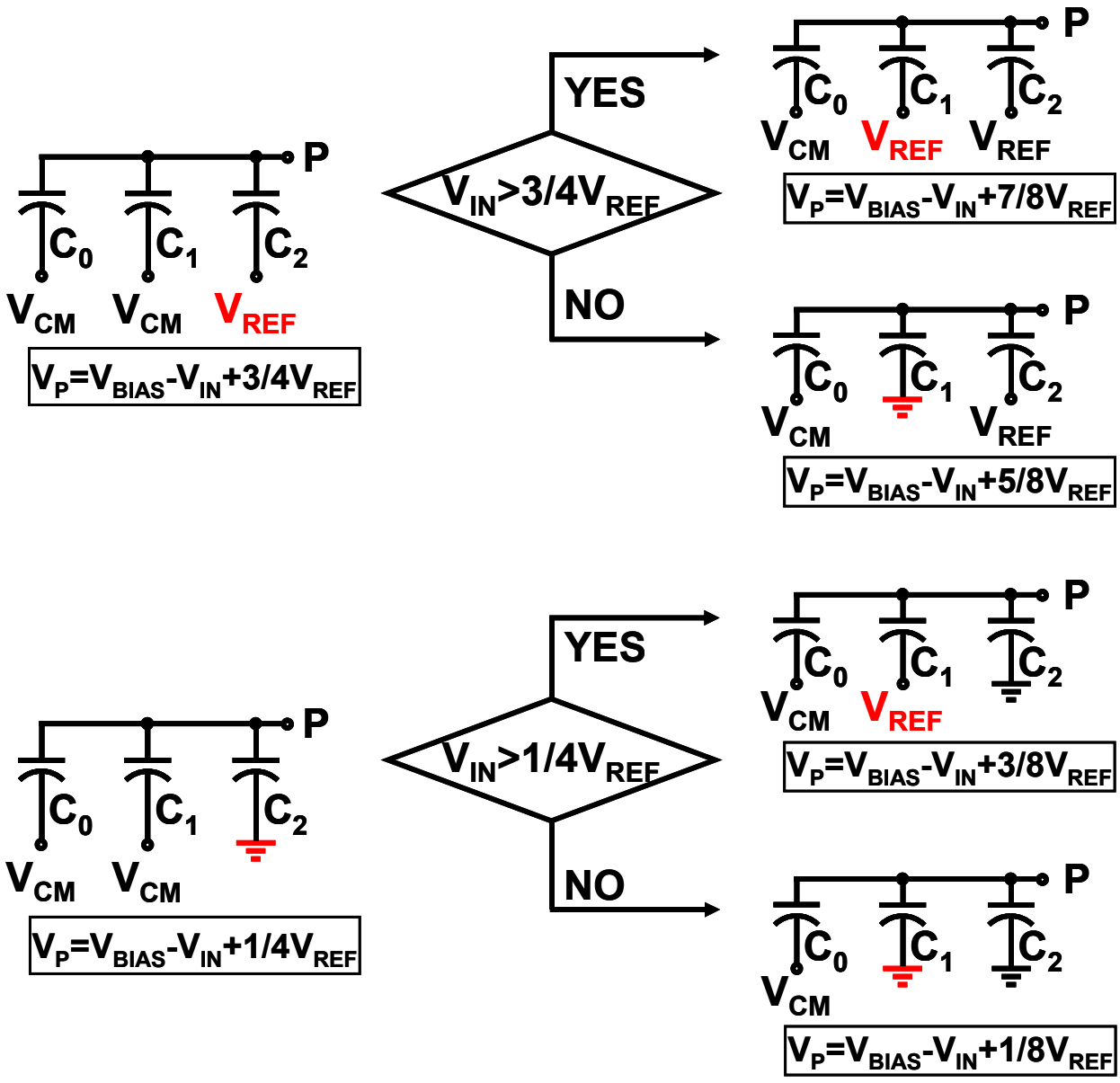


Figure 3.5 Extra Bit Resolution in The Tri-Level DAC.

Therefore, the 2-bit capacitor array implementing tri-level charge redistribution has an effective resolution of 3-bit. In other words, to meet the same resolution requirements, the tri-level DAC can implement one bit less capacitor array than the conventional DAC. Generally speaking, the smallest capacitance (unit capacitance) in the DAC array is determined by device matching, which is limited by process variation. Designed in the same process and targeting the same resolution, the tri-level DAC occupies twice smaller area than the conventional one if both of them implement binary-weighted capacitor array. Furthermore, the switching energy calculation in (3.4), (3.6), (3.8), (3.11) ~ (3.13) assumes that the proposed tri-level DAC has the same MSB capacitance as the conventional DAC. With the same unit capacitance, the MSB capacitance in the tri-level DAC is in fact twice smaller than the conventional one, making the switching energy saving twice larger.

To eliminate the need for generating the extra reference voltage V_{CM}, we propose a differential DAC capacitor bottom-plate charge-sharing technique. The tri-level charge redistribution DAC is implemented in the differential structure, as shown in Figure 3.6. The capacitor top plate nodes P_P and P_N are connected to the comparator differential inputs. During the sampling period, the differential input signal V_{INP} and V_{INN} are sampled by the bottom plates of the differential capacitor arrays in the DAC. The top plates of both differential arrays are connected to V_{BIAS}. Then during the first bit estimation, the top plates are disconnected from the bias voltage and become floating, and the bottom plates of the two differential capacitor arrays are disconnected from the differential input voltages and connected with each other through the switch arrays. The capacitor bottom-plate charge sharing achieves voltage averaging and therefore the bottom plate voltage of both differential capacitor arrays becomes the input signal common mode voltage $(V_{INP} + V_{INN})/2$, which is equal to V_{CM}. The p-channel capacitor array top plates are charged to reach the value:

$$V_{P_P}[1] = V_{BIAS} - V_{INP} + V_{CM} \tag{3.14}$$

The n-channel capacitor array top plates are charged to reach the value:

$$V_{P_N}[1] = V_{BIAS} - V_{INN} + V_{CM} \tag{3.15}$$

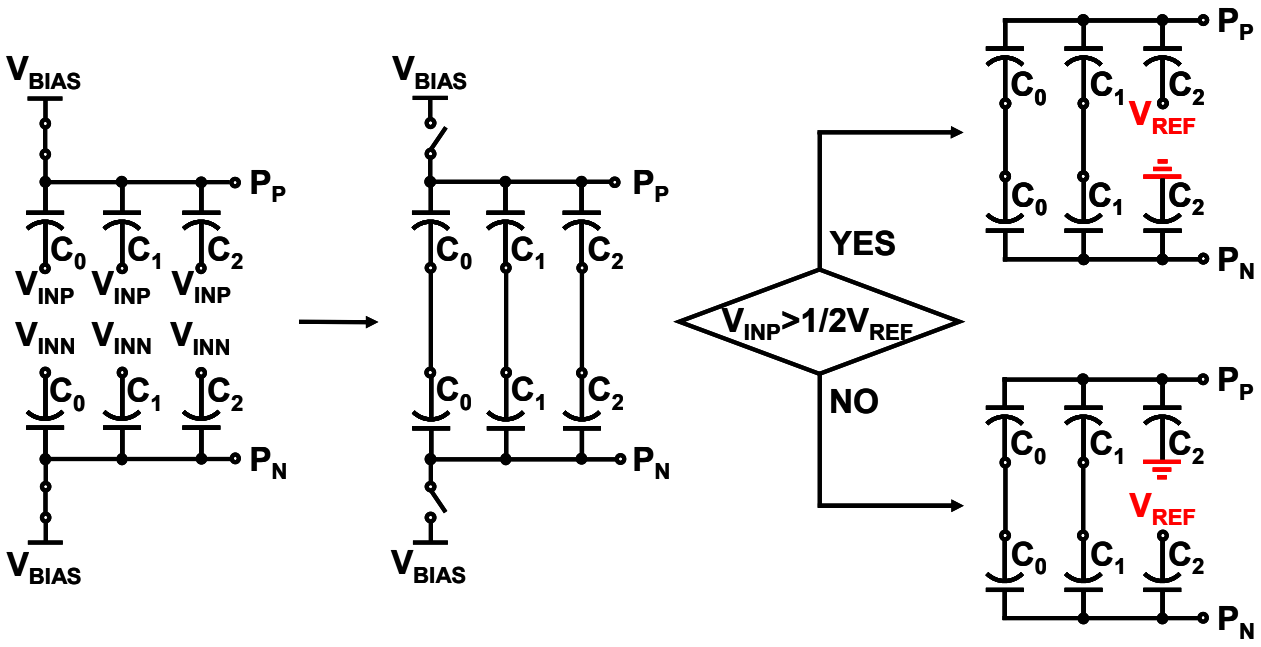


Figure 3.6 Differential Tri-Level Charge Redistribution DAC.

The above two voltages (3.14) and (3.15) are compared with each other to determine which one is larger than $V_{REF}/2$ and which one is smaller than $V_{REF}/2$. As explained earlier, this step does not consume switching energy drawn from V_{REF}. The bottom-plate charge sharing is simply a passive process and does not consume extra energy.

If V_{INP} is larger than $V_{REF}/2$, the MSB capacitors in the differential DAC will be disconnected from each other. C_2 in the p-channel array will be switched to V_{REF} and C_2 in the n-channel array will be switched to ground. The top plate node voltages become as follows.

$$V_{P_P}[2]_{up} = V_{BIAS} - V_{INP} + \frac{3}{4}V_{REF} \tag{3.16}$$

$$V_{P_N}[2]_{up} = V_{BIAS} - V_{INN} + \frac{1}{4}V_{REF} \tag{3.17}$$

The differential input voltage V_{INP} -V_{INN} is compared with $V_{REF}/2$, which is equivalent to the comparison between V_{INP} and 3/4V_{REF} (or between V_{INN} and 1/4V_{REF}). The switching energy drawn from V_{REF} in this step

is the sum of (3.9) and (3.10), which is equal to $\frac{1}{2}CV_{REF}^2$.

If V_{INP} is smaller than $V_{REF}/2$ ($V_{INP} < V_{INN}$), C_2 in the p-channel array will be switched to ground and C_2 in the n-channel array will be switched to V_{REF}. The differential structure makes the down transition very similar to the up transition. The top plate node voltages are:

$$V_{P_P}[2]_{down} = V_{BIAS} - V_{INP} + \frac{1}{4}V_{REF} \tag{3.18}$$

$$V_{P_N}[2]_{down} = V_{BIAS} - V_{INN} + \frac{3}{4}V_{REF} \tag{3.19}$$

The differential input voltage V_{INP} -V_{INN} is compared with -$V_{REF}/2$, which is equivalent to the comparison between V_{INP} and $1/4V_{REF}$ (or between V_{INN} and $3/4V_{REF}$). The switching energy in this step is also equal to $\frac{1}{2}CV_{REF}^2$.

The input common-mode level effectively becomes the third reference level. If there exists some noise, the stability of this level will be disturbed. However, thanks to the differential structure, fluctuation of the input common-mode voltage will not affect the expected operation. Suppose the input common-mode voltage $V_{INCM}=1/2V_{REF}+\Delta$. After the bottom-plate charge sharing, both P-channel and N-channel bottom-plate voltages become $1/2V_{REF}+\Delta$. Voltages at node P_P and P_N become as follows.

$$V_{P_P} = V_{BIAS} - V_{INP} + \frac{1}{2}V_{REF} + \Delta \tag{3.20}$$

$$V_{P_N} = V_{BIAS} - V_{INN} + \frac{1}{2}V_{REF} + \Delta \tag{3.21}$$

Therefore the differential DAC output is $V_{P_{diff}} = -V_{INP} + V_{INN}$, which is not affected by Δ.

If $V_{INP}>V_{INN}$ (or $V_{INP}>V_{INCM}$), the capacitor settling follows the "YES" path. C_2 in the P-channel is charged from $1/2V_{REF}+\Delta$ to V_{REF}, so the voltage at node P_P becomes:

$$V_{P_P} = V_{BIAS} - V_{INP} + \frac{1}{2}V_{REF} + \Delta + \frac{1}{2}(\frac{1}{2}V_{REF} - \Delta) = V_{BIAS} - V_{INP} + \frac{3}{4}V_{REF} + \frac{\Delta}{2} \tag{3.22}$$

C_2 in the N-channel is discharged from $1/2V_{REF}+\Delta$ to ground, so the voltage at node P_P becomes:

$$V_{P_N} = V_{BIAS} - V_{INN} + \frac{1}{2}V_{REF} + \Delta - \frac{1}{2}(\frac{1}{2}V_{REF} + \Delta) = V_{BIAS} - V_{INN} + \frac{1}{4}V_{REF} + \frac{\Delta}{2} \tag{3.23}$$

The differential DAC output becomes $V_{P_{diff}} = -V_{INP} + V_{INN} + \frac{1}{2}V_{REF}$. This is not related to Δ either. The "NO" path can be similarly analyzed. Therefore, the differential ADC operation will not be affected by the input common-mode fluctuation.

Figure 3.7 plots the normalized switching energy of the conventional DAC and the proposed tri-level DAC with respect to the output digital code. Both DAC capacitor arrays implement differential structures and have 9-bit resolution. Due to the intrinsic extra bit resolution, the MSB capacitor in the tri-level DAC is half size of that in the conventional one. Both the conventional DAC and the tri-level DAC use the same unit capacitance. The overall saving of energy drawn from the reference supply depends on the input signal. At the highest output code, all transitions are up, so the conventional DAC consumes the least switching energy. At lower output codes, more down transitions occur in the capacitor array, causing more switching energy for the conventional DAC. As for the differential tri-level charge redistribution DAC, up transition and down transition consume the same switching energy, so the total switching energy is independent on the output code. Therefore, the energy savings are greatest for the tri-level method at the lowest output code. Given a uniformly distributed input signal, the tri-level charge redistribution method saves 86% of the switching energy compared to the conventional DAC on average.

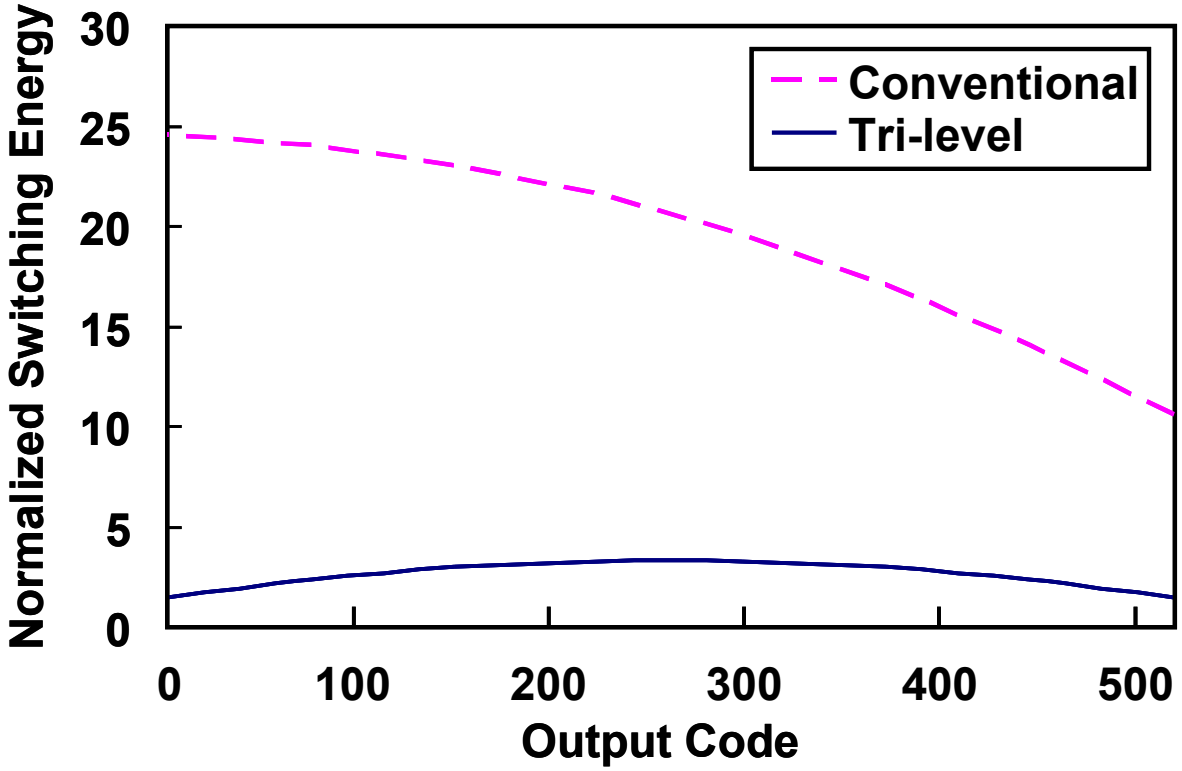
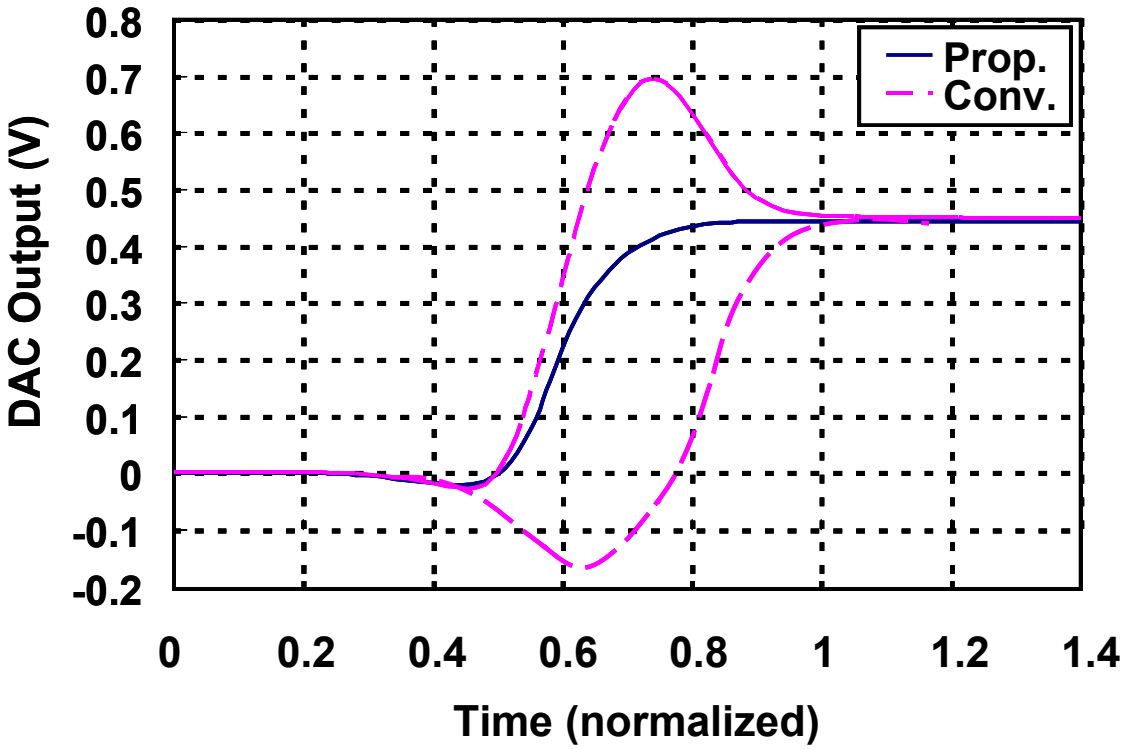


Figure 3.7 Switching Energy versus Output Code.

In the conventional DAC design, overshooting problems of DAC output settling occur when mismatches exist in the switch driving logic circuits, and thus degrade the settling speed. However, the proposed tri-level DAC doesn't have overshooting problems. In the first bit estimation, all the capacitors are disconnected from V_{IN} and switched to V_{CM}. Even if there are mismatches in the switch driver circuits, no overshooting will happen because all the capacitors are switched in the same direction. In either up transition or down transition of the bit cycling, only one capacitor is switched at a time, and therefore there is no overshooting problem. The settling time of the tri-level DAC only depends on the *rc* constant. Figure 3.8 is the simulation results of the first bit settling and down-transition settling for both the conventional DAC and the tri-level DAC.



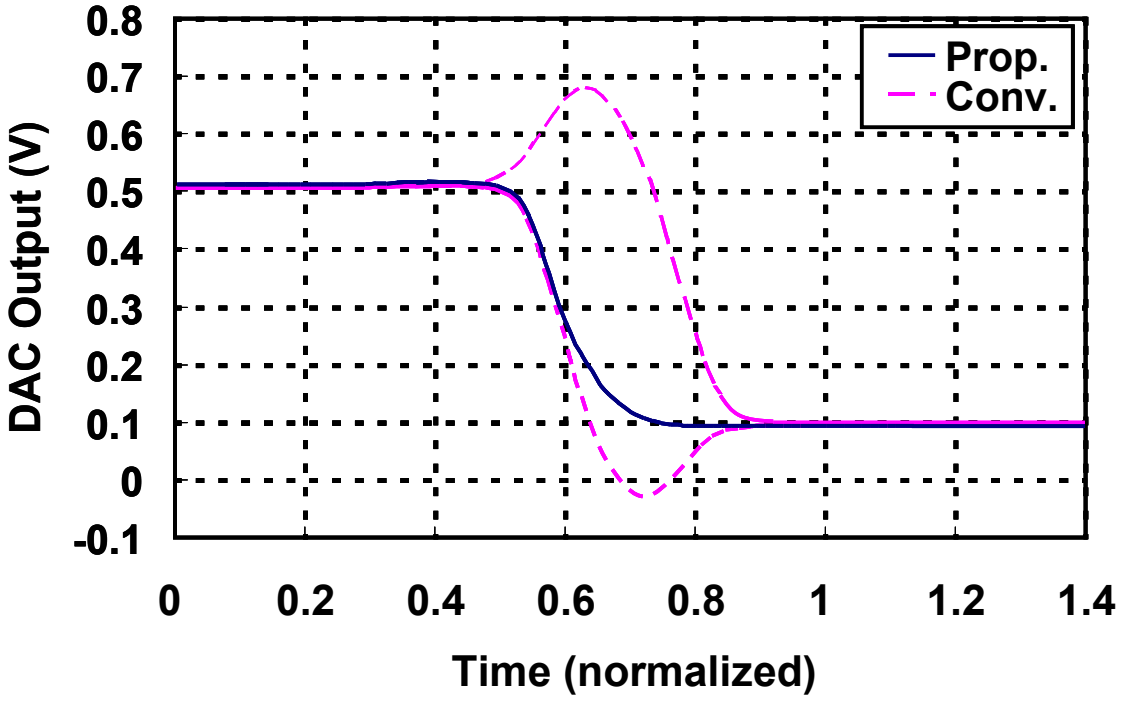


Figure 3.8 Simulated Output Settling of the Conventional and Proposed DAC with Switch Driving Mismatches (a) MSB Settling (b) Down-Transition Settling.

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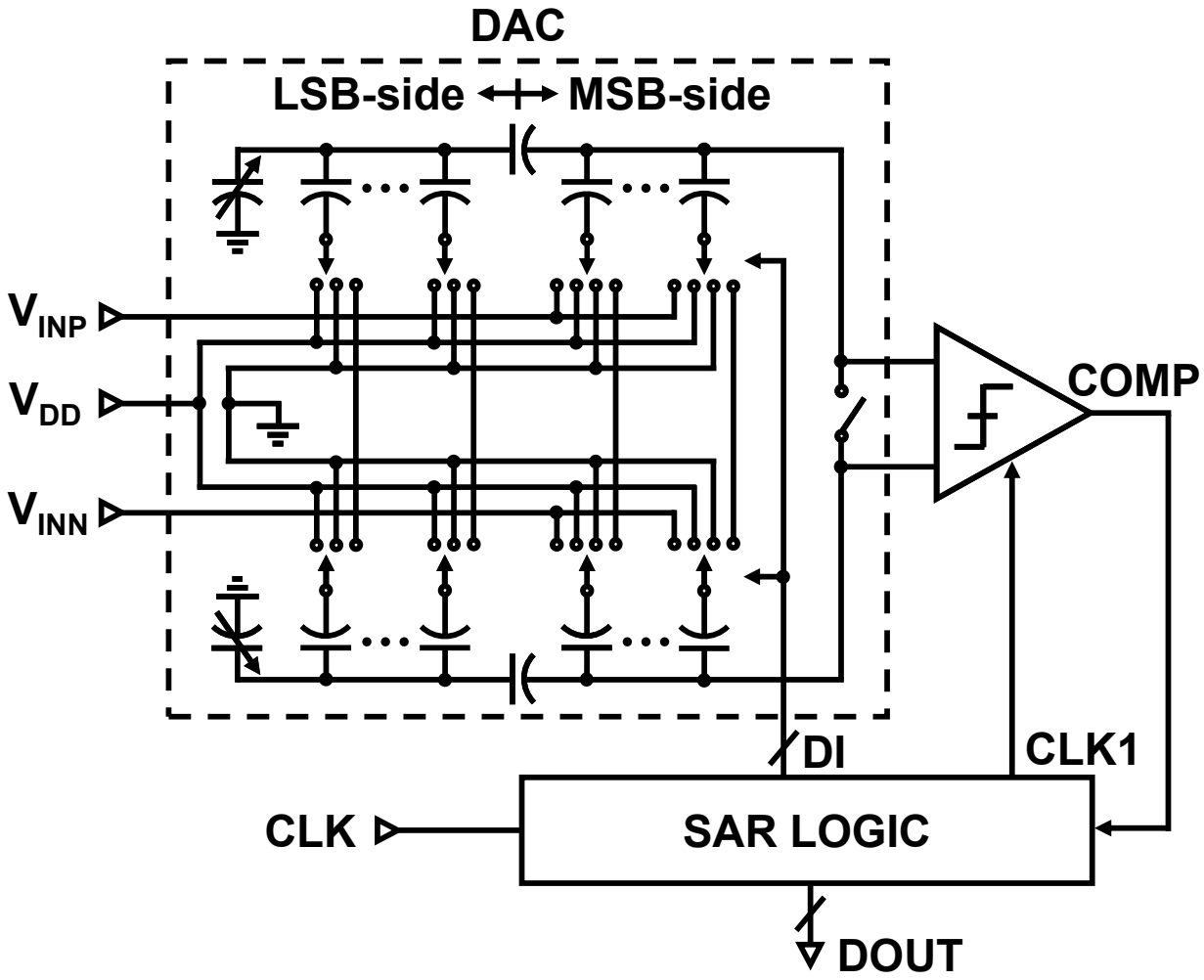
Chapter 4 9-Bit 100-MS/s SAR ADC Design

4.1 ADC Architecture

The ADC architecture is shown in Figure 4.1, consisting of a capacitive DAC, a comparator and SAR control logic circuits. Differential structure is implemented for good common-mode noise rejection and small distortion. The split CDAC calibration and the tri-level charge redistribution techniques presented in the previous two chapters are combined together in the ADC design [1]. The bottom-plate sampling separates the input signal from the sensitive floating top plates to avoid the signal-dependent charge injection and eliminate the necessity for bootstrapped switches. To avoid on-chip reference generation and therefore save power and cost, any reference voltage different from the supply voltage is removed. The supply voltage and ground are chosen to charge and discharge the capacitors during conversion. This also sets a rail-to-rail input range of the converter, which relieves noise requirements. Asynchronous processing technique [2] is used to remove the need for GHz clock generation and speed up the SAR algorithm. The SAR control logic circuits are simplified due to the tri-level charge redistribution.

The timing diagram is also shown in Figure 4.1. The external system clock *CLK* defines the sampling phase. When *CLK* is high, the top plates of the differential MSB-side capacitor arrays are connected with each other and the bottom plates are connected to the differential analog input signal [3]. When *CLK* is low, the bottom plates of both MSB-side and LSB-side capacitors can be switched between the supply voltage V_{DD} and ground. The bottom plates of the differential capacitor arrays are also designed to be connectable with each other so that the tri-level charge redistribution can be achieved by simple passive charge sharing. The comparator is triggered by an internal asynchronous clock *CLK1*, which is generated by detecting the outputs of the comparator itself. When all 9 bits are resolved, an end of conversion signal is given to stop the internal clock and thus power down the converter until the next sampling phase comes.

Design details of each ADC building blocks: DAC, comparator and SAR control logic, will be explained in the three following sections. The final section will present the measurement results and comparison with other state-of-the-art work.



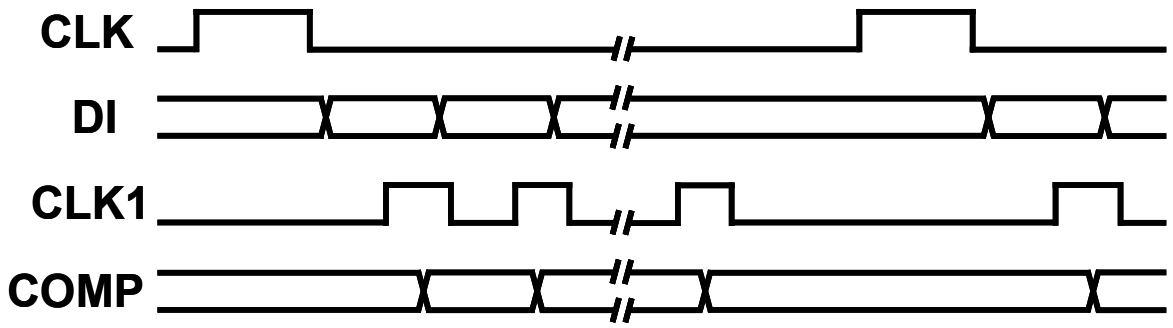


Figure 4.1 ADC Architecture with Timing Diagram.

4.2 DAC Design

The DAC design combines the calibrated split capacitor array with tri-level charge redistribution technique, which is shown in Figure 4.2. The 9-bit resolution is achieved with 4-bit + 4-bit split capacitor arrays, thanks to the intrinsic extra-bit resolution of the tri-level method.

Mismatches between the MSB-side and LSB-side capacitors caused by fractional value bridge capacitor and parasitic capacitance are compensated by the calibration capacitor C_C in parallel with the LSB-side capacitor arrays, which is adjustable in the range from 0 to 7.5C. Rather than the thermometer implementation shown in Chapter 2, here C_C is designed to be composed of 4-bit binary weighted capacitors with the smallest capacitor being 0.5C. The bottom plates of C_C are connected to ground and top plates are connected to node Q through switches. A 4-bit digital code generated off chip is applied to control the capacitance of C_C so that the total weight of the LSB-side capacitors can be adjusted to be equal to the weight of the lowest bit in the MSB-side array. The unit capacitance C is 11fF.

Differential charge-sharing technique is applied to both the top plates and the bottom plates of the capacitor arrays. During the sampling period, the differential input signal V_{INP} and V_{INN} are sampled by the differential MSB-side capacitor arrays. The LSB-side capacitors are connected to either "1" or "0" depending on the previous data conversion result. Therefore, the input load capacitance is reduced to 16 C, which is 16 times smaller than a full binary-weighted array. The top plates of both the MSB-side and LSB-side capacitor arrays are biased to the input common-mode voltage of the comparator. Since the top plates of the differential capacitor arrays have differential voltages during the conversion phase, switches are implemented to connect the differential top plates for charge sharing and thus voltage averaging. Furthermore, these switches help avoiding asymmetrical charge injection to the sensitive top-plate nodes at the end of the sampling phase.

During the conversion phase, the top-plate nodes all become floating. The bottom plates of the differential MSB-side capacitor arrays are disconnected from the inputs and connected with each other through switch arrays. Charge sharing leads to voltage averaging and the bottom plate voltage of both differential capacitor arrays becomes the input signal common mode voltage. The bottom plates of the

differential LSB-side capacitor arrays are also connected with each other through switch arrays. The charge sharing technique still works here, because the differential capacitors always have inverse digital codes in the conversion process. After the differential capacitor bottom plates are connected with each other, both of them achieve the middle point voltage. Thus the tri-level charge redistribution effects can be achieved without actually implementing a third reference voltage. The input common-mode voltage effectively becomes the third reference level. Fortunately, the fully differential implementation is intrinsically robust with common-mode noise, and therefore fluctuations of the input common-mode voltage will not affect the expected operation.

To avoid on-chip reference generation and thus save power and cost, any reference voltage different from the supply voltage is undesirable. Therefore, the high reference in the charge redistribution is chosen to be the supply voltage V_{DD} and the low reference is ground, which also leads to a rail-to-rail input range of the ADC. The voltage swing in both node *P* and node *Q* need to be taken into consideration since they are floating during the conversion phase. Figure 4.3 depicts the largest swing in node *P* and node *Q*, both of which have the largest range of V_{DD}. Therefore, the bias voltage of both node *P* and node *Q* during the sampling phase are chosen to be the middle point $1/2V_{DD}$ so that they can always swing between V_{DD} and ground. To avoid voltage shifting of floating nodes, a dynamic voltage division circuit consisting of two identical resistors and switches generates the middle point voltage $1/2V_{DD}$ connecting to node *P* and *Q*, as shown in Figure 4.2. Since the main function of the $1/2V_{DD}$ supply circuit is to prevent the top-plate nodes from being always floating, rather than charging the whole array to $1/2V_{DD}$, the current is designed to be very small, <0.1mA. ϕS is a clock signal of 10% duty cycle, so the average current is less than 0.01mA, which is ignorable. In the end of the sampling phase, the switches connecting the differential capacitor top plates are turned off by $\phi S'$, a delayed clock of ϕS, in order to reduce charge injection mismatches and also relieve the accuracy requirement of the $1/2V_{DD}$ supply circuit. As long as the differential capacitor top plates have the same voltage, which keeps close to $1/2V_{DD}$, the converter can perform properly.

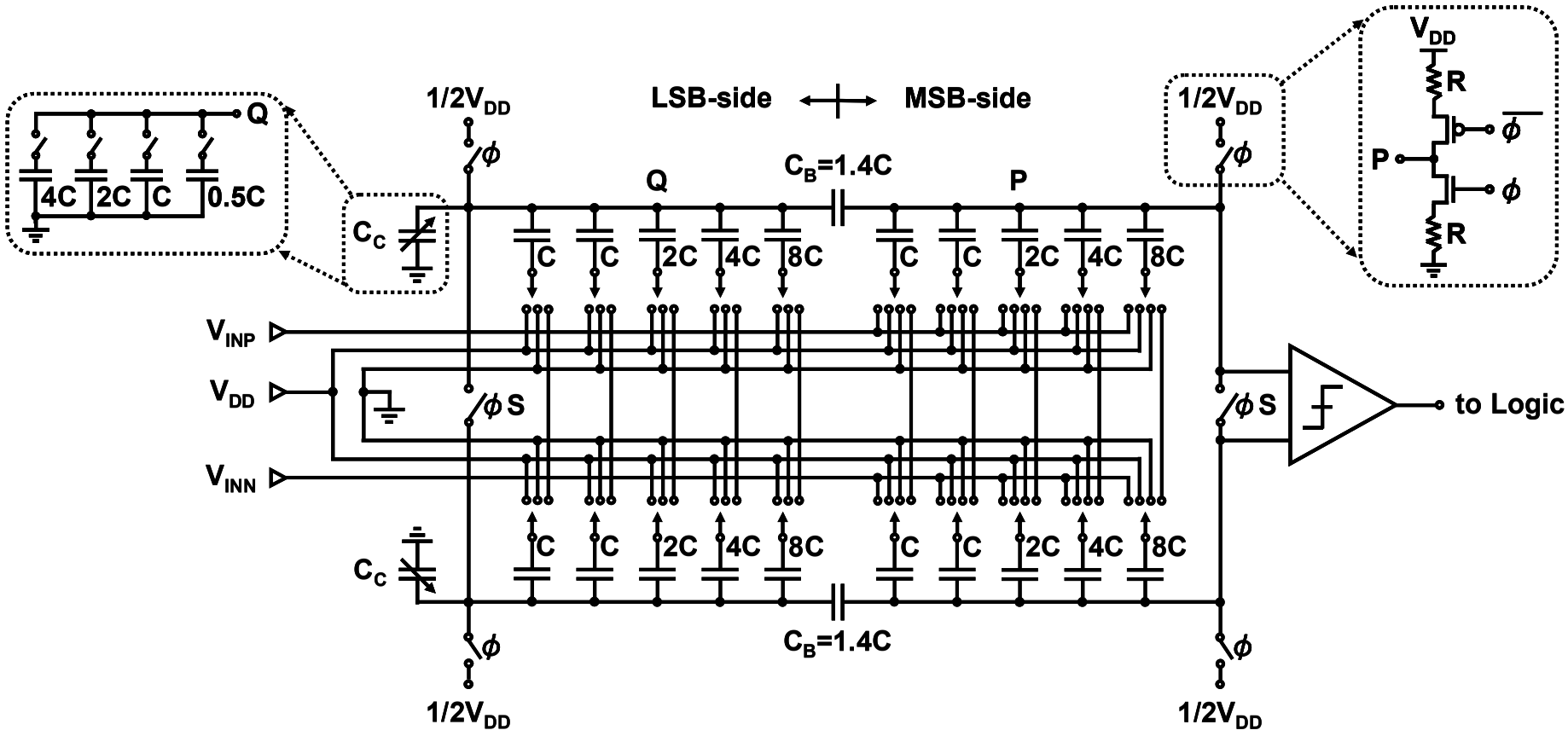
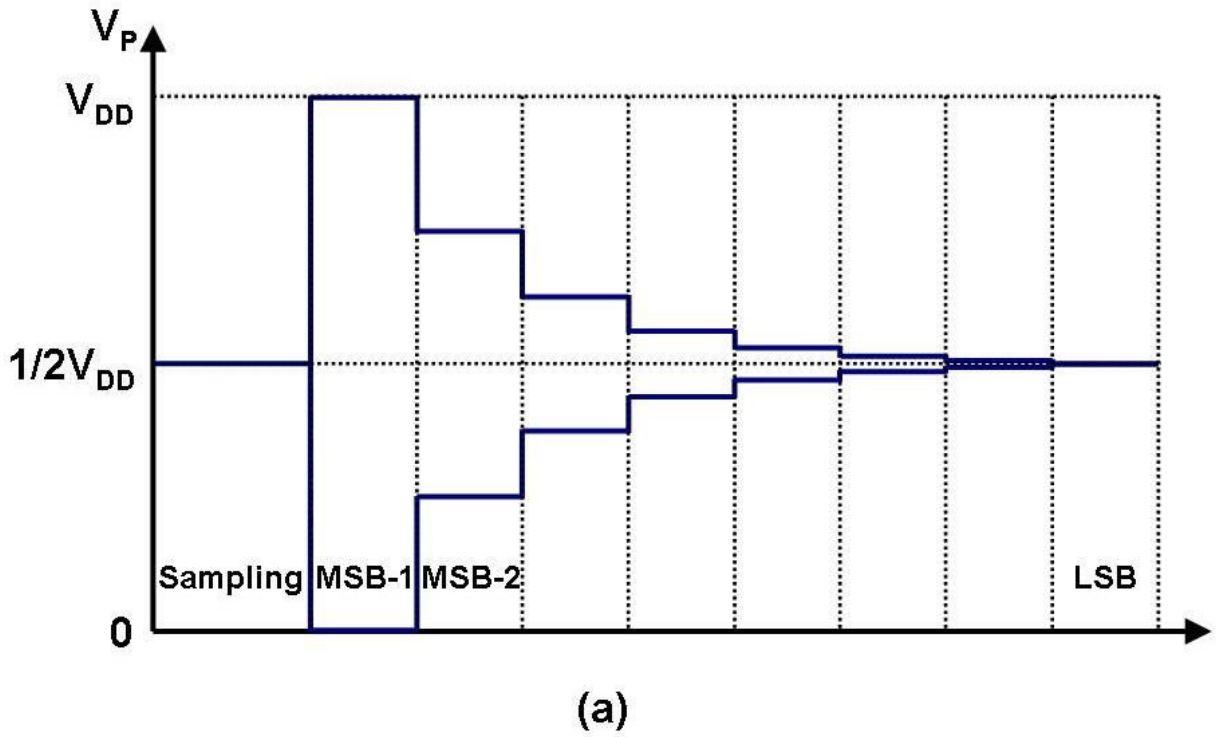


Figure 4.2 Implementation of the Tri-Level Split Capacitor DAC with Mismatch Calibration



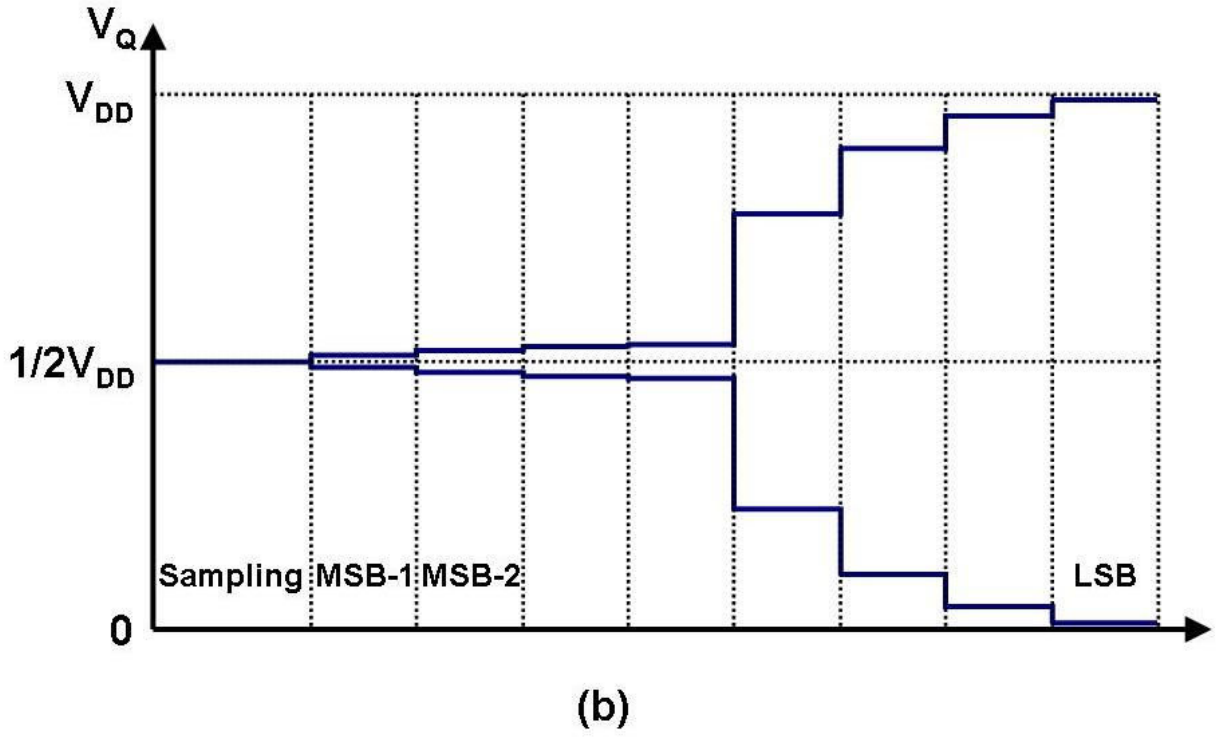


Figure 4.3 Largest Voltage Swing in Floating Nodes (a) Node *P* (b) Node *Q*.

The switches connecting the differential capacitor bottom plates have an operating point around $1/2V_{DD}$ when enabling charge sharing, and therefore the on-resistance is larger than switches connected to V_{DD} or ground. The settling time of the first bit estimate is affected by the on-resistance of the switches connecting the differential bottom plates. On the other hand, the settling time also depends on the input signal, as shown in Figure 4.4. Because all capacitors are switched from V_{IN} to $1/2V_{DD}$, the settling time is shorter for inputs close to $1/2V_{DD}$ and longer for inputs close to V_{DD} or ground. For the MSB decision, complete settling is most critical for the inputs near $1/2V_{DD}$, which exactly settle fastest. Therefore, the requirement for the switch on-resistance can be relieved.

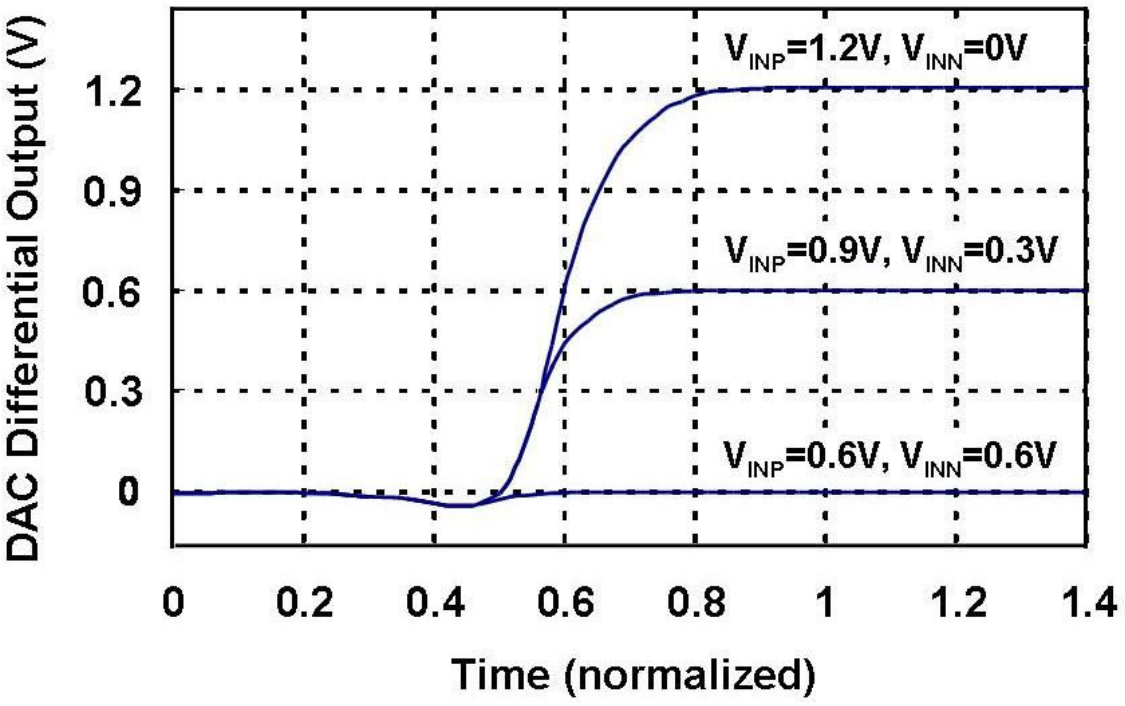


Figure 4.4 Output Settling of the MSB vs. Input Signal.

4.3 Comparator Design

For a 100-MS/s 9-bit SAR ADC, conventionally at least 1-GHz synchronous clock is required. Synthesizing such a high-frequency clock plus the clock distribution network would likely consume more power than the ADC itself. From a speed perspective, every clock cycle has to tolerate the worst case comparison time, depending on the minimum resolvable input level. In addition, every clock cycle requires margin for the clock jitter which will either slow down the conversion speed or impose a stringent jitter requirement on the clock generator. Therefore, an asynchronous clock generation circuit is used in the comparator design, which is shown in Figure 4.5.

A dynamic comparator is used, which is based on the StrongArm design [4]. A differential input pair feeds currents into a cross-coupled CMOS regenerative pair. The cross-coupled pair provides a large gain and amplifies the differential input into near full logic levels. A reset switch in the input pair helps to reduce the comparator recovery time during the reset phase.

The comparator outputs are connected with an SR-latch to control the successive approximation logic and also with a complementary CMOS NAND gate to generate an internal asynchronous clock [2]. During the reset phase, the complementary outputs of the comparator are pulled up to the positive supply voltage and the NAND gate outputs a low voltage. During the regeneration phase, one of the comparator outputs is pulled down to the negative supply voltage or both of them drop together to a lower level when the input is sufficiently small. In either case, the NAND gate outputs a high voltage as a comparison ready signal. The output of the NAND gate is delayed and buffered to trigger the comparator itself. The duration of the reset phase is determined by the control logic delay and the DAC settling time while the regeneration phase is simply decided by the comparator regenerative time.

In this work no calibration for comparator offset is implemented. Since the same comparator is used for the internal comparisons, the comparator offset causes the global ADC offset rather than nonlinearities.

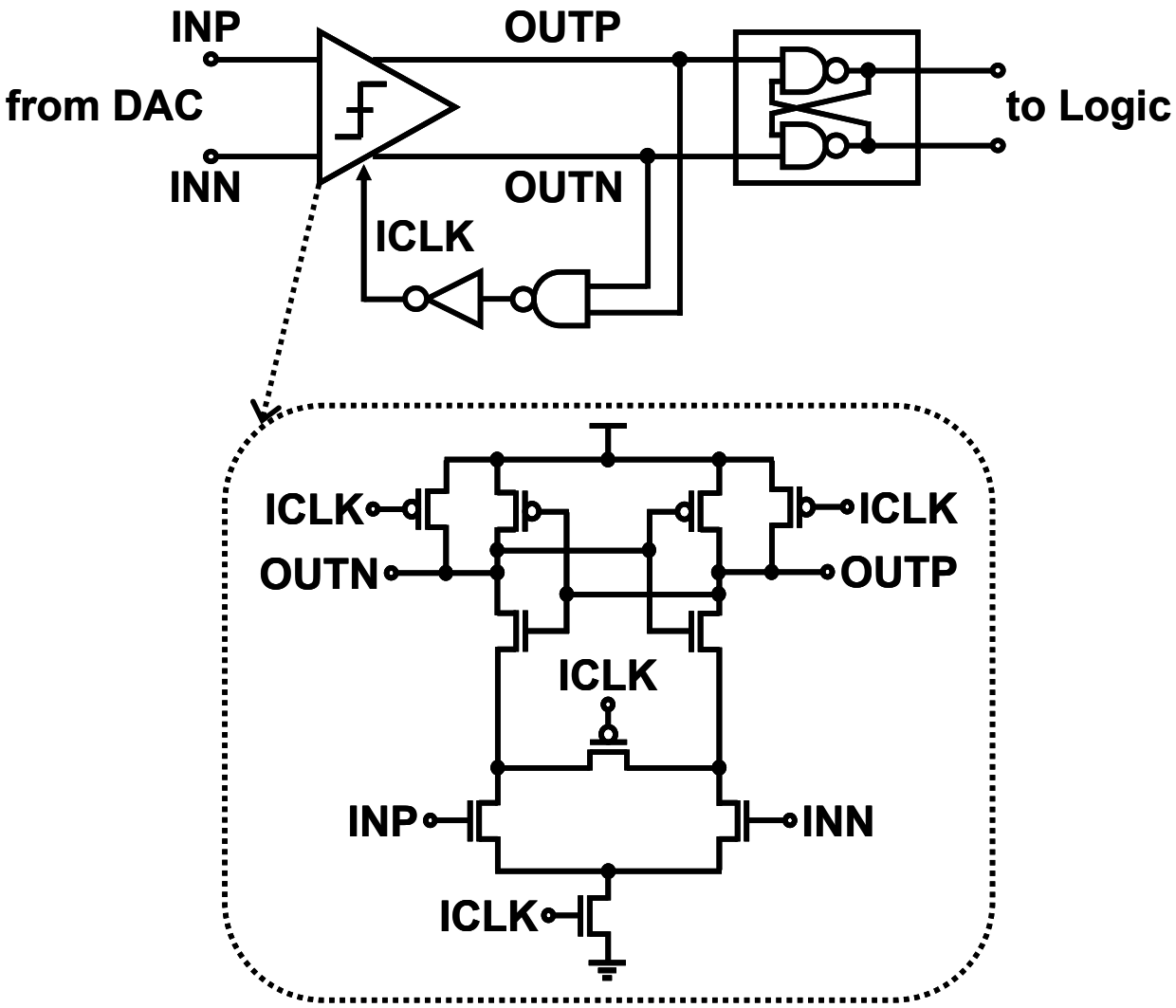


Figure 4.5 Comparator Schematic with Asynchronous Clock Generation.

4.4 SAR Control Logic Design

The SAR control logic consists of two functional parts, a sequencer and a code register [5]. As shown in Figure 4.6, the sequencer is a shifter register SR_1~SR_N which defines the operable period of each flip-flop SW_1~SW_N in the code register. The outputs of the code register S_1~S_N control the switch array in the DAC. In the conventional SAR control logic, one by one from SW_N to SW_1, each flip-flop in the code register is first set to "1" and then reset to "0" if its corresponding weight contribution is too large [6]. The operation of the conventional code register is determined by the conventional DAC design in which each bit estimate is done by setting that bit to "1" and all lower-weight bits to "0".

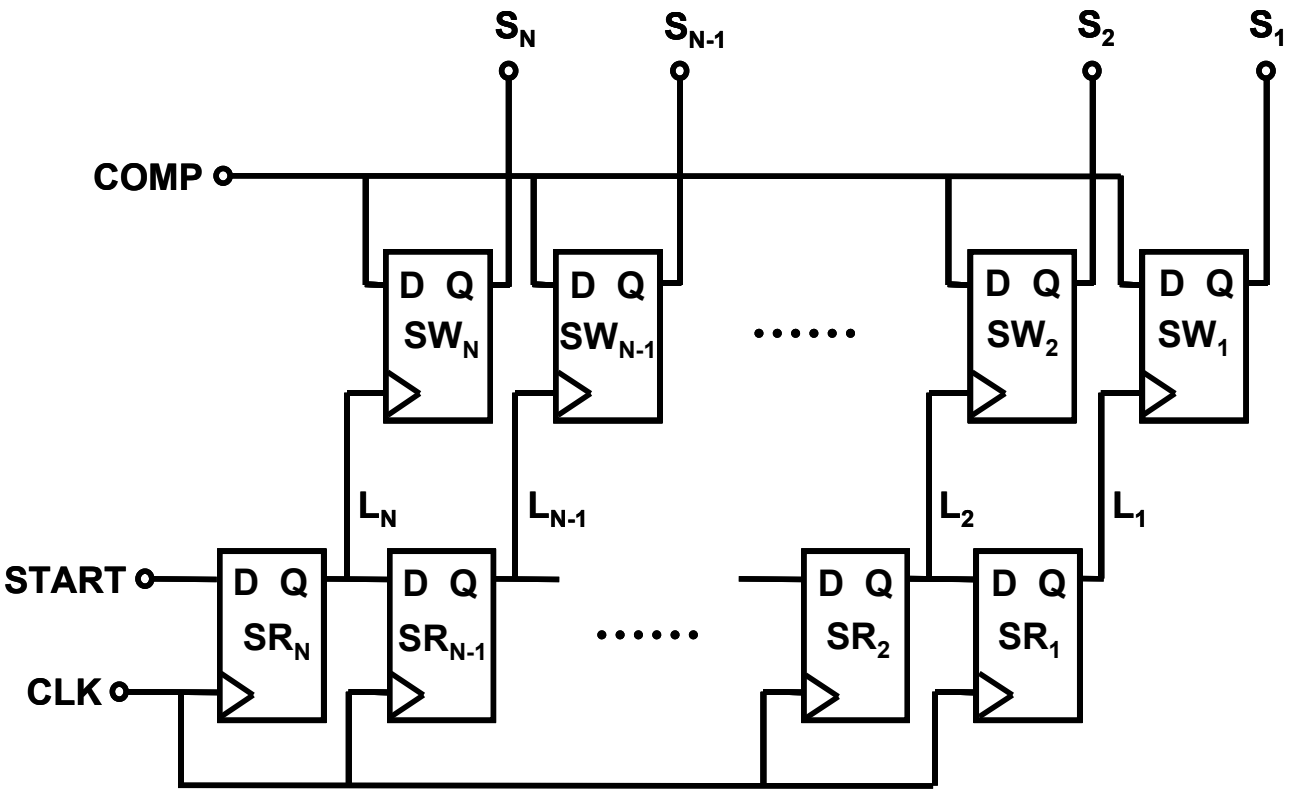


Figure 4.6 SAR Control Logic Implementation.

In this work, thanks to the tri-level charge redistribution technique, the successive approximation logic is simplified. In the tri-level DAC, all bits are initially set to "1/2" ($1/2V_{DD}$) for each conversion cycle. The output of the comparator determines whether the highest bit should be set to "1" or "0". At the time the highest bit is fixed, all remaining bits keep set to "1/2" and the estimate of the next bit is also completed. Then the comparator determines the second highest bit and the same simple procedure repeats. Therefore the code register flip-flops only need to be set and fixed, which makes the design much easier. The same flip-flops as in the sequencer can be used in the code register to drive the switches connecting the differential bottom plates in the DAC. The code register is reset at the beginning of each conversion cycle to turn on all the switches and enable bottom-plate charge sharing. One by one, flip-flops in the code register are set to turn off the corresponding switch before each bit in the DAC is set to "1" or "0". By simply comparing the number of logic gates, the power consumption of the SAR logic in the tri-level ADC is about 30% lower than that in the conventional design.

Both the shift register and the code register in the SAR logic implement dynamic C^2MOS flip-flops (Figure 4.7), which have a small number of transistors and operate at high speed and low power. However, dynamic flip-flops store state on parasitic capacitors and therefore only hold the state for a period of time. At low sampling rate, the ADC performance will be degraded by charge leakage.

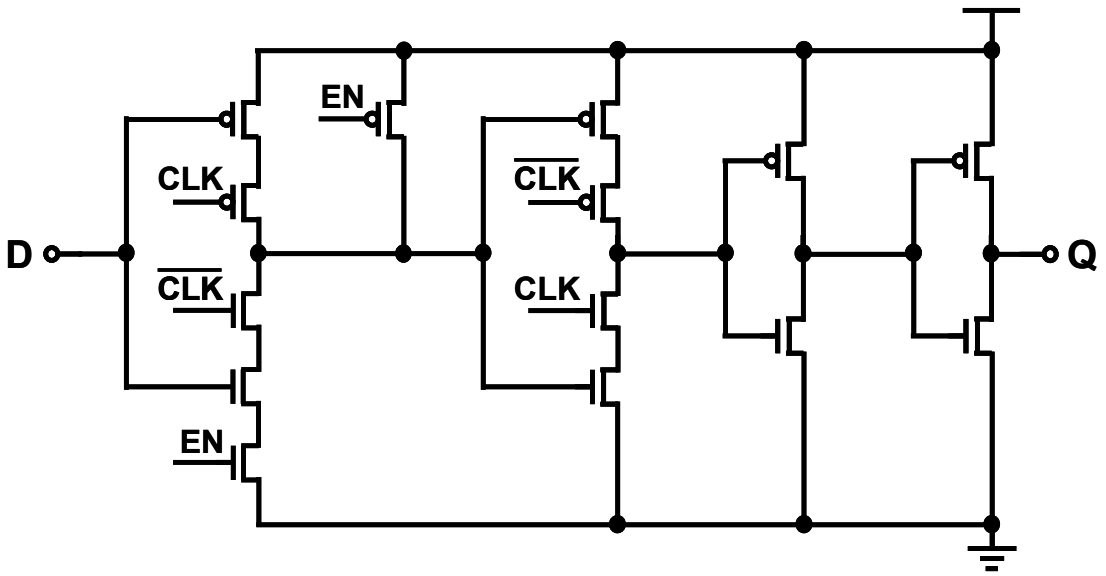


Figure 4.7 Dynamic C^2MOS Shifter Register.

4.5 Measurement Results

The SAR ADC chip has been fabricated in a standard 65 nm 1P7M CMOS process. Figure 8 shows the micrograph of the test chip. The active area of the ADC is 0.1 mm × 0.12 mm. The test setup for measuring the ADC is shown Figure 4.9, which contains an analog signal generator, a pulse pattern generator, a logic analyzer, and a PC. The sine-wave signal is passed through a low pass filter for good linearity. The ADC chip is packaged and tested using an evaluation board. In the following measurements, the supply voltage is 1.2 V unless noticed otherwise.

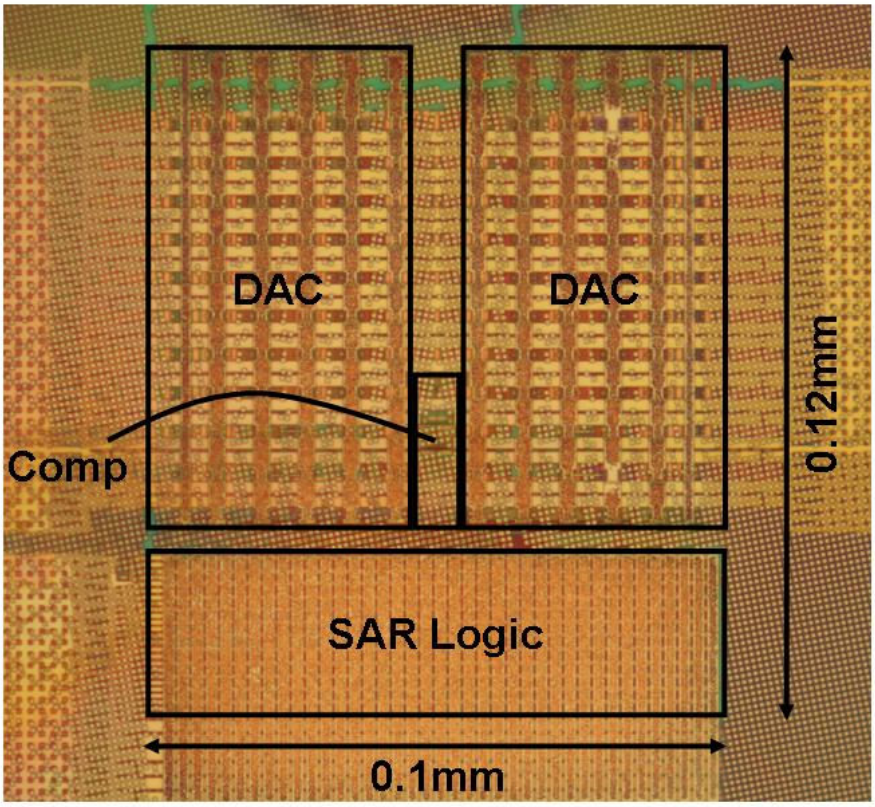
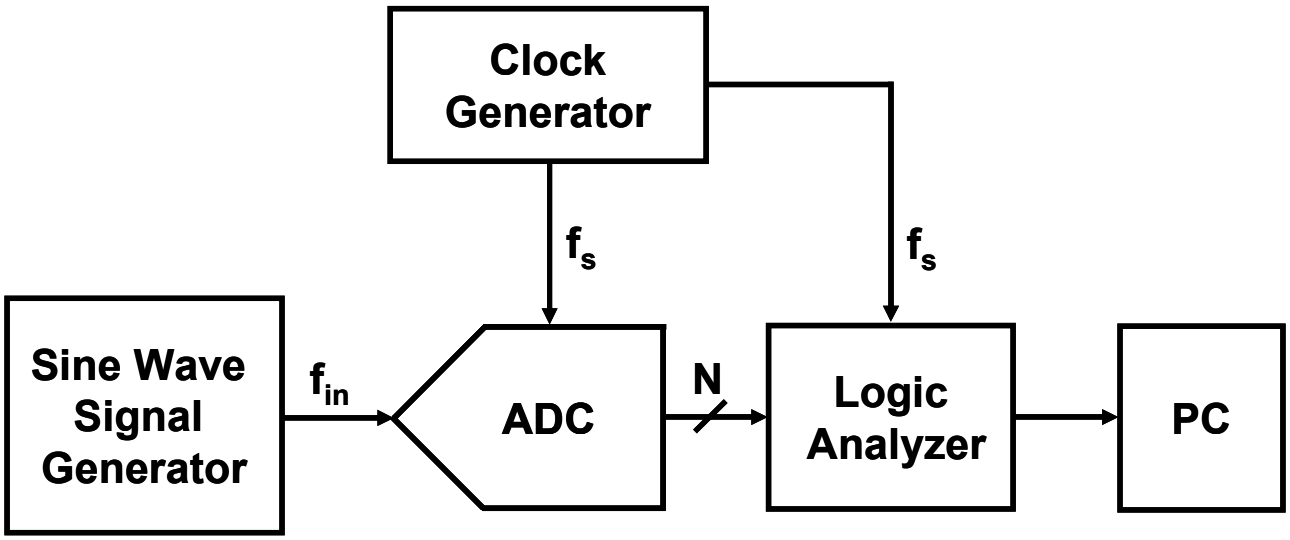


Figure 4.8 Chip Micrograph.



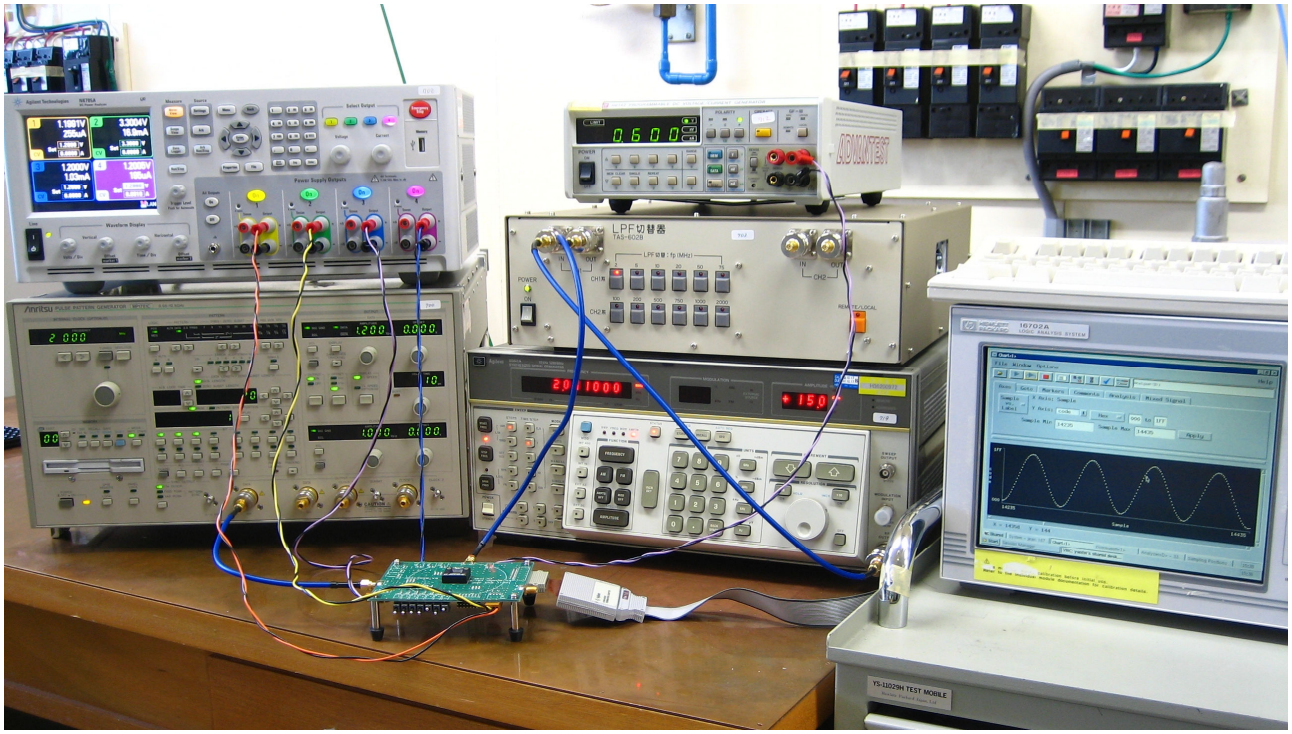


Figure 4.9 Test Setup for Measuring ADC.

The static performance testing method has been introduced in Chapter 2. Figure 4.10 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL). After the DAC mismatch calibration is performed, the DNL is within +0.3/-0.2 LSB and the INL is within +0.4/-0.4 LSB at a sampling rate of 100 MS/s. Since the minimum step of the calibration is 0.5 LSB, small periodical peaks in the DNL and INL can still be seen, indicating the implementation of split capacitor arrays.

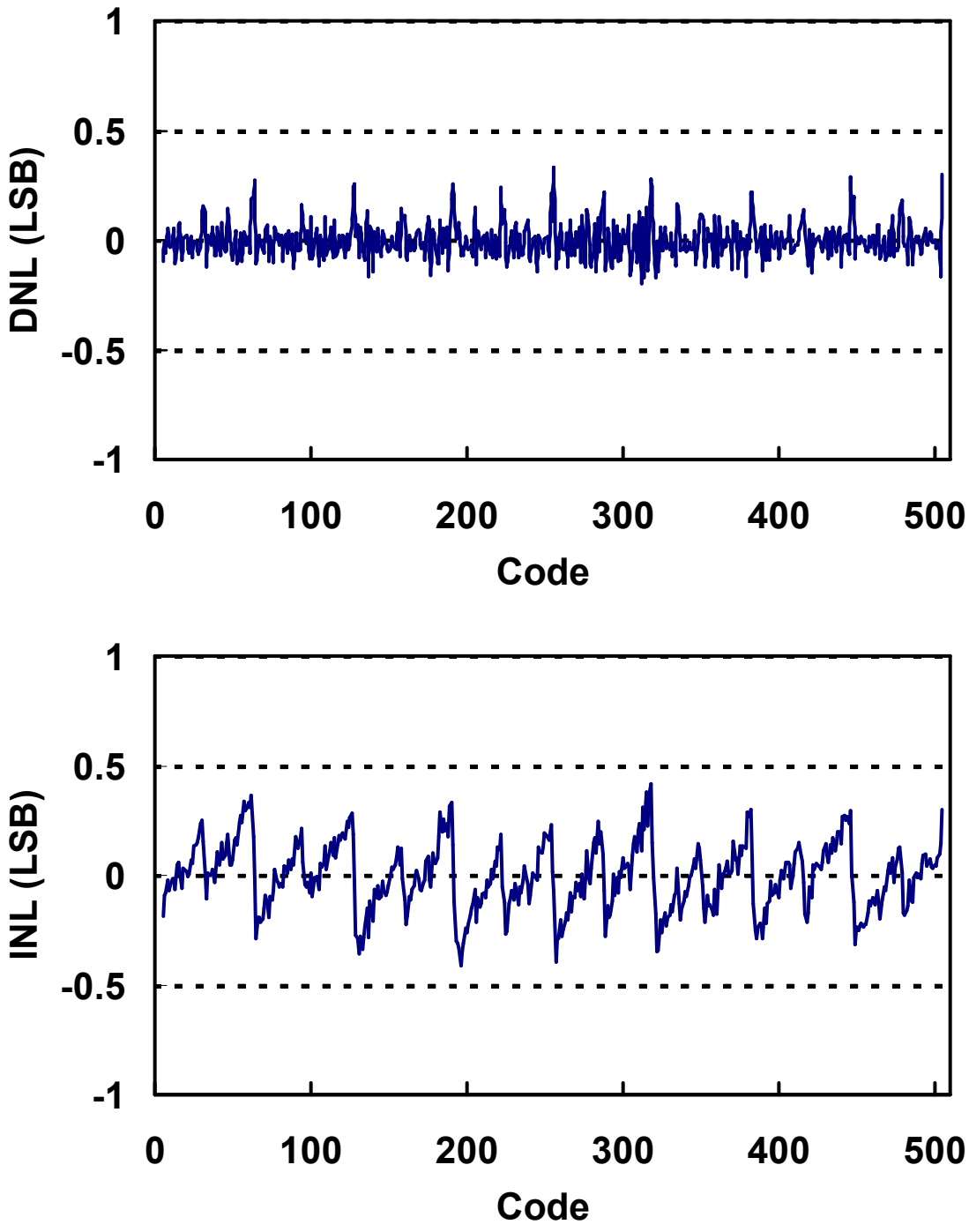


Figure 4.10 Measured DNL and INL.

In addition to the static specifications, dynamic performance characteristics such as signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), effective number of bits (ENOB), spurious-free dynamic range (SFDR), and etc. are usually used to specify sampling ADCs. In this work, the dynamic performance testing is based on Fourier transform. The Fourier transform allows a time domain signal to be converted into its equivalent representation in the frequency domain. For example, M samples of the ADC output are input into the Fast Fourier Transform (FFT). The M-point output spectrum is shown as in Figure 4.11. The resolution of the FFT is determined by M, and the frequency bin width is f_s/M. The larger M, the more frequency resolution is. Figure 4.11 also shows the relationship between the average noise floor of the FFT and the broadband quantization noise level. Quantization noise is approximately uniformly distributed over the bandwidth dc to f_s /2. Each time M is doubled, the average noise in the $\Delta f = f_s/M$ frequency bin decreases by 3 dB [7].

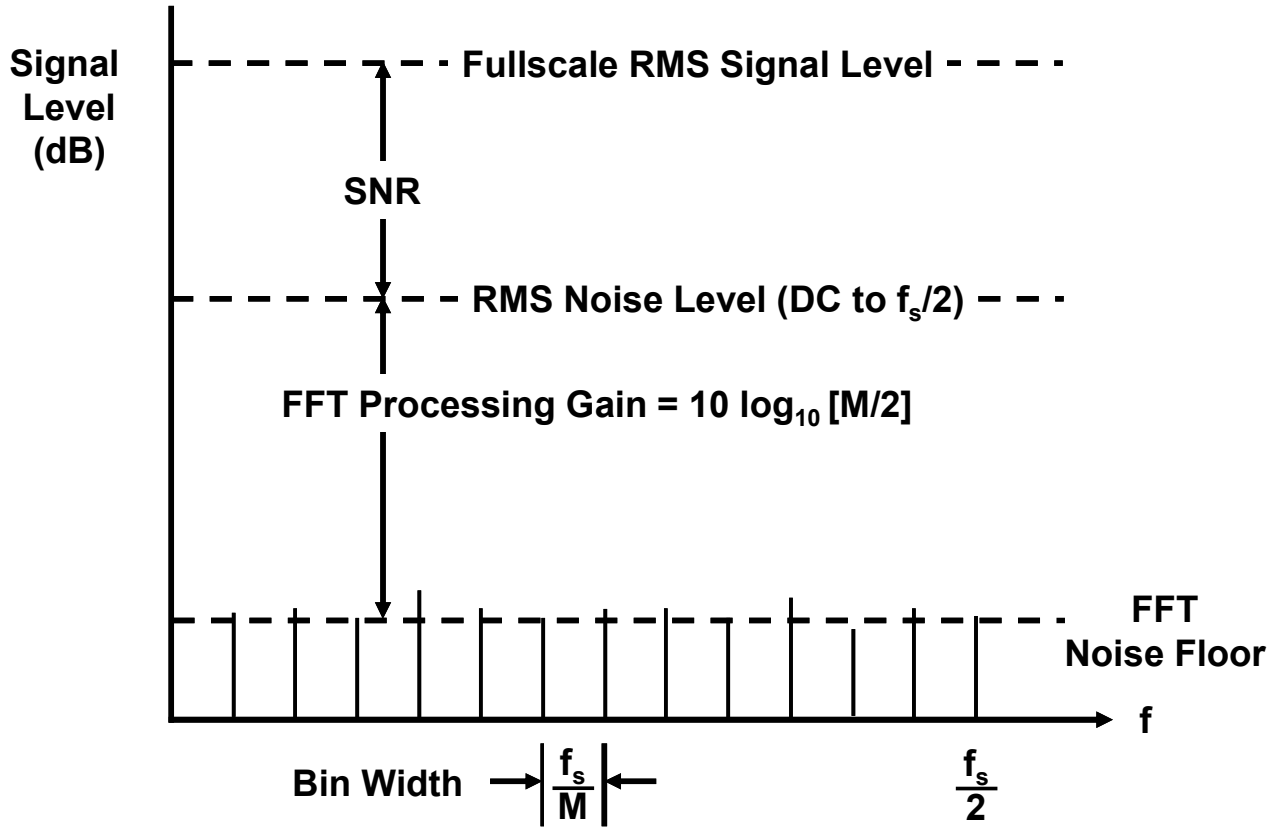


Figure 4.11 FFT Output Shows Effects of Processing Gain.

The measured FFT spectrum of the ADC at a sampling rate of 100 MS/s is shown in Figure 4.12. The input signal is near Nyquist frequency, 47.011 MHz. The number of samples *M* is chosen to be 16384 and the FFT processing gain is 39 dB. Therefore the SNR can be easily calculated, which is equal to 51.5 dB. Since harmonic distortion components are excluded from the SNR, it is better to use the SNDR, which includes all the components making up noise and distortion, as an indication of the overall dynamic performance of the ADC as a function of input frequency. Here the SNDR is measured to be 51 dB, which is very close to SNR. This means the dynamic performance at near Nyquist frequency is limited by distortion. The SNDR is often converted to the ENOB using the relationship for the theoretical SNR of an ideal N-bit ADC:

$$SNR = 6.02N + 1.76dB \tag{4.1}$$

The equation is solved for *N*, and the value of SNDR is substituted for SNR:

$$ENOB = \frac{SNDR - 1.76dB}{6.02} \tag{4.2}$$

The SFDR is defined as the ratio of the RMS signal amplitude to the RMS value of the peak spurious spectral content measured over the bandwidth of interest. In this case, the peak spectral spur is determined by the second harmonics of the fundamental, corresponding to the SFDR of 65.2 dB. SFDR is generally much greater than the theoretical SNR in Equation (4.1). For example, the theoretical SNR for 9-bit ADCs is 56 dB. This is because there is a fundamental distinction between noise and distortion measurements. The processing gain of the FFT allows frequency spurs well below the noise floor to be observed. Adding extra resolution to an ADC may serve to increase its SNR but may or may not increase its SFDR.

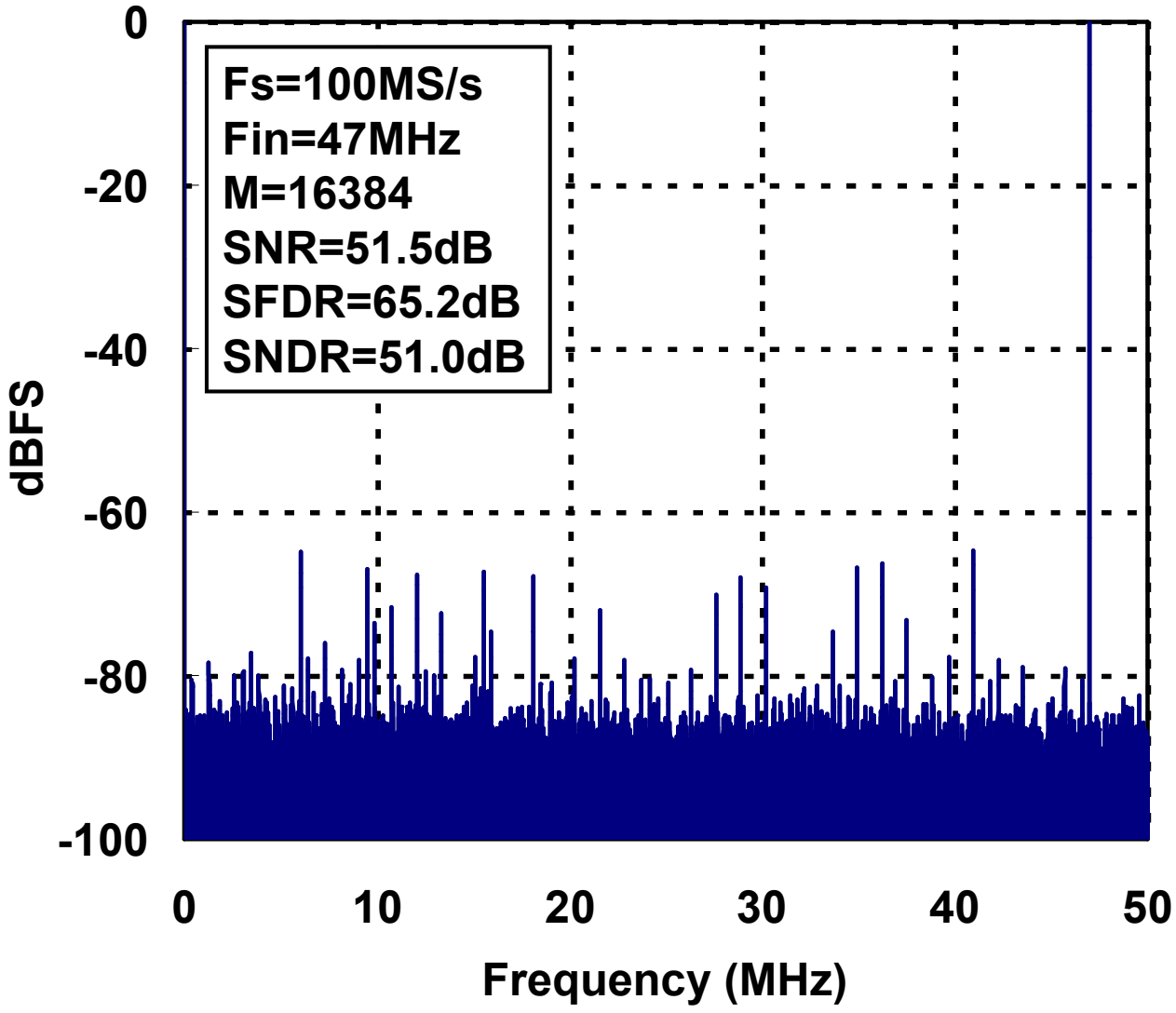


Figure 4.12 Measured Output FFT Spectrum.

Figure 4.13 depicts the measured SNDR and SFDR versus sampling frequency with a 2.011 MHz sinusoidal input to test the maximum operation speed of the ADC. The result shows that the ADC is able to operate at a sampling frequency as high as 100 MHz without SNDR degradation. Further increasing the sampling frequency will cause incomplete input sampling and incomplete LSB resolving and thus degrade the ADC performance.

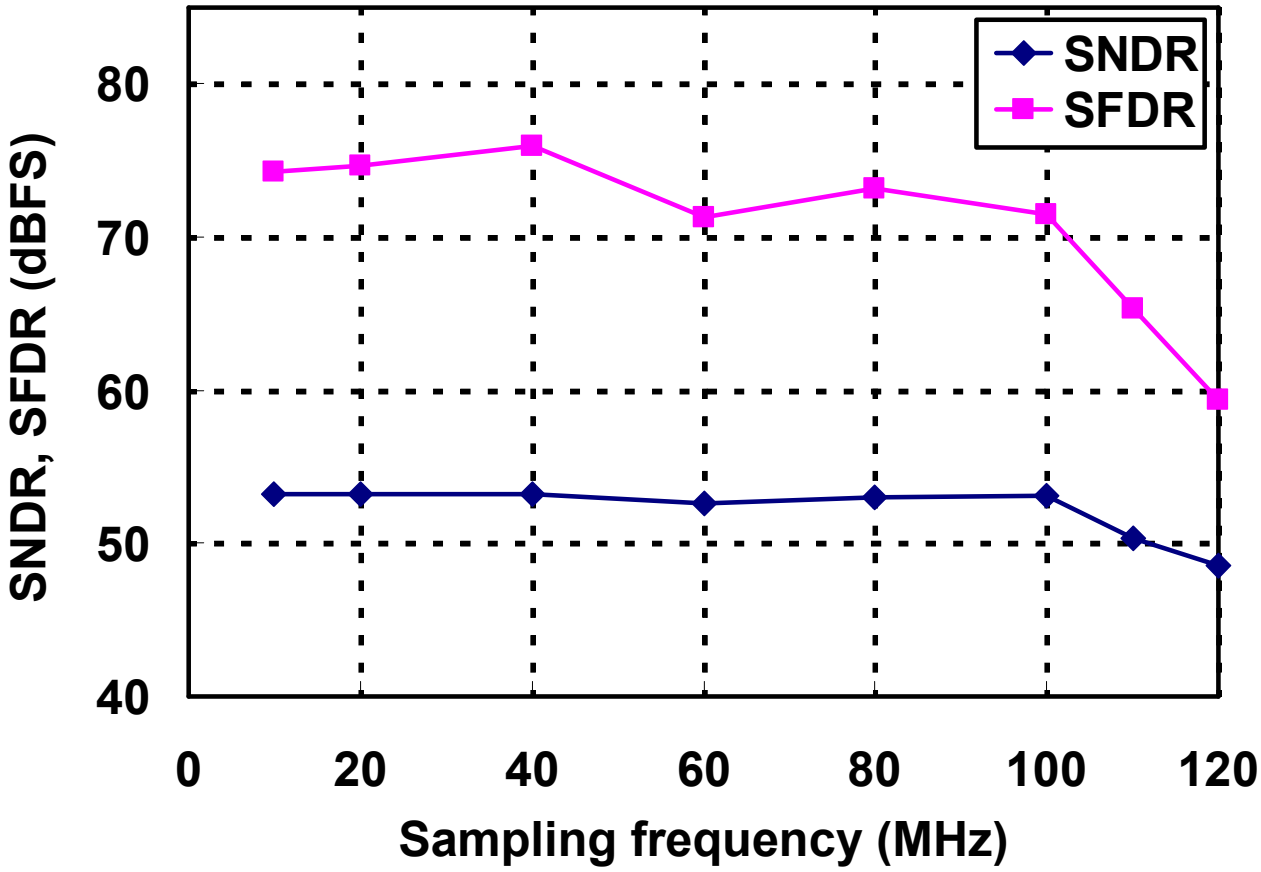


Figure 4.13 Measured SNDR and SFDR vs. Sampling Frequency.

Figure 4.14 shows the measured SNDR and SFDR of the ADC at 100 MS/s with respect to the input amplitude. The result proves that the ADC indeed has a rail-to-rail input range. With a 10% duty-cycle sampling clock, the ADC achieves a peak SNDR of 53.1 dB and SFDR of 73.2 dB, corresponding to an ENOB of 8.53. The nonlinearity in the SFDR is due to the differential nonlinearities in the ADC transfer function, corresponding to those shown in Figure 4.10.

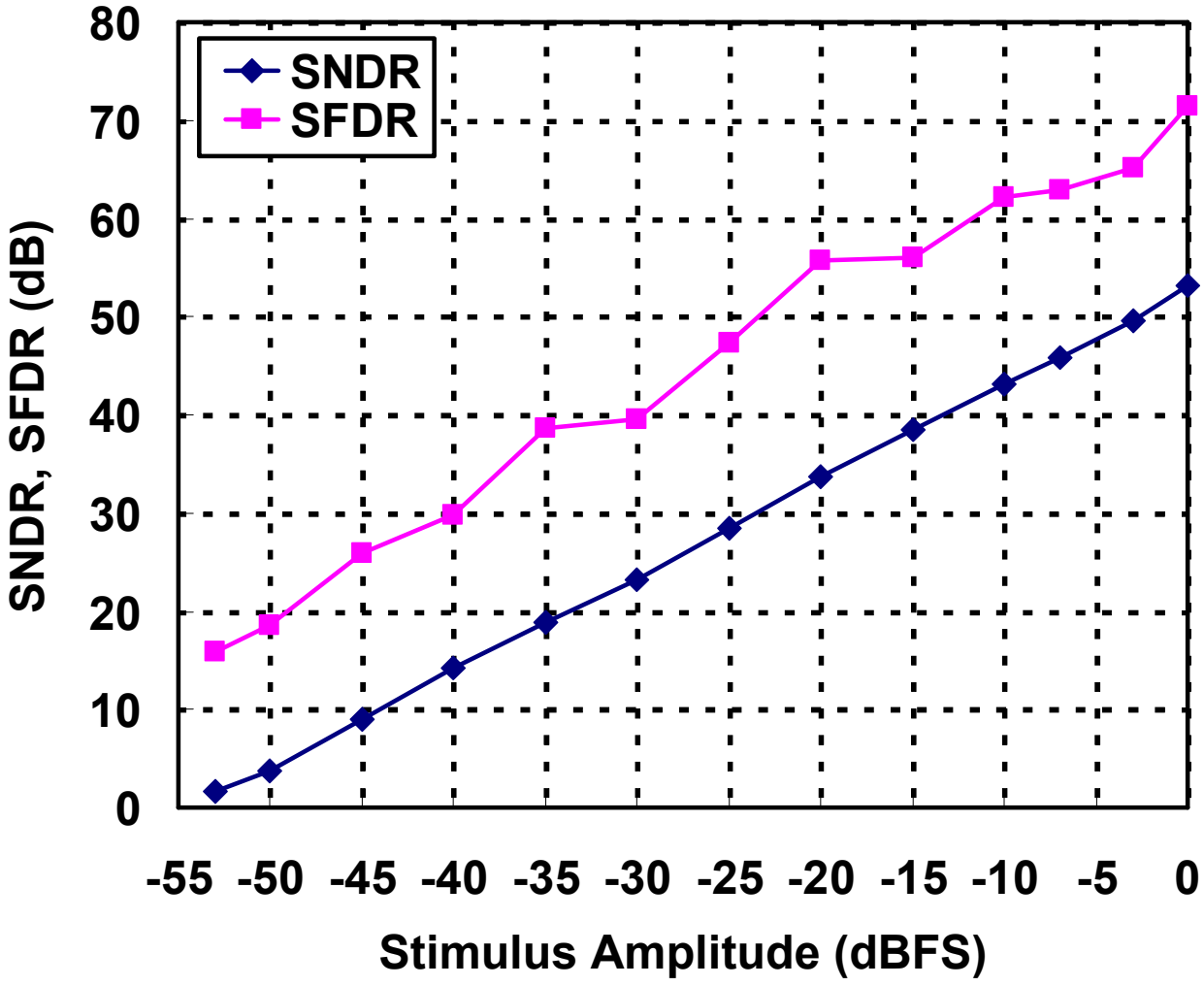


Figure 4.14 Measured SNDR and SFDR vs. Input Amplitude.

The analog bandwidth of an ADC is that frequency at which the spectral output of the fundamental swept frequency, as determined by the FFT analysis, is reduced by 3 dB. Figure 4.15 plots the measured SNDR and SFDR versus input frequency at the sampling rate of 100 MS/s. The SNDR does not degrade by 3 dB even with the input frequency close to 50 MHz, which means the ADC achieves an effective resolution bandwidth (ERBW) no less than its Nyquist bandwidth.

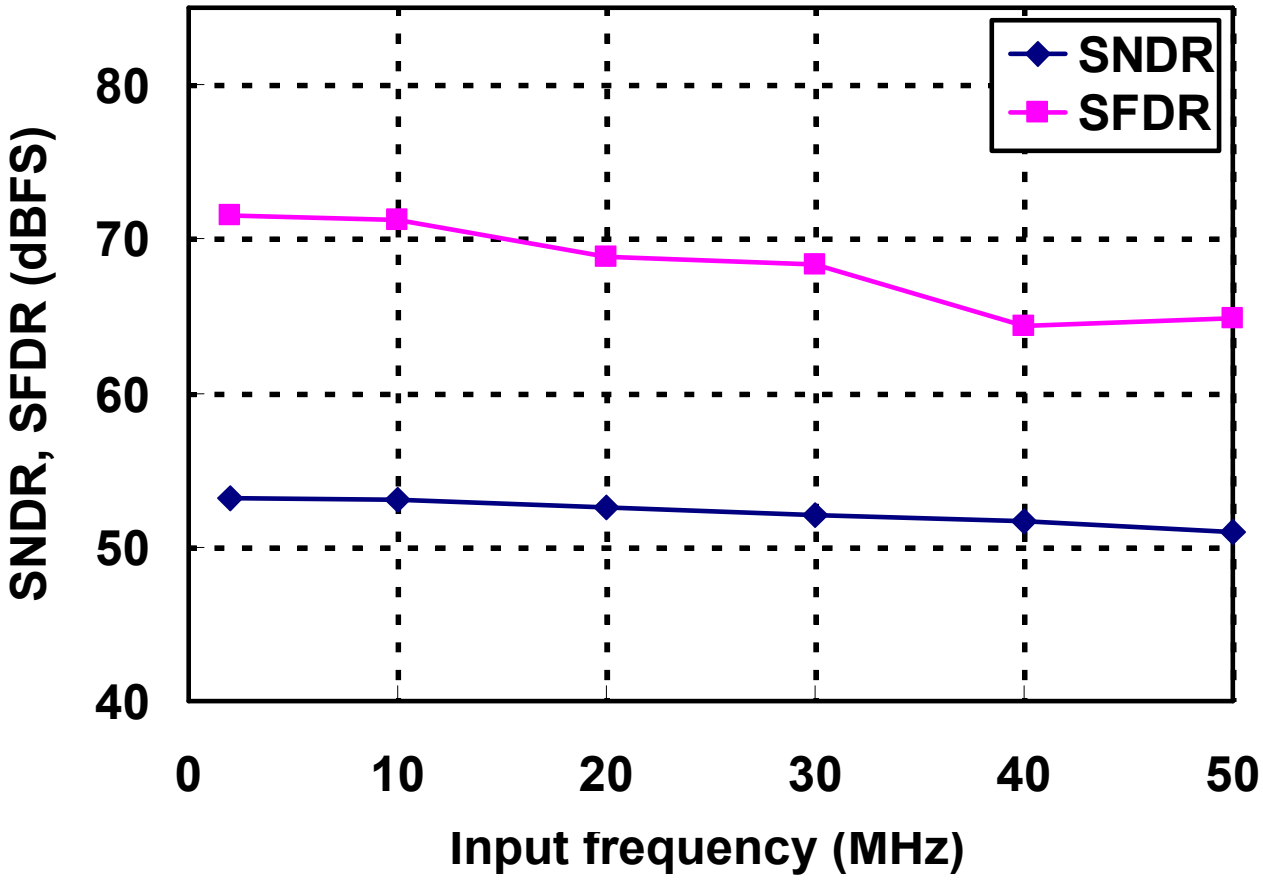


Figure 4.15 Measured SNDR and SFDR vs. Input Frequency.

The ADC totally consumes 1.46 mW at 100 MS/s sampling rate from the 1.2 V supply voltage. In the measurement, the analog signal generator's output is directly connected to the ADC input without using any input buffer. Therefore, the power which would be consumed by the buffers driving the ADC is not included in the overall power dissipation. The average power of analog circuits including the comparator and DAC is 0.26 mW and digital control logic circuits is 1.2 mW. The power can be even lower depending on applications. Figure 4.16 displays the measured power consumption versus the sampling frequency. When the sampling frequency is lower than 10 MHz, the digital power no more decreases proportionally, which is due to the charge leakage in the dynamic shift register flip-flops.

In this ADC, the digital part consumes more than 80% of the total power. Fortunately, with CMOS technology scaling to the next generation (45 nm), the digital power is expected to be reduced to 70% with constant supply voltage. With constant electric field (70% voltage scaling), the power consumption can be reduced to 34%.

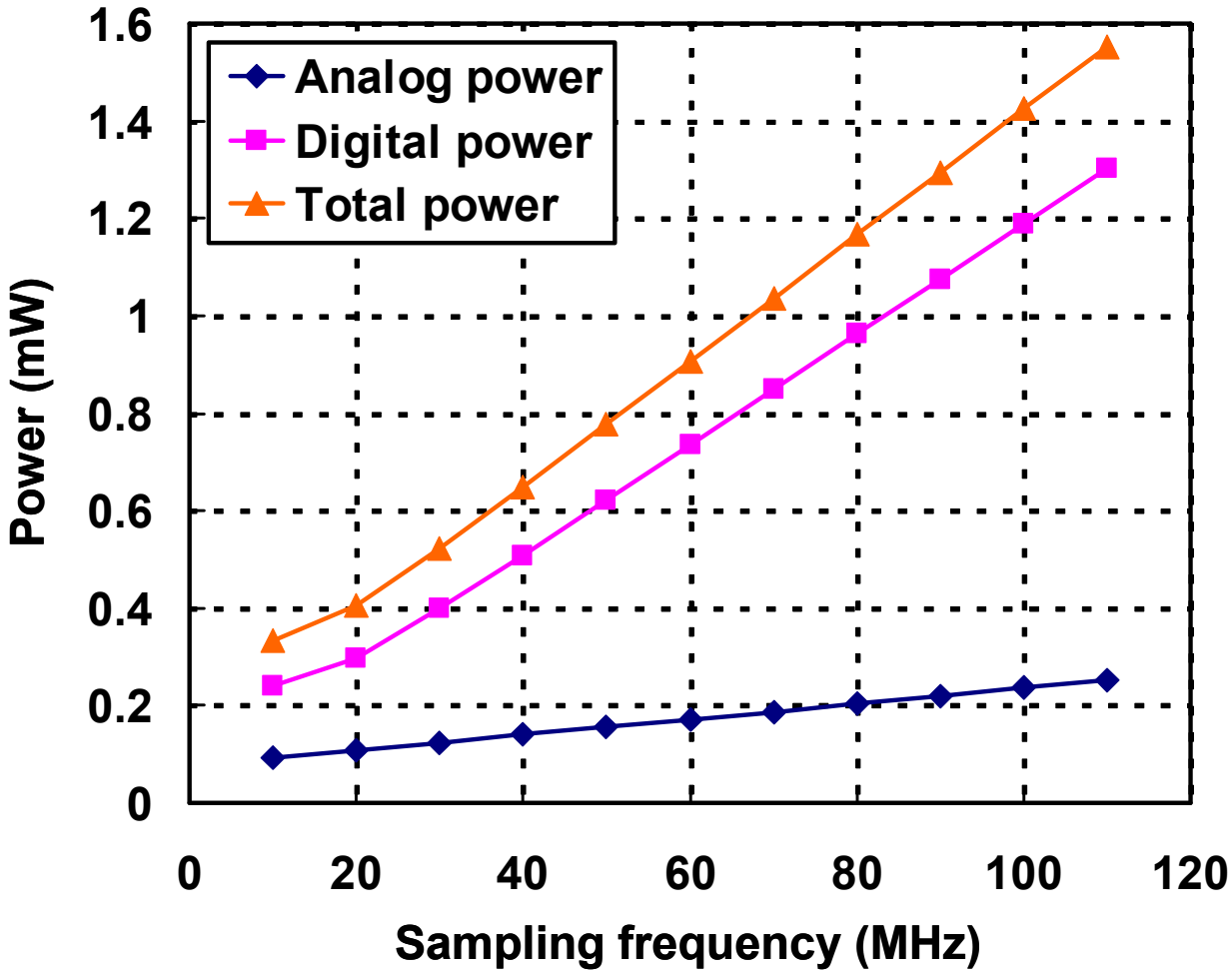


Figure 4.16 Measured Power Consumption vs. Sampling Frequency.

Reducing the supply voltage to 1.1 V, the ADC still achieves a peak SNDR of 52.3 dB at 100 MS/s, with the total power consumption reduced to 1.16 mW. However, SFDR is degraded, as shown in Figure 4.17. Because no bootstrapped sampling switch is implemented in this work, the supply voltage affects the sampling speed directly. The ADC is not able to operate at full speed with supply voltages lower than 1 V.

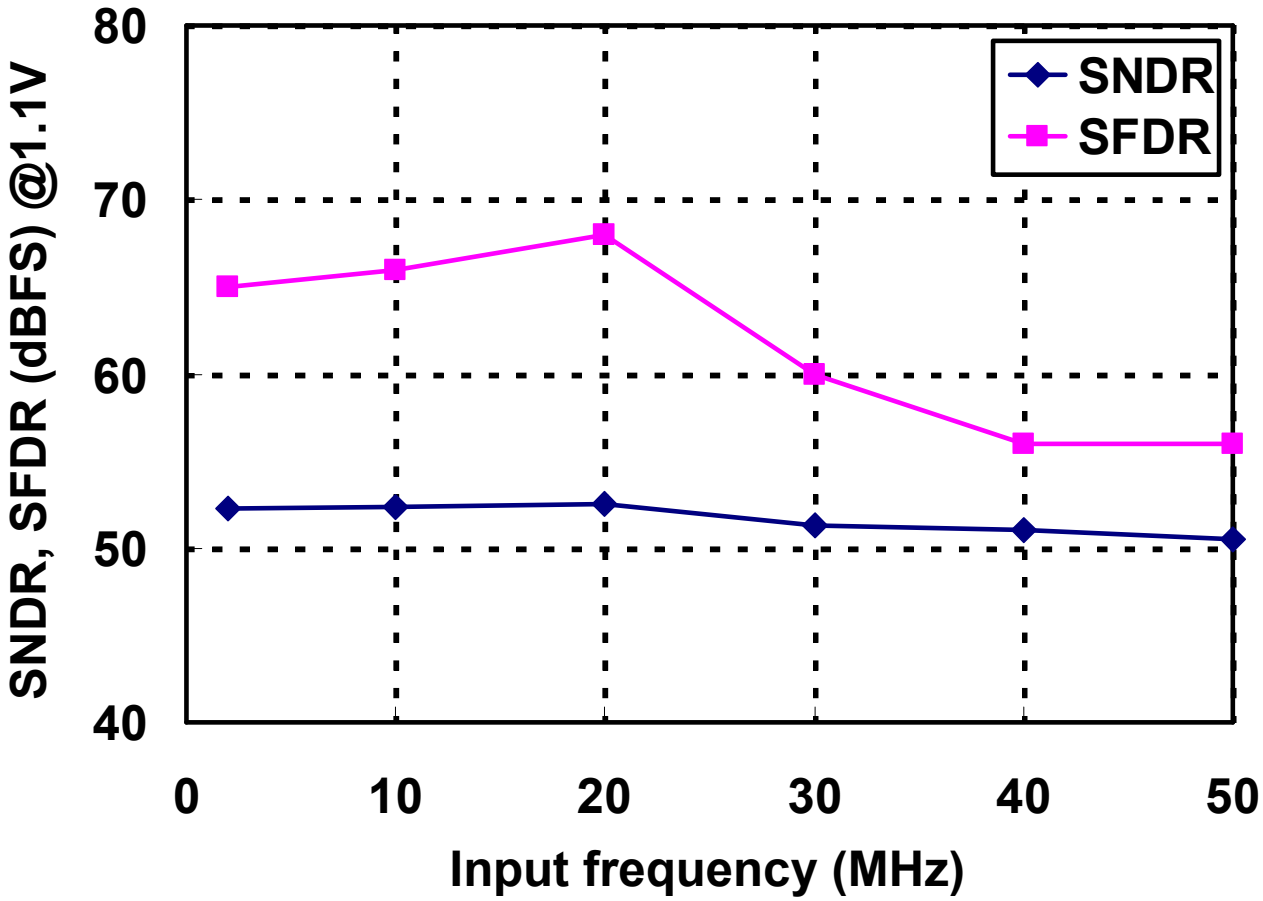


Figure 4.17 Measured SNDR and SFDR at 1.1 V-Supply vs. Input Frequency.

Table 4.1 summarizes the ADC performance.

A widely used definition of ADC figure of merit (FOM) is shown in Equation (4.3).

$$FOM = \frac{Power}{2^{ENOB} \cdot f_s} \tag{4.3}$$

This FOM indicates the energy required to complete an effective conversion step of an ADC. With this definition, the proposed SAR ADC achieves 39 fJ/conversion-step at 1.2 V-supply and 35 fJ/conversion-step at 1.1 V-supply.

Table 4.1 Performance Summary.

Power supply voltage (V)	1.2
Input range (V)	0 ~ 1.2
Input capacitance (fF)	180
Sampling rate (MS/s)	100
Resolution (bit)	9
Analog power (mW)	0.26
Digital power (mW)	1.2
Total power (mW)	1.46
DNL (LSB)	+0.3 / -0.2
INL (LSB)	+0.4 / -0.4
ENOB	8.53 at fin=10 MHz 8.17 at fin=50 MHz
Area (mm^2)	0.1 × 0.12
Technology (nm)	65 (1P7M CMOS with MIM capacitor)

However, area is also a critical parameter of any embedded ADC and should be included in the expression. Therefore, we define a new figure of merit (FOM*) as follows:

$$FOM* = \frac{Power \cdot Area}{2^{ENOB} \cdot f_s} \tag{4.4}$$

With the new figure of merit definition, both energy and area efficiency of ADC designs can be compared. Table 4.2 shows the comparison with recently reported medium resolution and medium sampling rate ADCs, including both pipelined and SAR architectures. The proposed ADC consumes the least energy and area for an effective conversion step.

Table 4.2 Comparison with Published Work.

Architecture	Technology (nm)	Area (mm^2)	ENOB	Fs (MS/s)	Power (mW)	FOM (fJ/conv.)	FOM* (fJ· mm^2/conv.)	Ref.
Pipelined	65	0.07	9.5	100	4.5	62	4.34	[8]
Pipelined	90	0.3	10	50	4.5	88	26.4	[9]
Pipelined	90	0.123	7.9	50	1.44	119	14.63	[10]
SAR	90	0.09	8.56	40	0.82	54	4.86	[11]
SAR	130	0.075	8.48	50	0.92	52	3.9	[12]
SAR	90	0.08	7.8	50	0.725	65	5.2	[13]
SAR	65	0.012	8.53	100	1.46	39	0.468	This work

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Chapter 5 Summary

5.1 Dissertation Summary

In battery-powered mixed-signal applications including data communication and image processing systems, high performance ADCs are in great demand. This work aims to design medium resolution and moderate sampling rate ADCs with very low power consumption and small footprint. Energy and area savings are realized in several aspects. In architecture selection, charge redistribution based SAR architecture shows the highest power efficiency, benefiting from the structure containing only one active analog component. In circuit design, each of ADC building blocks is simplified and optimized to reduce power consumption and area. The split CDAC with mismatch calibration is used to reduce input load capacitance and area without degrading the linearity performance. The tri-level charge redistribution scheme is proposed to reduce the CDAC switching energy and improve the settling speed. The tri-level method also helps simplifying the SAR control logic circuits by eliminating the need for set-and-reset function. To avoid on-chip reference generation and therefore save power and cost, any reference voltage different from the supply voltage is removed. Asynchronous processing technique is used to eliminate power-hungry GHz clock generation and speed up the SAR algorithm as well. The ADC designs have been verified by both simulations and test-chip measurements.

Chapter 1 is an introduction of the overall study. For a comprehensive understanding of ADCs, the development of data converters in the past century is first studied. It is interesting to find that all the fundamental ADC architectures used today had been discovered and published in one form or another by the mid-1960s. Nevertheless, diverse market forces keep driving high growths of ADC researches. The modern ADC architectures are summarized in terms of key features and characteristics. Then the trend in ADC designs in the past decade and the motivation of this research are presented. Finally the organization of the dissertation is introduced.

Chapter 2 presents the split CDAC calibration scheme. Firstly the operation of charge redistribution based SAR is introduced. The conventional split capacitor arrays as solutions to reduce area and input load capacitance have several issues, which are analyzed on a case-by-case base. Then the principle of the

proposed calibration method is presented, followed by the circuit implementation details. The digital timing-control offset cancellation method is applied to the comparator to guarantee the split CDAC calibration. A test chip is implemented in standard CMOS process and the measurement results of the ADC static performance proves the linearity improvement after calibration.

Chapter 3 presents the tri-level charge redistribution scheme. The capacitor switching energy inefficiency and overshooting problems in output settling of the conventional charge redistribution method are first analyzed. Then how the tri-level charge redistribution method operates and saves switching energy is introduced. Differential capacitor bottom-plate charge-sharing technique is proposed to achieve the tri-level effects without actually implementing a third reference. Finally the improvement of the switching energy efficiency and settling speed are shown in simulation results.

Chapter 4 introduces a high performance successive approximation ADC design, which combined the split CDAC calibration and the tri-level charge redistribution techniques introduced in Chapter 2 and Chapter 3. Circuit design details of each building block are provided. The supply voltage and ground are chosen to charge and discharge the capacitors, leading to a rail-to-rail input range of the converter. The comparator is triggered by an internal asynchronous clock which is generated by detecting the outputs of the comparator itself. The SAR control logic is simplified to be only composed of shifter registers. The ADC test chip implemented in standard CMOS process is measured for both static and dynamic performances. Finally comparison with other state-of-the-art converters proves that this work is one of the best performing ADCs in the world.

Last but not least, based on the ADC designs in this work, a prospect of future research in terms of motivation and design challenges will be discussed in the next section.

5.2 Future Work

The ADC design in this work has achieved a combination of energy efficiency, area efficiency and high performance. With more and more countries and companies concerning about eco-friendly society (green society), green electronic devices such as green display, solar-powered cell phone, solar-powered camera and etc. will play a more important role in creating the green society. Low power will continue being the key word of LSI design including ADC design. Fortunately, semiconductor technology scaling will benefit the charge redistribution based SAR ADC in terms of power consumption.

This work has focused attention on designing high-performance ADCs for single channel applications. The features of small footprint, low power and small input load capacitance indicate that the ADC has potential to be used in multi-channel systems [1-3]. First introduced in 1980, time interleaving of ADC systems employs the concept of running M ADCs at a sample rate that is $1/M$ of the overall system sampling rate f_s [4]. As shown in Figure 5.1, each channel is clocked at a phase that enables the system as a whole to sample at equally spaced increments of time, creating the seamless image of a single ADC sampling at full speed. It is proved that the time-interleaved solution requires less die area than a comparable flash converter design. But space-saving was not the only benefit. Time interleaving of ADCs offers a conceptually simple method for multiplying the sample rate of existing high-performing ADCs.

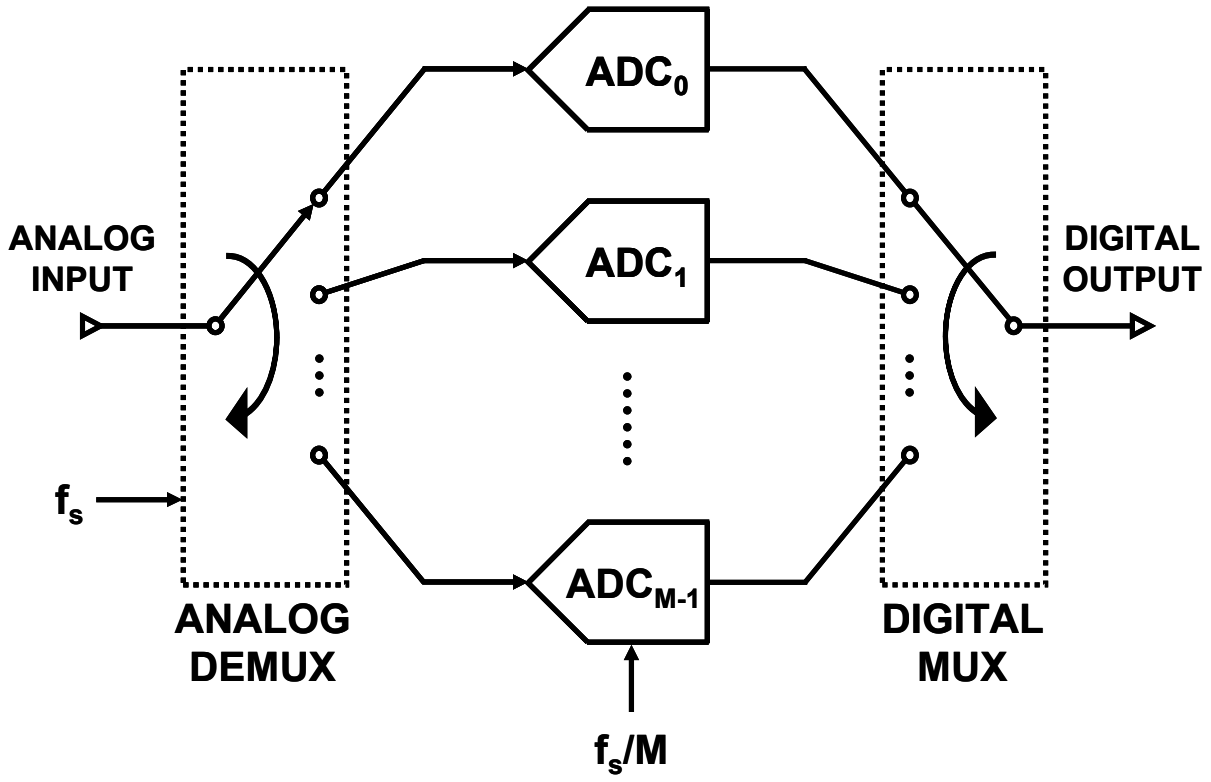

Figure 5.1 Time-Interleaved ADC System.

However, time-interleaving data converters is not an easy task, because even with perfectly linear components, gain/offset mismatches and timing errors can cause undesired spurs in the output spectrum. Pushing the operational limits of interleaved ADCs can be very attractive, but various limitations and considerations must be taken into account before turning this method into a successful experiment.

Firstly, applications that call for higher sampling speeds usually deal with higher-frequency input tones, so a data converter with an input bandwidth of half the sampling speed would not be suitable for interleaving. Fortunately, most high-speed data converters include track-and-hold amplifiers whose full-power and small-signal bandwidths are significantly higher than that called for by the Nyquist criteria.

Secondly, the channel-to-channel matching of offset and gain in separate ADCs is not trimmed, so gain and offset mismatches between ADCs are parameters of concern in a time-interleaved system [5]. If one ADC

shows an offset and the other a gain error, the digitized signal represents not only the original input signal but also an undesired error in the digital domain. An offset discrepancy causes a signal phase shift in the digitized signal, and gain mismatches show up as differences in signal amplitude. For interleaving designs, ADCs should be designed with integrated gain and offset correction or include external circuitry that allows correcting these mismatches.

Thirdly, INL is described as the deviation of the actual transfer function from a straight line, either in LSBs or in percent of full-scale range. INL errors of ±1LSB are quite common for individual ADCs, but in an interleaving system such errors can easily double, causing output-code errors that resemble the offset and gain problems discussed above. The appearance of nonlinearity introduces distortion into the system, which degrades dynamic parameters such as SNDR and ENOB.

Last but not least, the signal used as a system clock should have the lowest possible phase noise. Introducing a D-type flip-flop in a divide-by-two configuration reduces the otherwise stringent requirement for a precise 50% duty cycle. A clock circuit commensurate with the signal source's frequency range, amplitude, and slew rate should be selected. A low slew rate on the digitized signal relaxes the jitter requirement on the clock. If this slew rate is large, the clock jitter must be minimized.

Most of the errors discussed above can be overcome using calibration procedures in the time domain, careful circuit design and layout, a suitable selection of data converters, and digital post-processing. This approach is complex and entails extra cost, a lengthy calibration, and mathematical analysis.

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