High Performance SAR A/D Converter with Calibration Techniques

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Thesis Abstract

Modern portable and wireless applications are driving analog-to-digital converters (ADCs) design towards higher resolution and data rates with dramatically low power in scaled CMOS technology. Pipelined ADCs have been facing significant challenges with technology scaling since accurate residue amplification in each pipelined stage based on op-amplifier's property is required. Successive-Approximation-Register (SAR) ADC can benefits from the scaled CMOS because it does not need amplifier and most of the parts, switched capacitors and comparator, are digitally operation. Charge redistribution based capacitor DAC (CDAC) is widely used for SAR ADCs because of its superior response to resister DAC (RDAC). SAR ADC has become a main stream in application for several tens of megahertz and moderate resolution region due to the advantage of power and area efficiencies. The most design efforts for the CDAC based SAR ADC have been put on the comparator and the CDAC.

Comparators are crucial building blocks in most ADCs since they are responsible for decision-making when digital information needs to be recovered from analog signals. Mismatches due to feature scaling, process variation and input-referred supply noise cause offset that directly affects the resolution of a comparator and thus has a crucial influence on the overall performance of the ADCs. This work proposes a dynamic offset control technique based on charge compensation by timing adjustment. The error voltages suffer from charge injection and clock feed-through on each regenerative nodes are controlled in time domain so as to compensate the comparator’s offset.

On the other hand, CDAC needs to be designed large enough capacitance against thermal noise. However, implementing large capacitor array means increased cost and large input capacitance which will decrease the conversion speed. Split CDAC is widely used in SAR ADC architecture for reducing the area. However, the nonlinearity induced by the mismatch between MSB-side and LSB-side CDAC array limits the accuracy of a SAR ADC. Therefore, the calibration technique is required for split CDAC based ADC architecture. This work proposed an on chip histogram-based digitally assisted background calibration technique to compensate for CDAC mismatch with a minimum

cost. The calibration is performed using the input signal, watching the data stream to find the missing or wide code at ADC output, judge and feed back to the compensation capacitor so as to relax the nonlinearity suffer from the CDAC mismatch. The calibration does not require special input signal and extra analog hardware and offset-free comparator as well.

Split and Tri-level charge redistribution based CDAC was reported for area saving in CDAC based SAR ADC. This work proposed a partially asymmetric CDAC design technique based on the split CDAC architecture and tri-level charge redistribution technique. With this technique, it is possible for a SAR ADC to achieve 9-bit resolution with 4-bit + 3-bit split capacitor arrays which further improve the area and the power efficiency of the whole ADC.

Chapter 1 is an introduction of the study. Background of data converter technology and recent trends in ADC design are outlined along with the motivation for the study.

In chapter 2, several design issues of SAR ADC are discussed. Design consideration for the main building block like comparator and split CDAC are investigated. Digitally assisted calibration techniques are discussed at the end of the chapter.

Chapter 3 demonstrates a 380 uW 1GHz comparator with timing based dynamic offset control technique. Principle and circuits design are discussed in detail and the measurement results of the fabricated test chip are given.

Chapter 4 demonstrates a 9-bit 100MS/s SAR ADC with on chip digitally assisted background calibration. Principle and circuits design are discussed in detail and the measurement results of the fabricated test chip are provided.

Chapter 5 demonstrates a 9-bit 100MS/s SAR ADC with asymmetric CDAC design technique. Principle and circuits design are discussed in detail and the measurement results of the fabricated test chip are presented in the final of the chapter.

Chapter 6 is conclusion of the study. Results from each chapter are summarized and overview of the future work is mentioned.