High Performance SAR A/D Converter with Calibration Techniques

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Thesis Abstract

Modern portable and wireless applications are driving analog-to-digital converters (ADCs) design towards higher resolution and data rates with dramatically low power in scaled CMOS technology. Pipelined ADCs have been facing significant challenges with technology scaling since accurate residue amplification in each pipelined stage based on op-amplifier's property is required. Successive-Approximation-Register (SAR) ADC can benefits from the scaled CMOS because it does not need amplifier and most of the parts, switched capacitors and comparator, are digitally operation. Charge redistribution based capacitor DAC (CDAC) is widely used for SAR ADCs because of its superior response to resister DAC (RDAC). SAR ADC has become a main stream in application for several tens of megahertz and moderate resolution region due to the advantage of power and area efficiencies. The most design efforts for the CDAC based SAR ADC have been put on the comparator and the CDAC.

Comparators are crucial building blocks in most ADCs since they are responsible for decision-making when digital information needs to be recovered from analog signals. Mismatches due to feature scaling, process variation and input-referred supply noise cause offset that directly affects the resolution of a comparator and thus has a crucial influence on the overall performance of the ADCs. This work proposes a dynamic offset control technique based on charge compensation by timing adjustment. The error voltages suffer from charge injection and clock feed-through on each regenerative nodes are controlled in time domain so as to compensate the comparator’s offset.

On the other hand, CDAC needs to be designed large enough capacitance against thermal noise. However, implementing large capacitor array means increased cost and large input capacitance which will decrease the conversion speed. Split CDAC is widely used in SAR ADC architecture for reducing the area. However, the nonlinearity induced by the mismatch between MSB-side and LSB-side CDAC array limits the accuracy of a SAR ADC. Therefore, the calibration technique is required for split CDAC based ADC architecture. This work proposed an on chip histogram-based digitally assisted background calibration technique to compensate for CDAC mismatch with a minimum

cost. The calibration is performed using the input signal, watching the data stream to find the missing or wide code at ADC output, judge and feed back to the compensation capacitor so as to relax the nonlinearity suffer from the CDAC mismatch. The calibration does not require special input signal and extra analog hardware and offset-free comparator as well.

Split and Tri-level charge redistribution based CDAC was reported for area saving in CDAC based SAR ADC. This work proposed a partially asymmetric CDAC design technique based on the split CDAC architecture and tri-level charge redistribution technique. With this technique, it is possible for a SAR ADC to achieve 9-bit resolution with 4-bit + 3-bit split capacitor arrays which further improve the area and the power efficiency of the whole ADC.

Chapter 1 is an introduction of the study. Background of data converter technology and recent trends in ADC design are outlined along with the motivation for the study.

In chapter 2, several design issues of SAR ADC are discussed. Design consideration for the main building block like comparator and split CDAC are investigated. Digitally assisted calibration techniques are discussed at the end of the chapter.

Chapter 3 demonstrates a 380 uW 1GHz comparator with timing based dynamic offset control technique. Principle and circuits design are discussed in detail and the measurement results of the fabricated test chip are given.

Chapter 4 demonstrates a 9-bit 100MS/s SAR ADC with on chip digitally assisted background calibration. Principle and circuits design are discussed in detail and the measurement results of the fabricated test chip are provided.

Chapter 5 demonstrates a 9-bit 100MS/s SAR ADC with asymmetric CDAC design technique. Principle and circuits design are discussed in detail and the measurement results of the fabricated test chip are presented in the final of the chapter.

Chapter 6 is conclusion of the study. Results from each chapter are summarized and overview of the future work is mentioned.

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Chapter 1 Introduction

1.1 Background

Analog-to-digital converters (ADCs) are key design blocks in modern microelectronic digital communication systems since they act as bridges between the analog and digital worlds. It is a necessary component whenever data from the analog domain, through sensors or transducers, should be digitally processed.

Figure 1.1 depicts a typical signal processing system [1]. The analog input signal is first filtered to remove high-frequency components in order to avoid aliasing. Then the signal is sampled at frequency f_s, and the discrete sampled data is quantized in the analog-to-digital converter (ADC). The digital outputs from ADC are executed in the digital signal processor (DSP). Finally, they return to an analog signal by the conversion of digital-to-analog converter (DAC) and smoothing of the followed reconstruction filter.

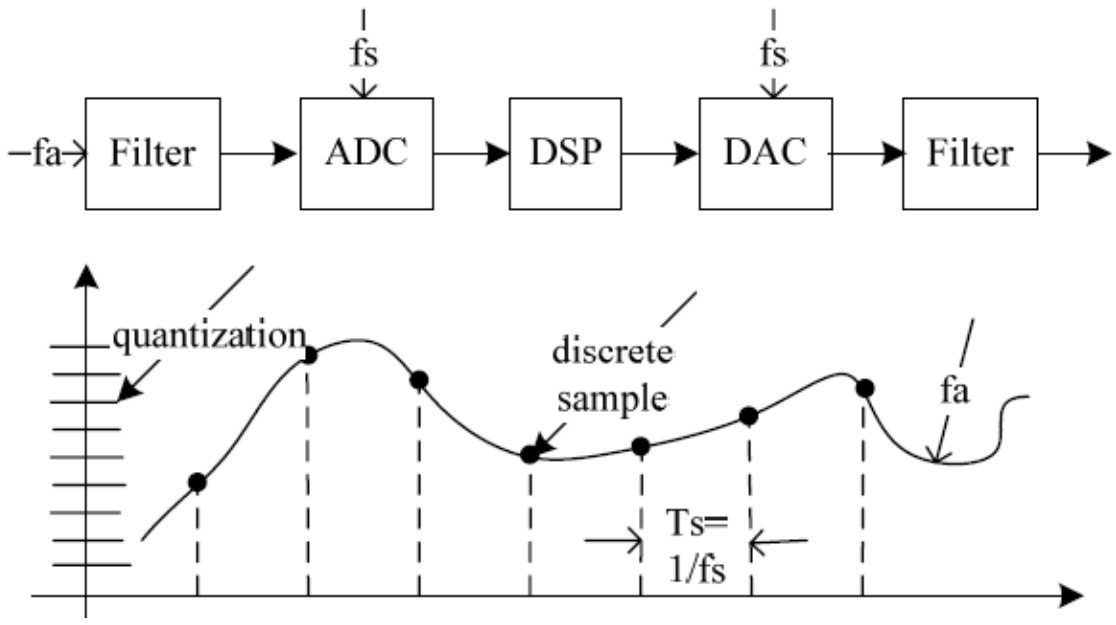


Figure 1.1 Basic signal processing system.

1.1.1 Brief History and Trends of ADC

The first documented example of an ADC was a 5-bit, electro-optical and mechanical flash-type converter patented by Paul Rainey in 1921, used to transmit facsimile over telegraph lines with 5-bit pulse-coded modulation (PCM) [2]. The first all-electrical implementation came in 1937 by Alec Harvey Reeves, this also had a 5‐bit resolution and the ADC was implemented by converting the input signal to a train of pulses which was counted to generate the binary output at a sample rate of 6 kS/s [2]. Following this, the successive approximation ADC was developed in 1948 by Black, Edson and Goodall to digitize voice to 5-bits at 8 kS/s [2]. Also in 1948, a 96 kS/s, 7-bit ADC was developed and it was implemented using an electron beam with a sensor placed on the other side of a mask. The mask had holes patterned according to the binary weights so that all bits were simultaneously detected, the pattern also employed Gray coding of the output in order to reduce the effect of errors in the most significant bit (MSB) transition [2], much as is done in modern high-speed flash ADCs [3]. Following the development of the transistor in 1947 and the integrated circuit in 1958, the ADC development continued in the 1960's with for example an 8-bit, 10 MS/s converter that was used in missile-defense programs in the United States [2]. During the same decade, all the currently used high-speed architectures were developed including pipeline ADCs with error-correction.

In the recent years there has been a trend in ADC research to use low accuracy analog components which are compensated for through the use of digital error correction [3]. The motivation behind this is that analog design have not been able to

benefit from process scaling in the same way as digital logic and therefore the relatively area-cheap digital logic is used to compensate for the shortcomings of expensive analog circuits.

1.1.2 High-Speed Nyquist rate ADC Architecture

There is a wide variety of different ADC architectures available depending on the requirements of the application. They can range from high-speed, low resolution flash converters to the high-resolution, low-speed oversampled noise-shaping sigma-delta converters. This thesis deals mainly with the design high-speed Nyquist rate converters. An overview of the performance regions for the different high-speed nyquist rate architectures is shown in Figure 1.2.

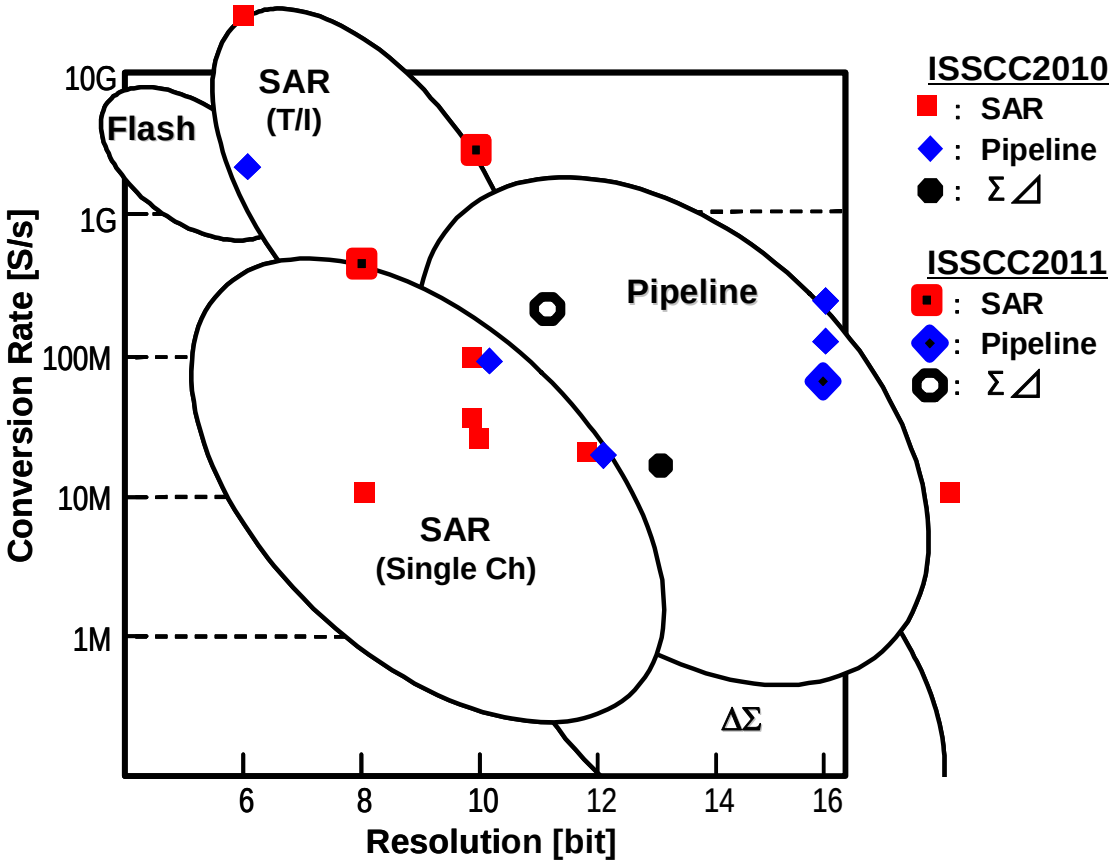


Figure 1.2 Performance regions of different high-speed ADC architectures.

A. Flash ADC

Flash ADC is known for its fast speed [5-7]. As depicted in Figure 1.3, it has 2^N-1 comparators corresponding to 2^N-1 quantization steps. The total 2^N resistors generate all the voltage references. The comparator outputs one if the input voltage is larger than the related reference voltage, and zero vice versa. There is a decoder followed at the last stage to translate the thermometer code produced by comparators to N-bit binary digital output. Though Flash ADC has a high speed, the great numbers of

comparators consume huge power and area. Taking a 9-bit Flash ADC as an example, there will be 511 comparators in the circuit. This disadvantage limits the resolution of Flash ADC up to 6 bits.

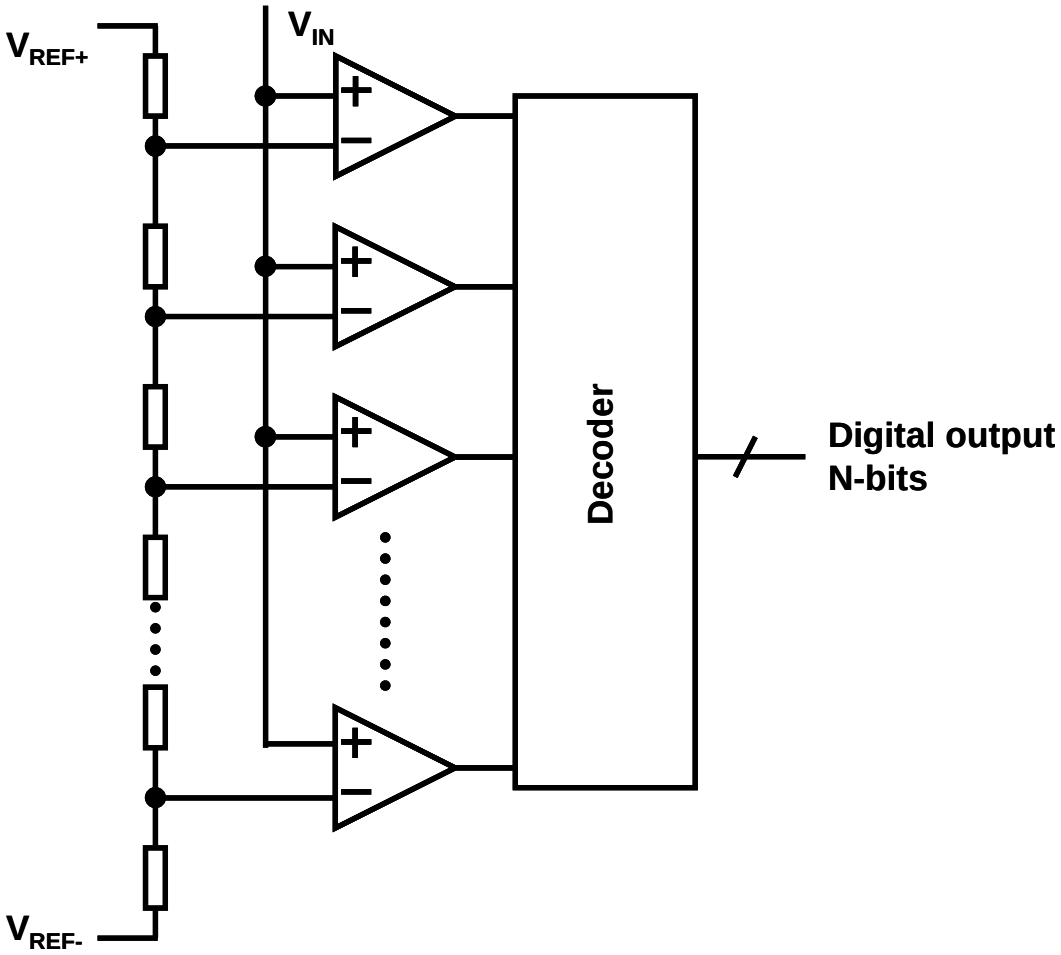
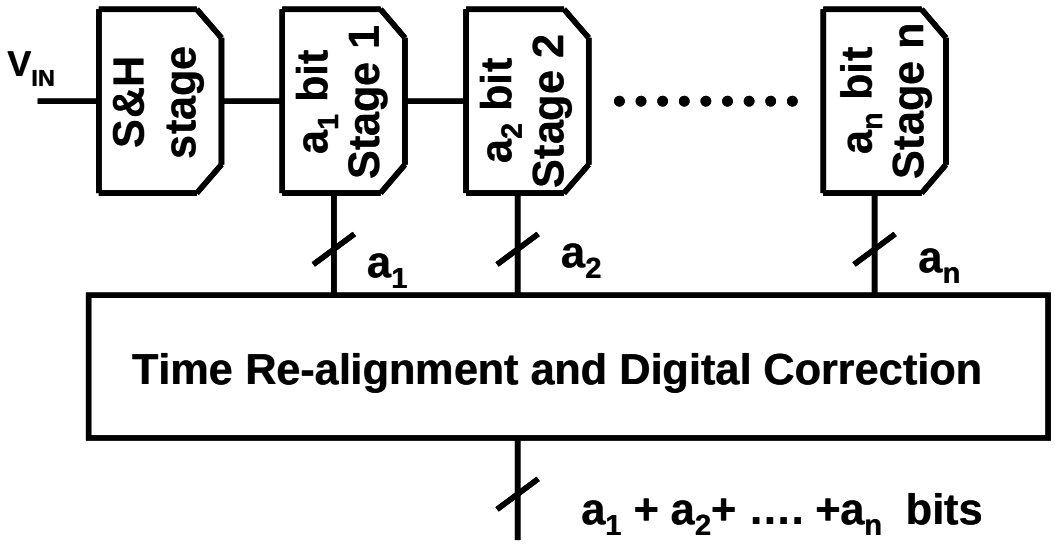


Figure 1.3 Flash ADC Architecture.

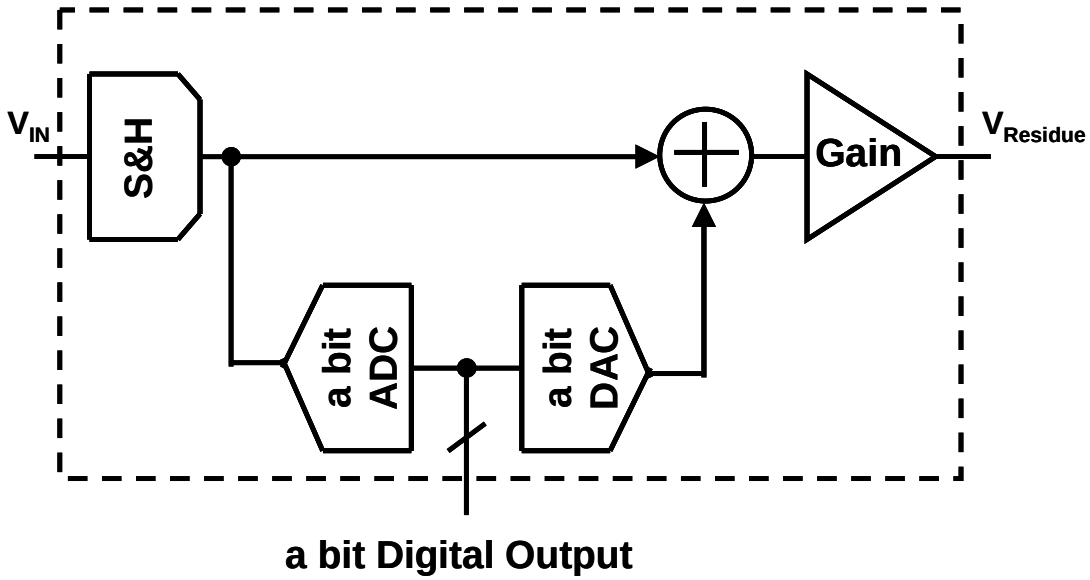
B. Pipeline ADC

The pipeline ADC architecture combines the benefits of high throughput and an input capacitance bound by noise constraints [9]. The architecture is shown in Figure 1.4. Each stage samples the input signal and generates *ak* additional bits of information of the input. An output residue is sent to the succeeding stages with the last stage

typically implemented as a flash ADC. Each stage, known as a multiplying DAC (MDAC), is based on the same principle as the algorithmic ADC and is shown in Figure 1.4. The input signal is sampled and quantized by an *a*-bit sub-ADC, this is converted back to analog and subtracted from the input signal, resulting in the sub-ADC quantization error. This is amplified to cover the full input range which has the advantage that all pipeline stages can be designed identically, simplifying the implementation. Despite the initial N-clock cycles, Pipeline ADC is frequently used for its high speed and resolution.



(a) Pipeline architecture



(b) **MDAC**

Figure 1.4 Pipeline ADC architecture.

C. SAR ADC

Successive approximation register (SAR) ADC is designed based on a binary search algorithm [10-13]. It consists of a successive approximation register (SAR), a digital-to-analog converter, a comparator and a sample and hold circuit, which is illustrated in Figure 1.5. First, input voltage (V_{IN}) is sampled and the registers are reset to zero. Secondly, the conversion starts through an approximation of MSB (set MSB as one) by SAR; DAC converts the digital information to a voltage V_{OUT} (half of the reference voltage V_{REF}); Comparator compares V_{OUT} with V_{IN}. If V_{IN} is larger than V_{OUT}, it outputs *one*, otherwise, it outputs *zero*; SAR loads the comparator result, registers the value of MSB and generates its next approximation; the conversion

continues until the LSB is decided. Therefore, an N-bit SAR ADC needs N clock cycles per conversion.

SAR ADC is known for its simple structure, thus consuming less power and saving more die size. However, with increase of its resolution, the linearity problem of DAC becomes more severe, which directly causes non linearity of ADC. Therefore, SAR ADC is not suitable for high resolution.

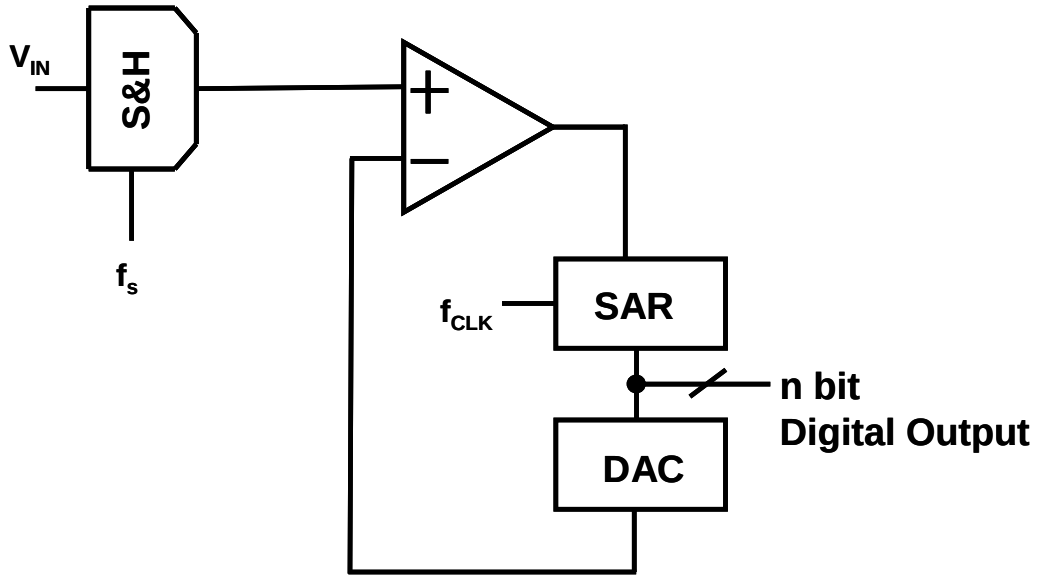


Figure 1.5 SAR ADC architecture.

D. Time-Interleaved ADC

In order to achieve very high sample-rates, especially at medium resolution, then a single ADC is not sufficient and time-interleaving of ADCs is required to increase the sample rate [14-16]. Time-interleaved technique allows power-efficient architectures such as SAR and Pipeline ADCs to be used to achieve low-to medium resolutions at sample rates that still within the reach of flash ADCs. In the time-interleaved configuration, each sub-ADC samples the input in a sequential manner. The concept of

time-interleaving is shown in Figure 1.6 where *n* parallel ADCs are used to increase the effective sample rate *n* times. The main sample-and-hold samples the input signal at the frequency *fs*, this is later re-sampled the by the sub-S&H at the frequency of *fs/n* but with a clock duty cycle of *1/n*. The clock signal to each sub-S&H is phase shifted to uniformly sample the input signal. Using this input technique, the high bandwidth and sample rate requirements are placed on the input stage alone, allowing the input stage of the sub-ADCs to be designed with a bandwidth set by the Nyquist rate of that individual ADC.

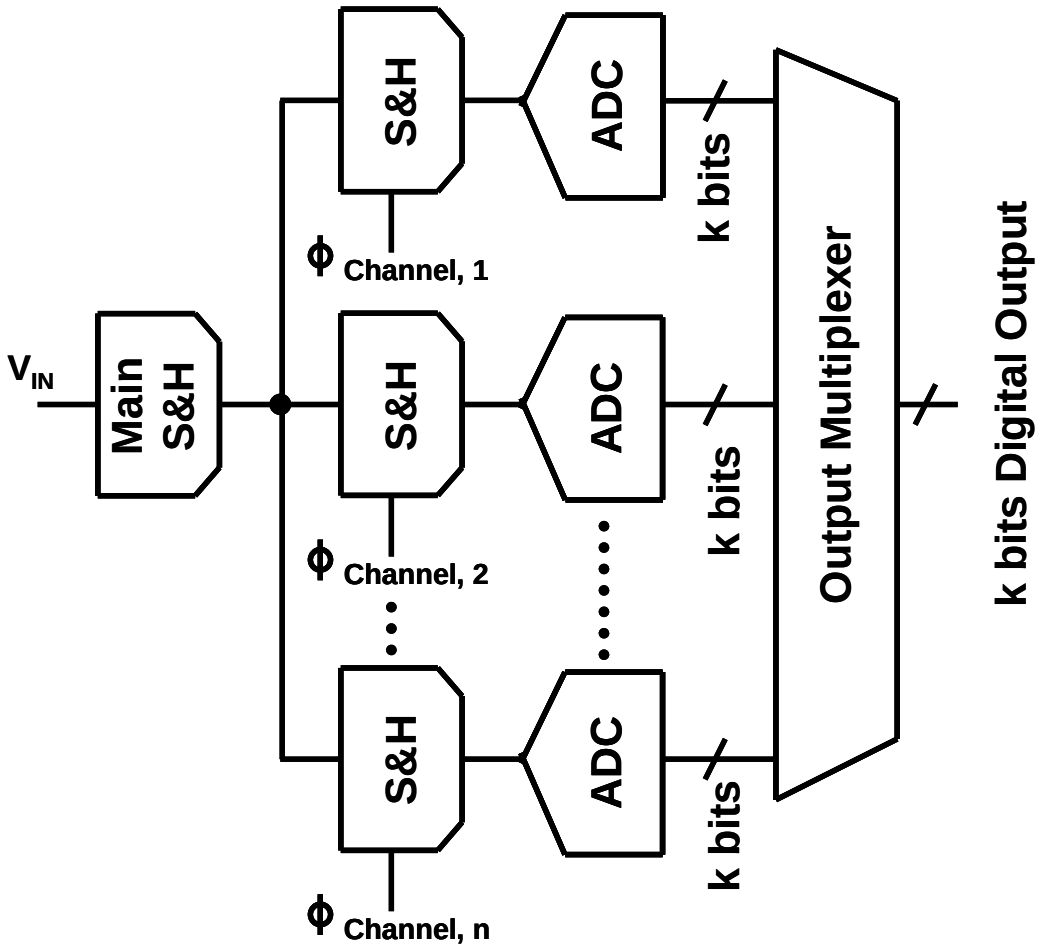


Figure 1.6. Time-Interleaved ADC architecture.

1.1.3 Applications with Different Types of ADC Architectures

The four popular high-speed ADC architectures were described in the above sections. ADCs are selected according to specific application within the consideration of resolution, power, size, sampling frequency, performance and etc. Among the aforesaid four types of high-speed ADC, the time-interleaved ADC is a combination of several single channeled ADC, which is not suitable to be compared with the other three types of high-speed ADC architecture. So we just take the other three types of architectures, Flash, Pipeline and SAR as a comparison. For some applications, almost all the architectures may work well; for others, there may be a better choice to achieve the best performance. For example, a Flash ADC is most popular for applications requiring ultra-high speed when resolution and power consumption is not a primary concern; A SAR ADC is usually first considered to be implemented in the application of low power and small size with medium resolution[12-13]. Figure 1.7 shows the A/D converter application space according to different requirements of ADC sampling rate and resolution.

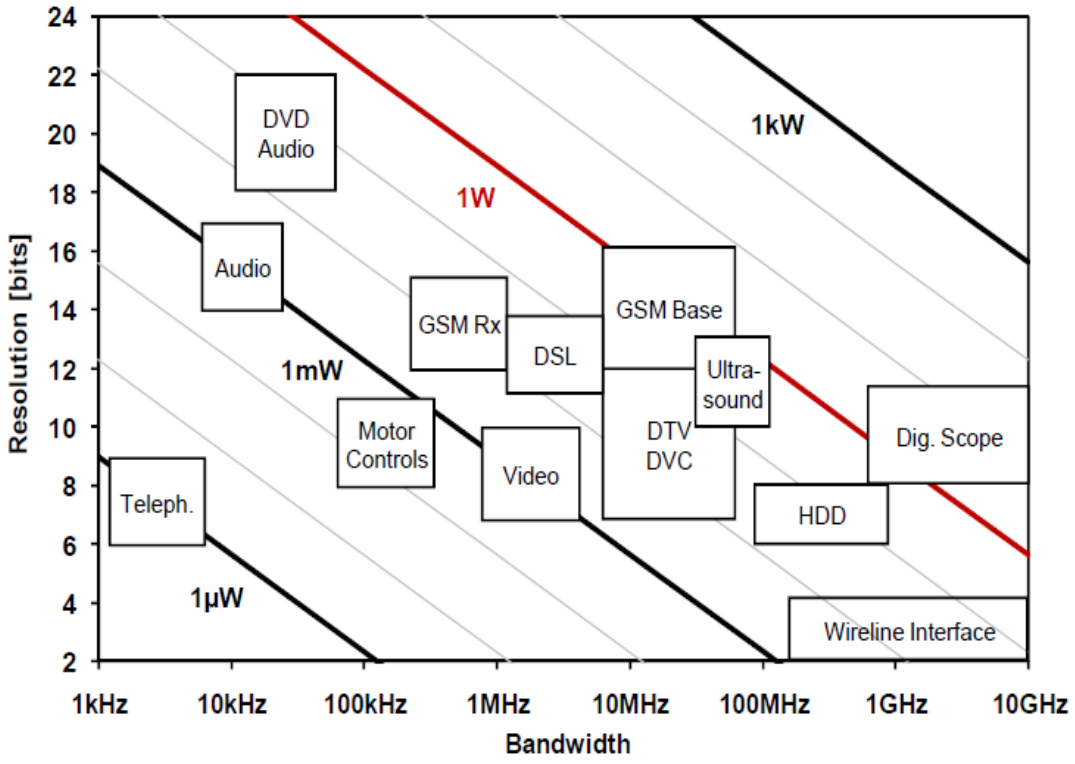


Figure 1.7 A/D Converter Application Space.

1.2 Research Motivation

An ADC with a medium sampling rate (a few tens to hundreds of MS/s) and a moderate resolution (6-12 bits) is a crucial building block for battery-powered applications including data communication and multi-media signal processing systems. Modern portable and wireless applications are driving ADC design towards higher performance with ultra low power in scaled CMOS technology. Pipelined ADCs have been facing significant challenges with technology scaling since accurate residue amplification in each pipelined stage based on op-amplifier's property is required [1]-[3]. Reduced drain-induced barrier results in limited gain in short channel devices. Implementing amplifier that consumes the static power also leads to large power consumption.

Comparators are crucial building blocks in A/D converters since they are responsible for decision-making when digital information needs to be recovered from analog signals [1-6]. With the supply voltage scaling in CMOS technologies and the increasing demand for low power and high speed, the channel length of the transistors are minimized at the expense of an increased level of mismatch [7-8]. Mismatches in the pre-amplifier and regenerative stages due to process variations, and input-referred supply noise cause offset that directly affects the resolution of a comparator and thus has a crucial influence on the overall performance in those applications [9-11]. For higher speed and resolutions in deep sub-micron CMOS technology, it is necessary to cancel or calibrate for these mismatch by means of circuit or algorithmic techniques [12-19]. Among recent comparator offset cancellation techniques, an approach using capacitors with dynamic correction to adjust the output loads of comparators [18] degrades the response. Another approach using capacitors to control current for offset cancellation [19] requires refreshing for the capacitors to maintain the charge against the leakage. Effective and simple method for offset cancel by applying additional circuits without scarifying the power, speed and area is always challenging.

On the other hand, SAR ADC can benefit from the advancement of scaled CMOS technology since it does not need amplifier and most of the parts, switched capacitors and comparator, are digitally operation. In the view point of power and area efficiencies, SAR ADC is better than pipelined ADC. Currently, improvements in system architecture and calibration technologies enable the SAR ADCs to be a mainstream in medium sampling rate and resolution region [4]-[10]. Charge redistribution based CDAC is widely used for SAR ADCs because of its superior response to resister DAC (RDAC). However, CDAC needs to be large enough capacitance against thermal noise,

as well as mismatch of each unit capacitors. Large capacitance required by the CDAC results in limited settling speed, increased power consumption and silicon cost. Therefore, improvement of the area and energy efficiencies for the CDAC is one of the most important issues for SAR ADC design.

Split CDAC is one of the solutions for both area efficiency and decreasing the input capacitance. However, the nonlinearity induced by the mismatch between MSB-side and LSB-side CDAC array limits the accuracy of a split CDAC based SAR ADC. Therefore, the calibration technique is required for most of the ADC blocks. Analog calibration techniques [17], [18] use analog components in the signal path to generate higher linearity at the expense of conversion speed. On the other hand, digitally assisted calibration techniques, which compensate for ADC mismatch, are reported [7], [10]-[13], [15]. For example, [15] can correct the linearity as well as radix error, but it needs two times conversion, resulting in the conversion rate into half. The trade off between compensated performance and the costs, area, power, sacrificed performance and convergent time, needs to be considered. Therefore, low cost, high efficient calibration technique is always required by the industry in SAR ADC design.

1.3 Target of This Research

Many ADC architectures and integrated circuit technologies have been proposed and implemented to push back performance limits. Although different metrics and interpretations of ADC performances may be used in different research work, an overall trend is not affected in a significant way. The trend that cuts across nearly all resolutions and sampling rates is “low power”. The average FOM becomes smaller and smaller, indicating lower energy consumed in each effective conversion step. This

work targets battery-powered data communication and imaging processing systems. ADCs with medium resolution (8-bit to 10-bit) and moderate sampling rate (several tens to hundred of MHz) are required for applications such as one-segment digital TV receiver in cell phones, high definition camcorders, and etc. Today's portable consumer electronics devices require designs of professional-quality sound, display and high definition video with lower power consumption, smaller area, more functions and lower cost. Therefore, energy efficient and area efficient ADCs with high performance are in great demand. So far considerable research has been done on the design of ADC systems and many works [10-19] have reported high performance as shown in Figure 1.8 and 1.9. In this work a 9-bit 100-MS/s ADC has been designed and implemented with power consumption of only 1.28 mW, resulting in an FOM of 45 fJ/conv-step, which is one of the best-performing converters. Among the best-performing ADC reported in the last few years as shown in Figure 1.8 and 1.9, some of the design does not implement the calibration while some other design implement the calibration techniques by off-chip. Although the designed ADC does not achieve the best performance compared to the state-of-art reported ADC, the on-chip digitally assisted background calibration is implemented into a SAR ADC which make this research be one of the practical and feasible solution for mass production.

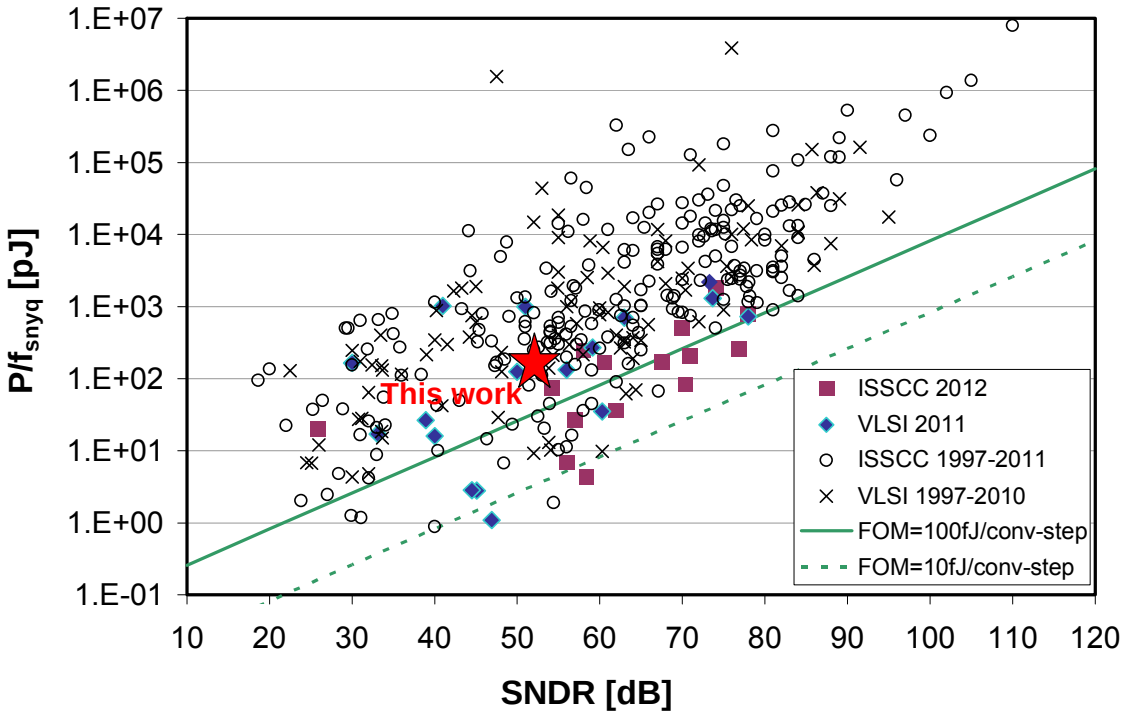


Figure 1.8 SNDR vs energy of ADC reported recently.

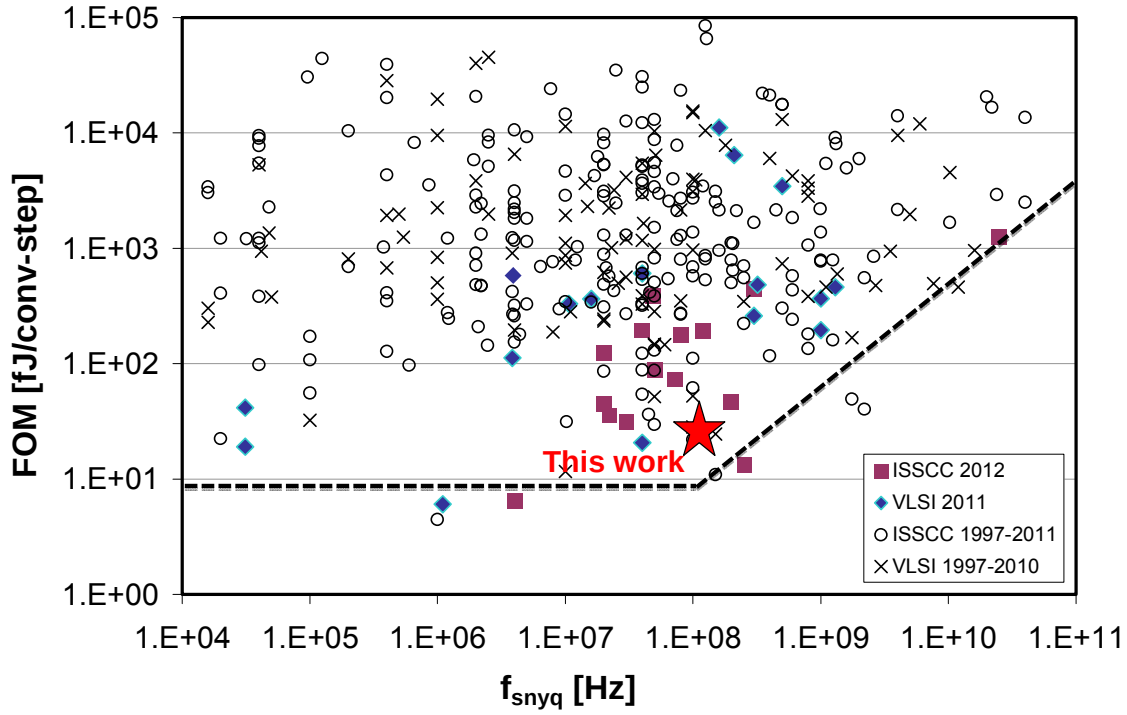


Figure 1.9 Sampling rate vs FOM of ADC reported recently.

1.4 Thesis Organization

This thesis is divided into six chapters as shown in Figure 1.10.

Chapter 1 is an introduction of the study. Background of data converter technology and recent trends in ADC design are outlined along with the motivation for the study.

In chapter 2, several design issues of SAR ADC are discussed. Design consideration for the main building block like comparator and split CDAC are investigated. Digitally assisted calibration techniques are discussed at the end of the chapter.

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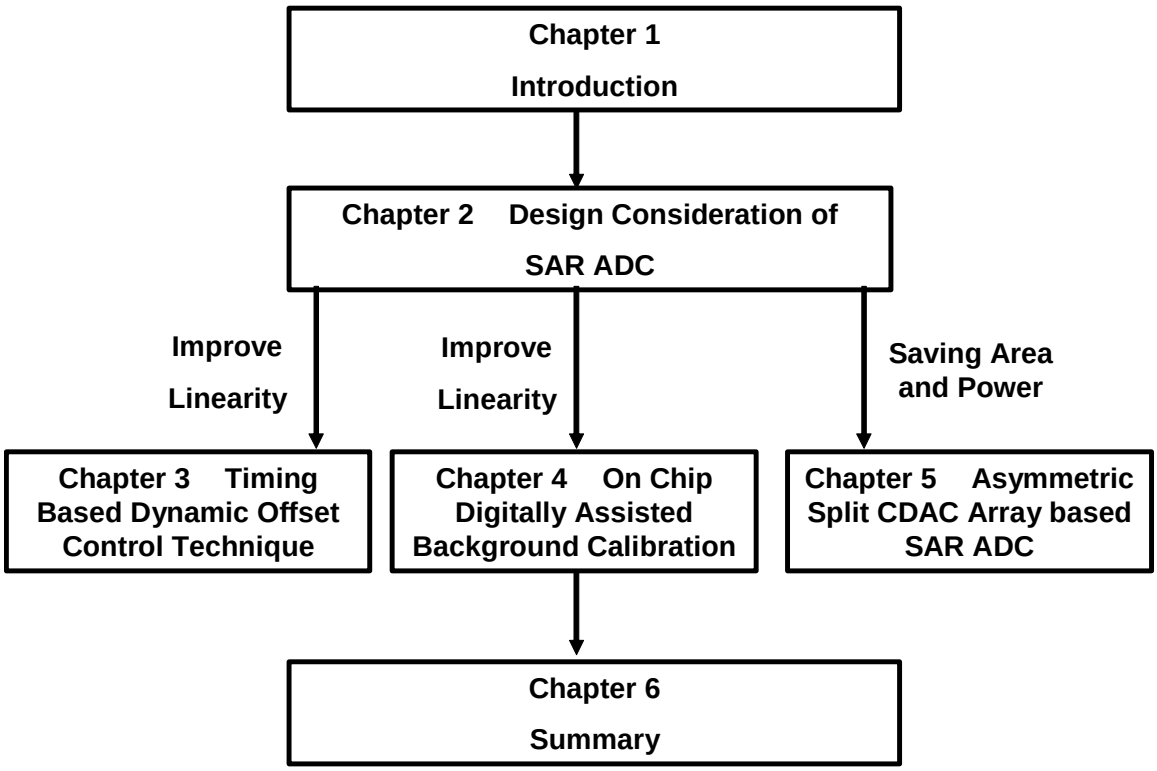

Figure 1.10 Organization flowchart of thesis.

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Chapter 2 Design Considerations for High Performance SAR ADC

2.1 ADC Performance Metrics

In order to measure the performance of a converter, many different performance specifications are utilized. Similar to the other types of ADC architectures, some of these specifications for SAR ADC performance can be more important than the others and an optimization should be carried out to achieve the best performance. ADC specifications can be classified in two groups: a) DC (static) and b) AC (dynamic) specifications. DC specifications are related with the static transfer function of the ADCs where as the AC specifications cover the dynamic performance of the converters.

2.1.1 Static Error

Static errors are deviation of converter transfer characteristics from ideal one. The static performance of an ADC is defined by these metrics: offset error, gain error, and nonlinearities like DNL error and INL errors.

A. Offset

Offset is a shift for zero input and it changes the transfer characteristic in such a way that all the steps are shifted by the amount of the offset which is generally expressed in LSB. Figure 2.1 presents the ideal transfer characteristic of an ADC and the one with offset.

For systems utilizing a single ADC, offset should be corrected substantially by shifting the raw converter output by the amount of the offset voltage in terms of LSB. It can be a more severe problem for time-interleaved applications where many ADCs operate in parallel and all suffer from different offsets due to mismatches. In such a

case, undesired spurs will appear within the bandwidth of interest and these spurs can deteriorate the SNDR (Signal-to-Noise-and-Distortion Ratio) significantly. Robust offset calibration schemes are generally mandatory for such applications.

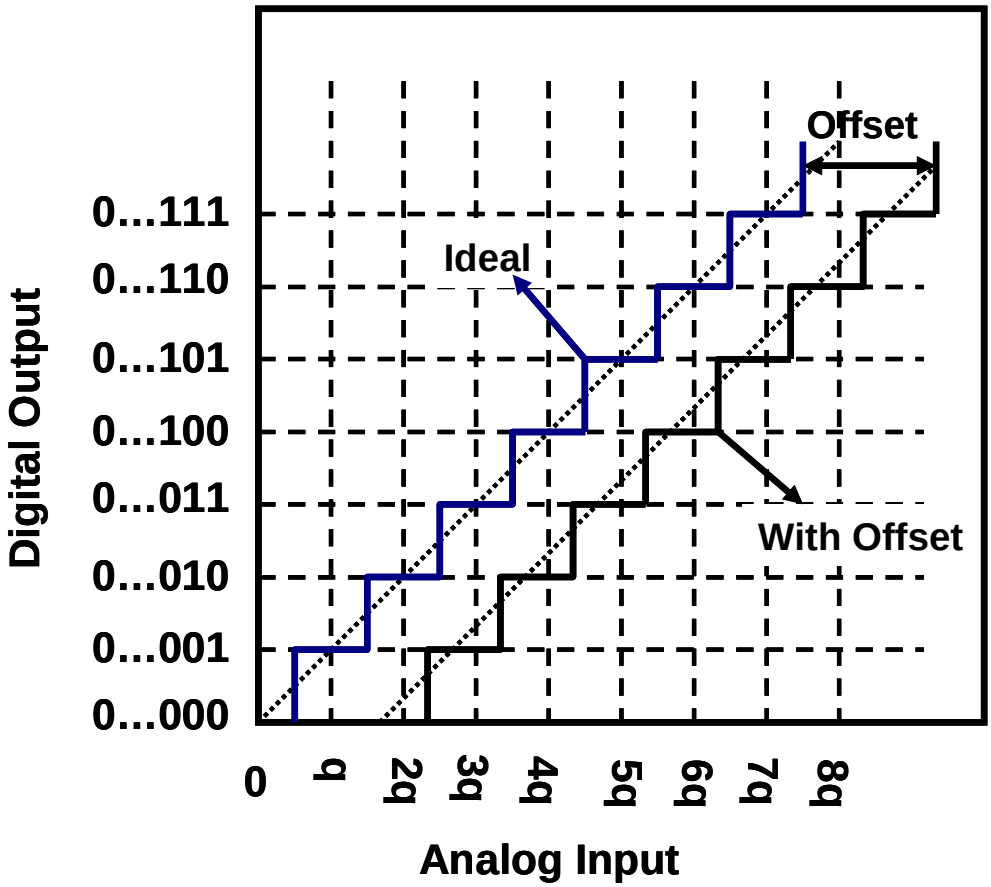

Figure 2.1 Ideal transfer characteristic and the one with offset.

B. Gain Error

The gain of the transfer characteristic of an ADC can be calculated by drawing a straight line which interpolates the actual transfer curve. The resulting line can be expressed as D=O+GA where D represents the digital output, O represents the offset, A represents the analog input, and G represents the gain. The error on the slope of the straight line is referred as the gain error and it is generally expressed as the percentage

difference between the ideal and the actual gains but different expressions are also possible such as full scale error [1].

Figure 2.1 shows the ideal transfer curve and the one with gain error. Note that in the gain error case, the step sizes are also identical to each other but different from the ideal case. Similar to offset, gain error can be corrected to a great extent digitally by multiplying the raw ADC data with a correction coefficient.

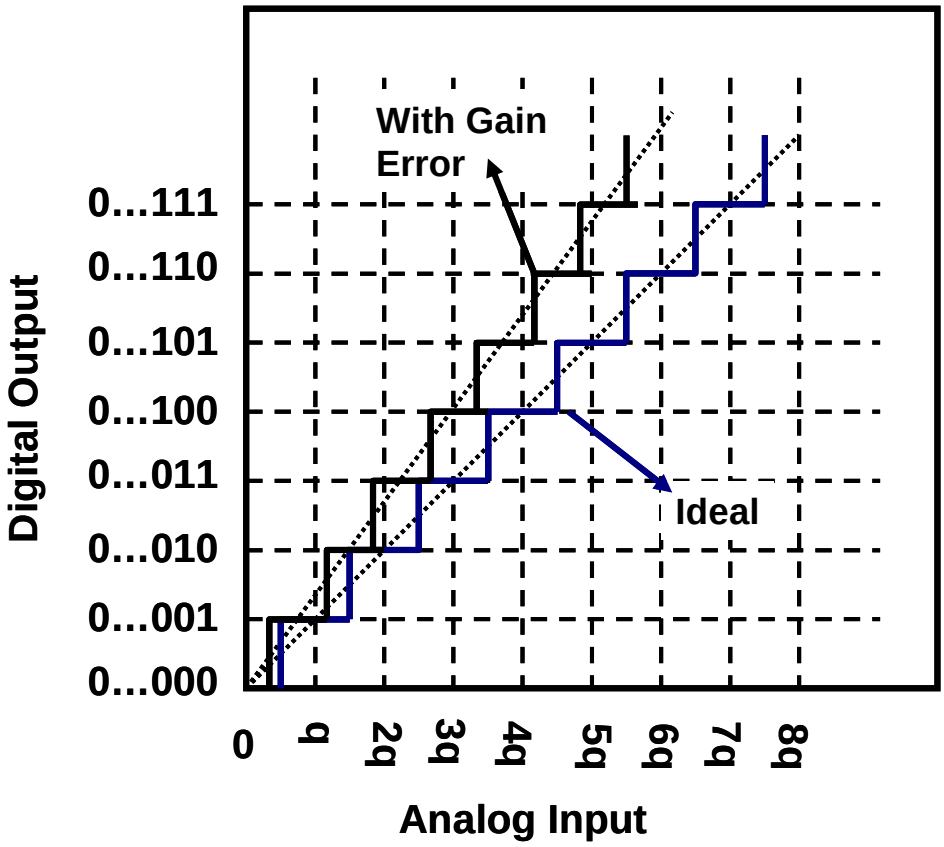

Figure 2.1 Ideal transfer characteristic and the one with gain error.

C Nonlinearities

Both for the offset and the gain error cases, the linearity of the transfer curves have been preserved. The step sizes were identical to each other but either the zero crossing or the step size was different from the ideal ones. The main reason for nonlinearity

arises from the variation in the step sizes of the transfer curve. Figure 2.3 shows two non-ideal transfer curves with non-linearity problems [1].

- As given in Figure 2.3 (a), these variations can be random with almost no correlation between successive steps. In this case the interpolating curve can be still very close the ideal one but the quantization error can vary significantly. In Figure 2.3 (b), the step size is small at the beginning but increases as the analog input becomes larger. Thus, there is a strong correlation between the successive steps and the interpolating curve moves away from the ideal one. However, the variation in the quantization error might be smaller [2]. To cover both of the cases presented in Figure 2.3, two different non-linearity specifications are used: 1) Differential Non-Linearity (DNL) and 2) Integral Non- Linearity (INL).

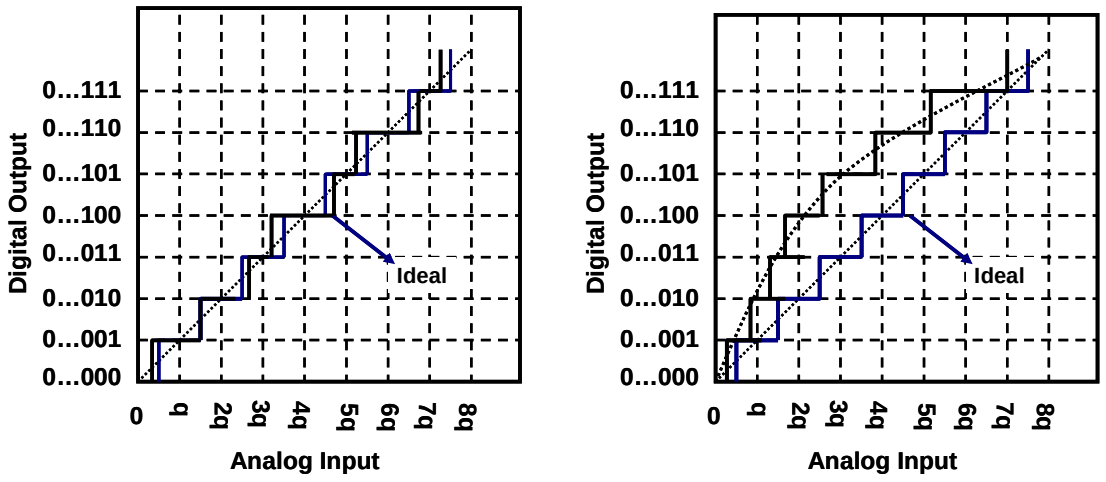

Figure 2.3 Two non-ideal transfer curves

In the IEEE standard for measurements of ADCs [3], they are defined as:

- DNL[k] – The difference between the code bin width of code k and the average code bin width, divided by the average code bin width after correcting for gain and offset.
- DNL – The maximum absolute value of DNL for all k. Simply, Figure 2.3 (a) suffers from large DNL but small INL. On the other hand, Figure 2.3 (b) suffers from large INL but relatively smaller DNL.
- INL[k] – The difference between the ideal and actual code transition level k after correcting for gain and offset.

INL – The maximum absolute value of INL for all k.

2.1.2 Dynamic Error

In order to completely quantify ADC performance, also sampling and input frequency dependant error sources should be characterized. The terms used to describe the dynamic performance are, as defined in [3]:

- SNR - The ratio of the signal power to the total noise power at the output, measured typically for a sinusoidal input.
- Signal-to-noise-and-distortion (SNDR) -The ratio of the signal power to the total noise and harmonic power at the output, when the input is a sinusoid.
- Effective number of bits (ENOB) -Defined as in (2.1), where SNDR is the maximum SNDR for the converter, measured in decibel.

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2.1}$$

- Dynamic Range (DR) - The ratio of the power of a full-scale input sinusoidal to the power of a sinusoidal input for which SNR = 0 dB.

There is a wide variety of sources responsible for causing degradation of the dynamic performance, for example, architecture independent examples are finite circuit bandwidth and clock jitter in sampling circuits.

2.1.3 Figure-of-Merit (FoM)

FoM is generally used to compare the performances of different ADCs. It basically gives an idea on the power efficiency of the converter and it is expressed as:

$$FoM = \frac{Total\ Power}{2^{ENOB} \cdot BW} \tag{2.2}$$

where BW is the bandwidth of the input signal and total power is the power consumed by the converter. FoM is not a solid parameter due to its strong dependence on technology parameters and signal bandwidth, but can be used to compare efficiency of the converters used in similar applications.

2.2 Design considerations for SAR ADC with Binary-Weighted Capacitive DAC

A general SAR ADC is composed of an input sampling network (T&H), a comparator, a Digital-to-Analog Converter (DAC) and a digital controller (SAR Logic). The DAC has the same resolution as the ADC which has been introduced in chapter 1. The most critical block in a SAR ADC is the DAC. DAC can be implemented with many different well-known techniques. However, the most widely used DAC topology in SAR ADCs is the charge-redistribution based capacitive array

[4], as capacitive arrays do not dissipate static power and improve the power efficiency significantly. The most common capacitive DAC is the binary-weighted architecture which as been shown in Figure 2.4 with a 9-bit resolution. In this architecture, the input load capacitance and area of a binary-weighted capacitor DAC (CDAC) increase exponentially with the number of bits. For a 9-bit resolution as an example, the total input capacitance is equal to 512C and the total area is 512 times the unit capacitor area. This shows area un-efficiency by using this architecture.

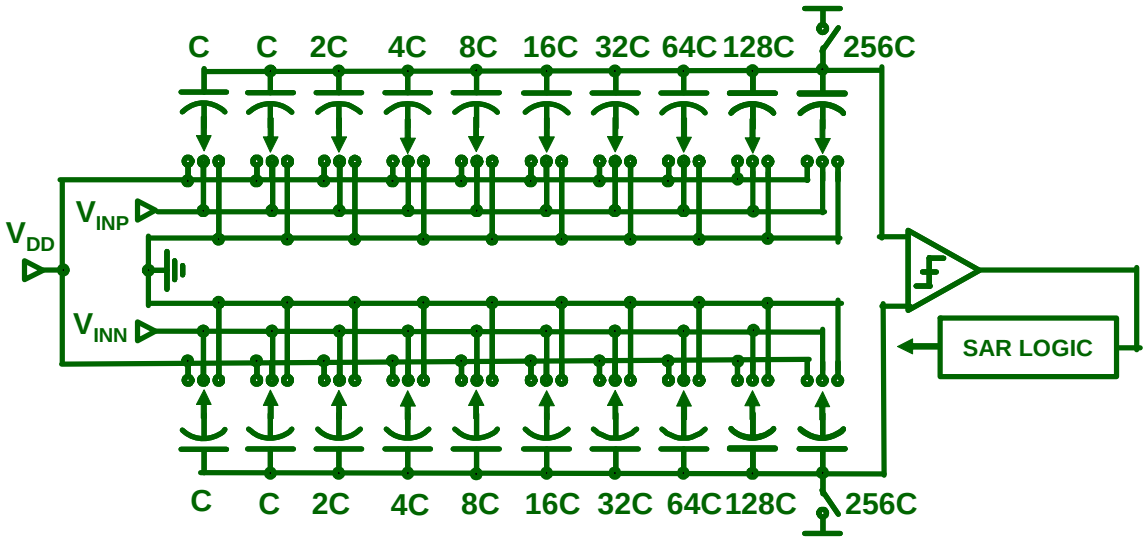

Figure 2.4 Conventional binary-weighted CDAC based SAR ADC (9-bit).

Split CDAC is one of alternative to reduce both input capacitance and area, shown in Figure 2.5, a fractional value bridge capacitor is implemented so that the two capacitor arrays have the same scaling [5]. In the charge redistribution, the total weight of the left array is equal to the weight of the lowest bit in the right array.

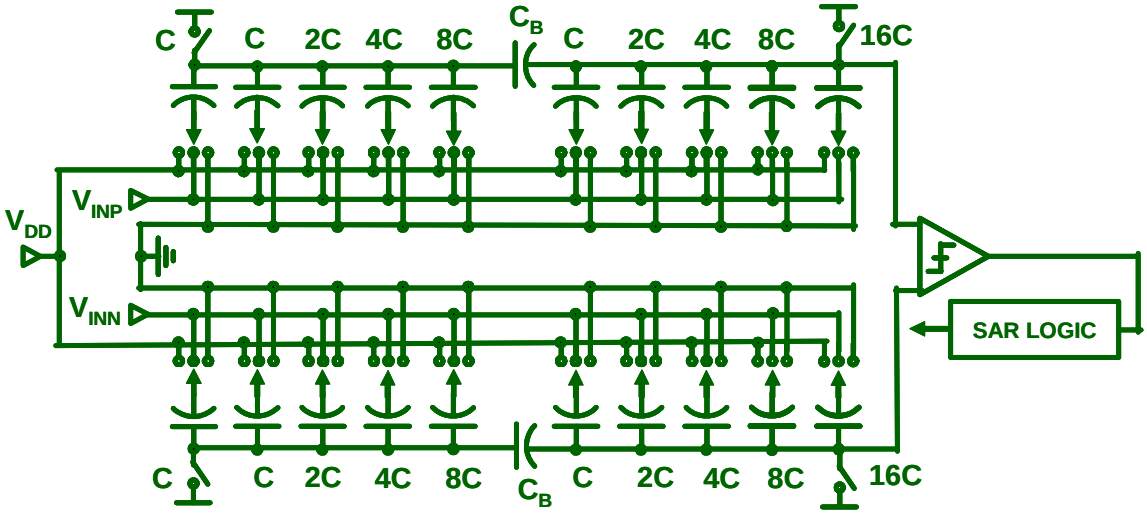

Figure 2.5 Differential split CDAC based SAR ADC (9-bit).

The performance of this type of SAR ADC is limited by:

A. The comparator, which must resolve small differences in V_{IN} and V_{DAC} within the specified time with accuracy;

B. Each of the capacitors associated with the data bits would be exactly twice the value of the next-smaller capacitor, and the settling time of the DAC, which must settle to within the resolution of the overall converter, for example, ½ LSB.

Therefore, the two critical components of this type of SAR ADC are the comparator and the DAC.

The requirements of the comparator are speed and accuracy. Although comparator offset does not affect overall linearity as it appears as an offset in the overall transfer characteristic, the comparator needs to resolve voltages within the accuracy of the overall system. Therefore, offset-cancellation techniques are usually applied to reduce the comparator offset. It needs to be as accurate as the overall system. The comparator is usually designed to have input-referred noise less than 1 LSB.

On the other hand, in split CDAC architecture, the bridge capacitor being fraction causes poor matching with the other capacitors. In addition, parasitic capacitance is sensitive to process options, such as the number of metal layers, which varies according to system-on-chips (SoC), the split CDAC linearity performance is not well controlled. Therefore, CDAC calibration is always necessary for this type of SAR ADC.

2.3 Calibration Techniques

Comparator offset calibration have been widely researched by the academic and industry [6-15]. Among recent comparator offset calibration techniques, an approach using capacitors with dynamic correction to adjust the output loads of comparators [12] degrades the response. Another approach using capacitors to control current for offset cancellation [13] requires refreshing for the capacitors to maintain the charge against the leakage. This work proposes a dynamic offset control technique based on charge compensation by timing adjustment. The charge injection and clock feed-through [13-15] results from turning off the latch reset transistor are investigated. These two effects are generally considered as limitations to the accuracy performance of the analog CMOS circuits since they introduce error voltages to the surrounding sampling node. The principle and circuits in detail will be discussed in chapter 3.

As for the CDAC, the calibration technique is also required for most of the ADC blocks. Analog calibration techniques [16-17] use analog components in the signal path to generate higher linearity at the expense of conversion speed. On the other hand, digitally assisted calibration techniques, which compensate for ADC mismatch, are reported [18-21]. For example, [20] is able to correct the linearity as well as radix error,

but it needs two times conversion, resulting in the conversion rate into half. The trade off between compensated performance and the costs, area, power, sacrificed performance and convergent time, needs to be considered. This work proposed an on chip histogram-based digitally assisted technique to compensate for CDAC mismatch with a minimum cost. The calibration is performed using the input signal, watching the data stream to find the missing or wide code at ADC output, judge and feed back to the compensation capacitor so as to relax the nonlinearity suffer from the CDAC mismatch. The calibration does not require special input signal and extra analog hardware and offset-free comparator as well. The calibration operation and circuits design in detail will be discussed in chapter 4.

2.4 Area Efficiency

Improvement of the area and energy efficiencies for the CDAC is one of the most important issues for SAR ADC design [22-28]. This work proposed a partially asymmetric CDAC design technique based on the split CDAC architecture and tri-level charge redistribution technique [23]. With this technique, it is possible for a SAR ADC to achieve 9-bit resolution with 4-bit + 3-bit split capacitor arrays. The principle and the circuits will be presented in chapter 5.

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Chapter 3 Design of 1 GHz 380 uW Comparator with Dynamic Offset Cancel Technology

3.1 Introduction

. With the supply voltage scaling in CMOS technologies and the increasing demand for low power and high speed, the channel length of the transistors are minimized at the expense of an increased level of mismatch [1-2]. Mismatches in the pre-amplifier and regenerative stages due to process variations, and input-referred supply noise cause offset that directly affects the resolution of a comparator and thus has a crucial influence on the overall performance in many applications like ADC. Other important limitations are the offset between channels for interleaved architectures as they are transformed into dynamic errors by the system operation [3-5]. For higher speed and resolutions in deep sub-micron CMOS technology, it is often necessary to calibrate or control for these mismatch by means of circuit or algorithmic techniques [6-13]. Among recent comparator offset calibration techniques, an approach using capacitors with dynamic correction to adjust the output loads of comparators [12] degrades the response. Another approach using capacitors to control current for offset cancellation [13] requires refreshing for the capacitors to maintain the charge against the leakage. Effective and simple method for offset calibration by applying additional circuits without scarifying the power, speed and area is always challenging.

This work proposes a dynamic offset control technique based on charge compensation by timing adjustment. The charge injection and clock feed-through results from turning off the latch reset transistor are investigated.

3.2 Dynamic Offset Control Technique

3.2.1 Principle of Charge Compensation Approach for Comparator Offset Control

Figure 3.1 shows a comparator consists of preamplifier and cross-coupled regenerative pair. A different input pair feeds currents into a cross-coupled CMOS regenerative pair I_1 and I_2. The regenerative nodes, c and d, are connected through reset transistor M_3 which helps recovering from overdrive as well as allowing offset compensation. Two source-drain shorted NMOS transistors M_4 and M_5 are implemented on each regenerative node respectively. M_4 and M_5 have the same channel length with that of M_3 while have the half channel width of M_3. The switching of the M_4 and M_5 are controlled by applying timing clock OC_1 and OC_2 on their gates. Logic levels are produced at V_{out} when the latch stage is enabled. The principle of the dynamic offset control is explained in detail as follows.

During the reset period, M_3 is turning on, and the differential inputs pair of the preamplifier is biased to ground through switches S_1 and S_2. Assuming that the Offset of the preamplifier is positive and the latch stage is ideally symmetric, then the voltage on node a is lower than node b since the current I (M_2) > I (M_1). During this period, the M_3 is turning on by keeping its gate voltage, RES, at high while M_4 and M_5 are turning off by applying their gate voltages, OC_1 and OC_2, at low. Thus the regenerative nodes are shorted together through M_3, resulting in $V_c \approx V_d$ (Voltage on node c and d). The total charge Q_{ch} in the inversion layer of M_3 is

$$Q_{ch} = LWC_{ox}(V_{RES} - V_c - V_{TH}) = LWC_{ox}V_{od} \qquad (3.1)$$

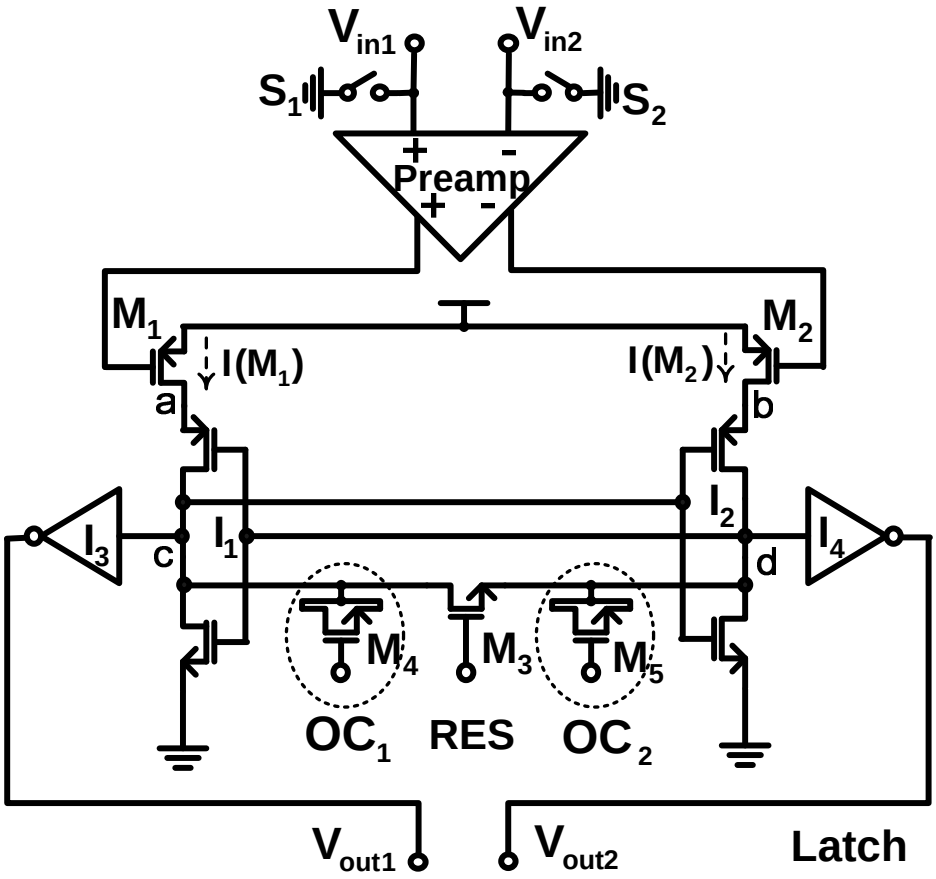


Figure 3.1 Comparator with dynamic offset control technique.

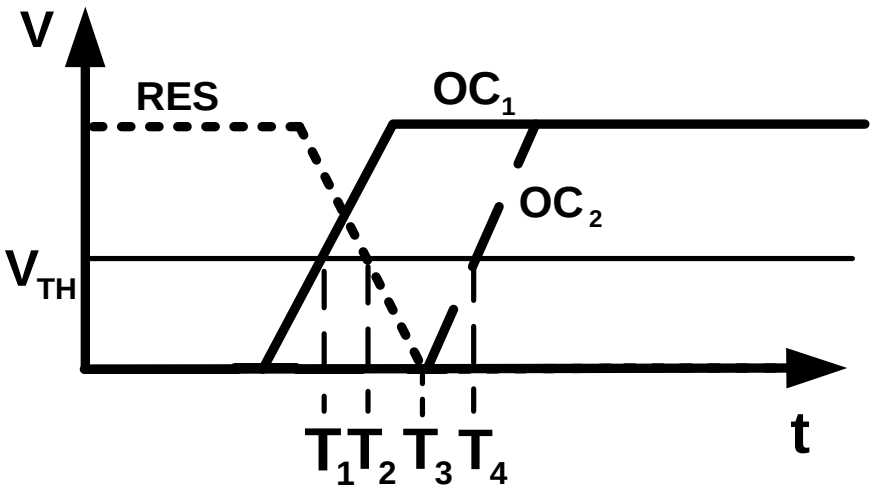
where L denotes the effective channel length, C_{ox} multiplied by W presents the total gate capacitance per unit length, and V_{TH} denotes the threshold voltage of M_3. Equation (3.1) indicates that Q_{ch} depends on the overdrive voltage V_{od}. Because the charges absorbed by M_4 and M_5 also have a dependency on the overdrive voltage, the same as M_3 as explained in (3.1), the voltage at node c and d will be influenced by the overdrive voltage of M_4 and M_5 at the moment M_3 turns off.

To perform the offset compensation, the channel charge on node c and d are absorbed by M_4 and M_5 with appropriate timings. Figure 3.2 shows the mechanism of

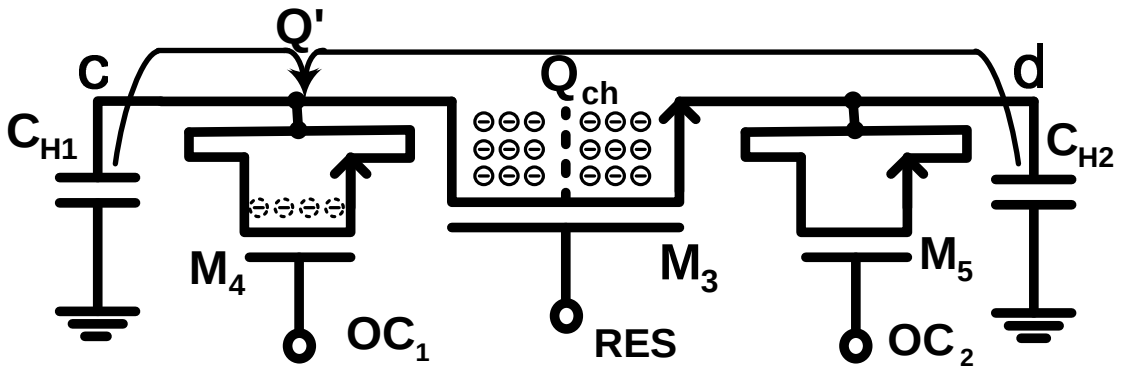
the proposed timing-based offset control. Here, we explain the case where a positive input-referred offset is compensated for.

Let T_1, T_2 and T_4 , in Figure 3.2 (a), be the moments at which the overdrive voltages reach the threshold levels of M_4, M_3 and M_5, T_3 is the moment at which M_3 completely turning off. The timings are chosen to be $T_1 < T_2 < T_3 < T_4$. This means M_3 starts to turn off while the M_4 turns on and M_5 remains off.

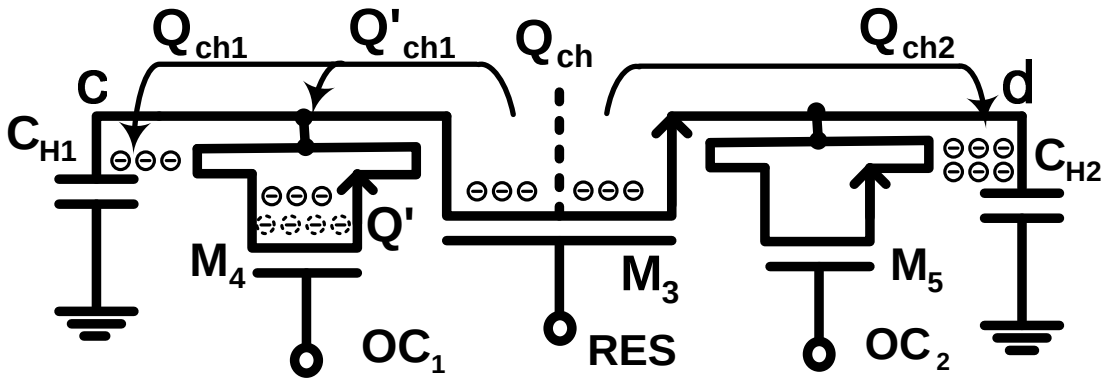
During the period between T_1 and T_2, M_4 absorbs charges Q', as illustrated in Figure 3.2 (b), from parasitic capacitor C_{H1} and $C_{H2,}$ on the node c and d. Thus the charge absorption



(a) Timing of RES, OC_1 and OC_2.



(b) $T_1 < t < T_2$



(c) $T_2 < t < T_3$

Figure 3.2. Mechanism of offset control by charge absorption.

has approximately the same contribution to the potentials on nodes c and d because M_3 is turning on. Assuming the channel transit time for M_4 is long compared to $T_2 - T_1$, the channel of M_4 will be partially depleted during this period. During the period between T_2 and T_3, the latching operation starts as reset transistor M_3 starts being turned off by RES. In the meantime, charge injection and clock feed-through [14] appears on the latching nodes c and d. However, charge injection dominates the effects

on the potentials of the regenerative nodes c and d. Since M_4 is turned on while M_5 remains off in this period, as illustrated in Figure 3.2, some of the charge Q'_{ch1} injected from the channel of M_3 is absorbed by M_4, and the remaining charge Q_{ch1} is deposited by C_{H1} on node c. The charge Q_{ch2} injected from the source of M_3 is not absorbed by M_5 but deposited by C_{H2} on node d. Thus the charge absorption by M_4 in this period contributes to generating a compensation voltage at the initial state of the latch regeneration. Adjusting the phase between T_1 and T_2 controls the amount of the compensation voltage. The period of $T_2 \sim T_4$ is chosen to be long enough comparing to the positive feedback loop time constant. This ensures that the input signal along with the compensation voltage grows enough by the time when M_5 starts to absorb charge from C_{H2} on node d. Thus the charge absorption by M_5 will affect little on the latch output.

Analysis above shows the offset of the comparator can be controlled by timing adjustment of OC_1 and OC_2.

3.2.2 Analysis of Timing Control

Based on the aforesaid mechanism, the timing of signals OC_1 and OC_2 for offset control should be adjusted in time domain in order to let two transistors M_4 and M_5 switch an appropriate manner to allocate the charge injected by M_3 between nodes c and d so as to control the offset. As shown in Figure 3.3, the timing diagram of clock, offset control and output shows how the dynamic offset control technique works. Here, assuming that the comparator has a positive input offset, OC_2 lags OC_1. To train the circuit, inputs are shorted to ground (S1 and S2 turn on in Figure 3.1) and the latching operation is performed over a series of phase steps on signal OC_1 with fixed control

signals OC_2 and RES. When the offset is on cancelled, in theory, the output will remain meta-stable forever. In practice, it latches to opposite states on each side of the phase offset that most closely cancels the offset. The phase offset is then fixed to one of these two values. In the case of negative offset the training operation is the same, but OC_1 lags OC_2.

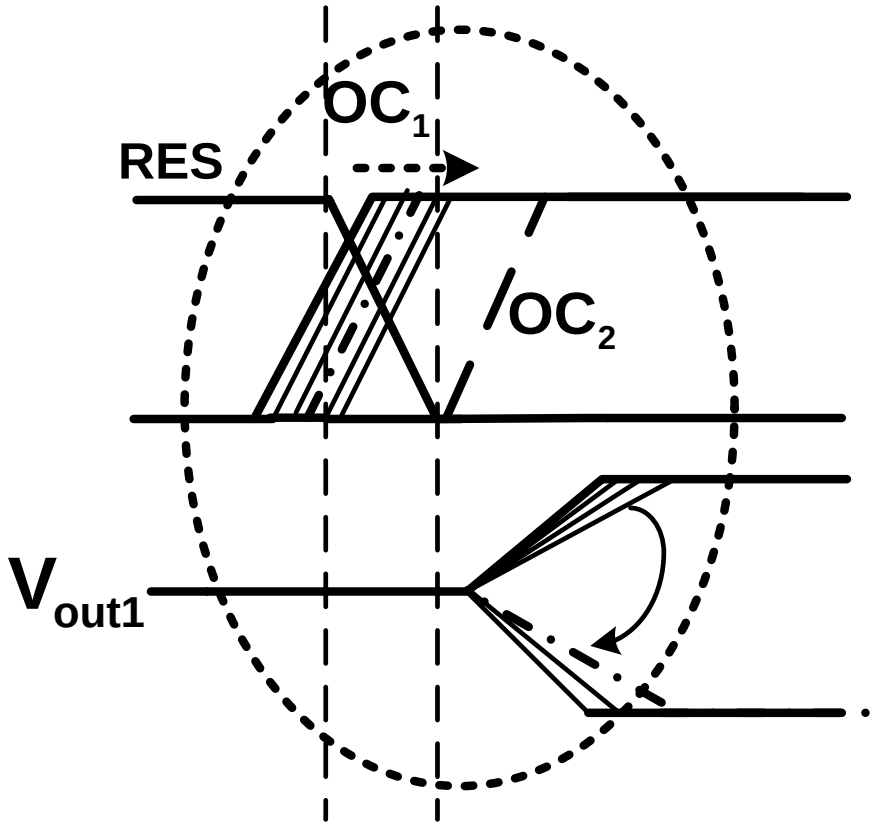


Figure 3.3 Timing diagram of clock, offset control and output.

To confirm the relationship between offset and timing control, we simulated the circuits shown in Figure 3.1, giving 50 mV of input offset to the preamplifier (Gain 3dB), applying ideal timing control signals OC_1, OC_2, and RES which have the same

frequency of 1 GHz and the same typical slew rate of 40V/ns to M_4, M_5, and M_3. The delay between OC_1 and RES, $T_{OC1, RES}$, is swept from 475ps to 495ps in pico-second steps, which let the M_4 turn on slightly before the M_3 turns off. The delay between OC_2 and RES, $T_{OC2, RES}$, is set to 530ps, which guarantees the M_5 turn on after the M_3 completely turns off. As shown in Figure 3.4, the transition appears at the latch output when

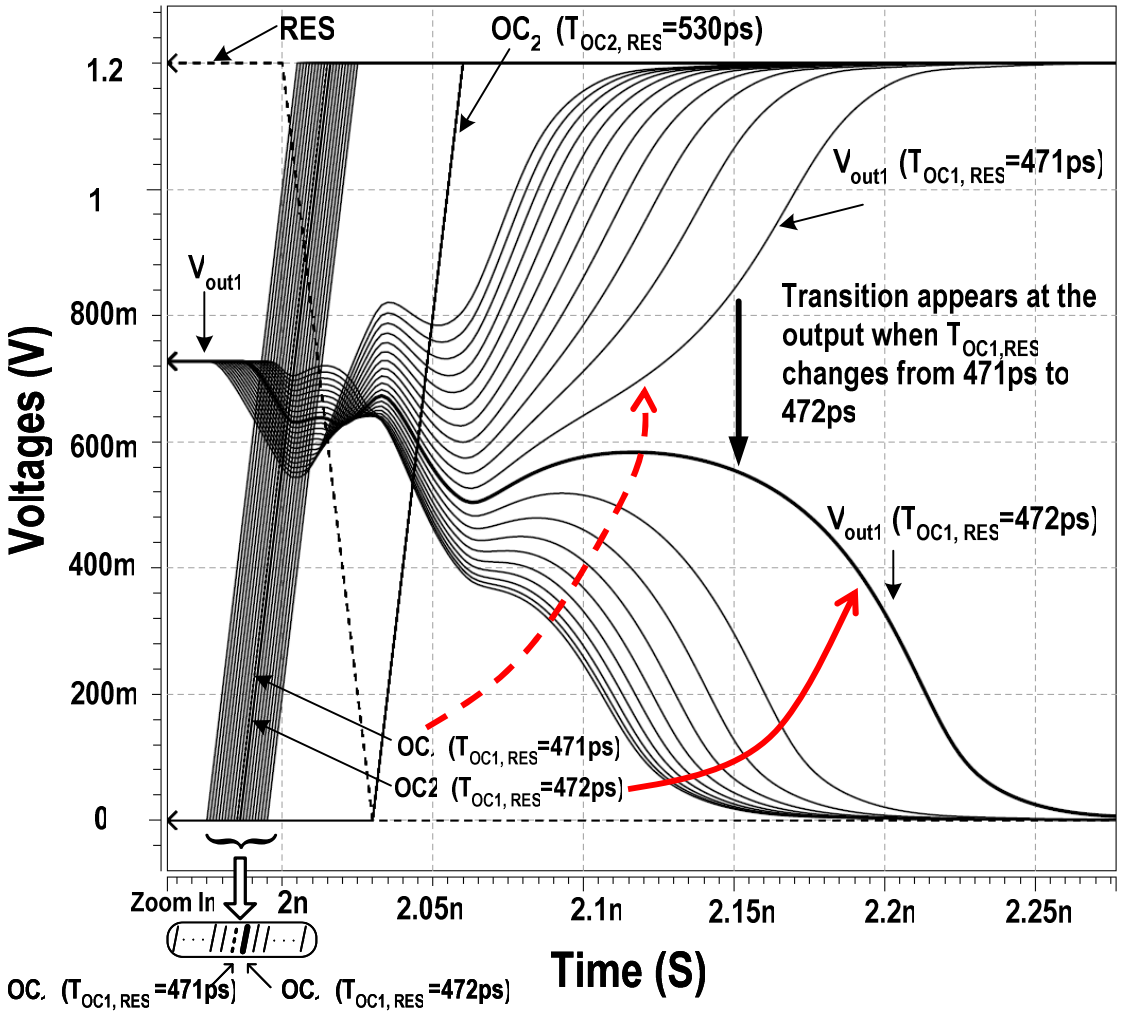


Figure 3.4 Simulation results for offset vs timing control.

$T_{OC1, RES}$ changes from 471ps to 472ps. By changing the input offsets, as well as the slew rates of OC_1, OC_2, and RES, performing the similar simulation as above, we got the relationship between offset and timing control under three different slew rates (12V/ns, 40V/ns, 120V/ns) as illustrated in Figure 3.5. The results show that relationship between offset and timing control is not linear. For example, when the slew rate of the three timing control signals are typical 40V/ns, 1ps generally control 5mV offset while on the margins, 1ps delay control around 1~2mV offset. The different slew rates of the control signals result in different non-linear relationships between the offset and the timing control and the maximum controllable offset voltage as well. For instance, when the slew rate is 120V/ns, 1ps delay is generally able to control 5.5mV offset, while the maximum controllable offset is around 160mV. When the slew rate is 12V/ns, 1ps delay is able to control around 0.83mV offset, while the maximum controllable offset is decreased to 60mV.

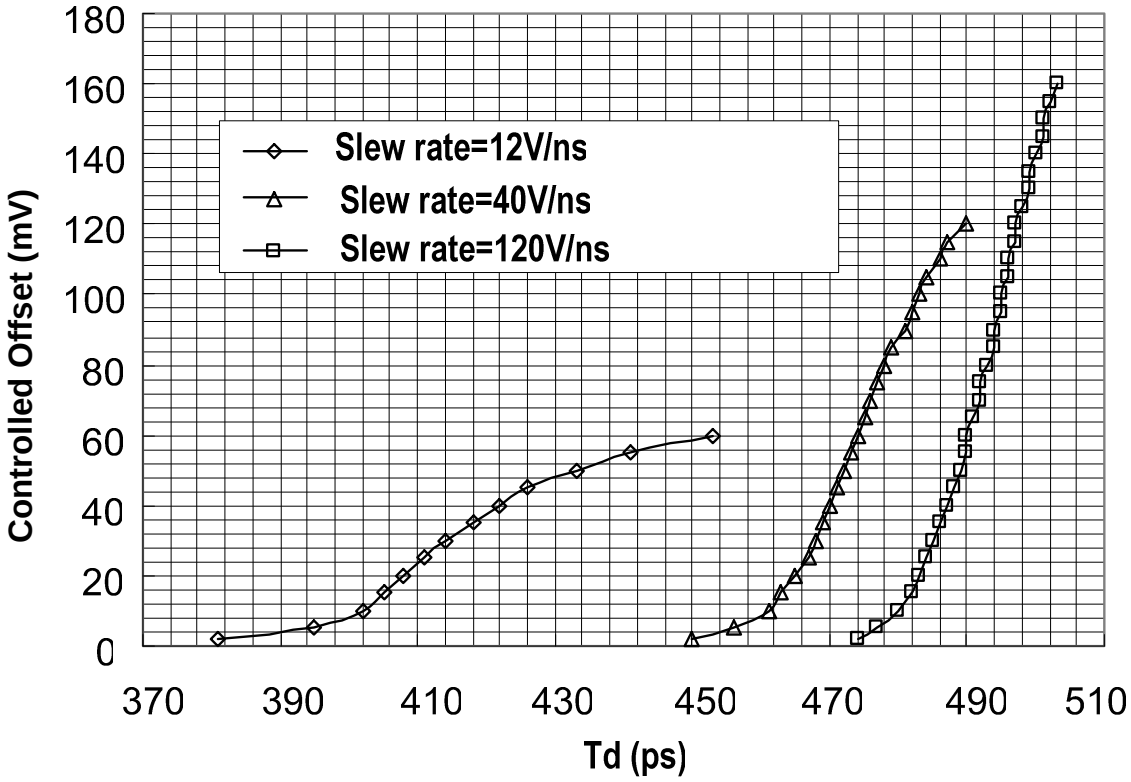


Figure 3.5 Relationship between offset and timing control with different slew rates applied on the timing control signal.

The relationship between offset and T_d shows the offset control has the dependence on the slew rate of RES, OC_1 and OC_2. It results from the fraction of Q_{ch} injected onto the regenerative nodes c and d has the dependency on the slew rate of the clock phase [14]. A function of a switching parameter *B* related to the slew rate α is given by

$$B = V_{ov}\sqrt{\frac{\mu C_{ox} W / L}{|\alpha| C_s}} \tag{3.2}$$

where μ is the mobility of the electrons in the channel and C_s is the sampling capacitance. While in this case, C_s is the parasitic capacitance on one of the regenerative nodes c or d. During the period of charge injection appears on the

regenerative nodes, M_3 starts turning off, M_4 is turned on while M_5 remains off. Based on the study on the charge injection of the S/H circuits in [14], the characteristic for the fraction of the charge injected by switching transistor versus parameter *B* is illustrated in Figure 3.6. The diagrams for small values of *B* account for an injected charge equal to half the channel charge, while for large values of *B* (associated long transition times, small value of α), an injected charge is smaller than half of the channel charge, thus the amount of the compensation voltage is decreased. It further demonstrates the results of relationship between offset and timing control with different slew rates as illustrated in Figure 3.5.

Simulation results in Figure 3.5 also show that the lager the slew rate of the timing control signals are chosen, the lower the requirements for the delay time resolution and the smaller the maximum controllable offset will be.

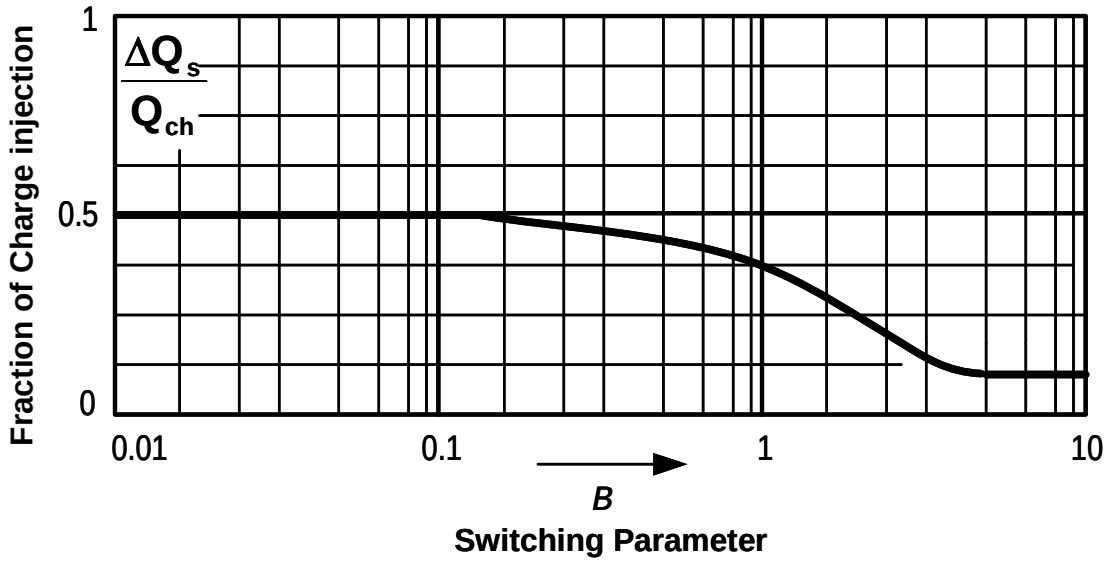


Figure 3.6 Fraction of the charge injected by switching transistor vs *B*

3.2.3 Timing Controller

Based on the timing analysis in section 3.2.2, the dynamic offset control needs to control the timing of OC_1 and OC_2. Figure 3.7 shows an analog-to-timing controller (ATC). Two delay elements (I_2, I_3), two tunable delay elements (I_7, I_8) and four buffers (I_1, I_4, I_5, I_6) are implemented to control The timing of OC_1, OC_2 and RES. In the case of negative offset, OC_1 and OC_2 are swapped.

Although the timing among RES, OC_2 and OC_1 is controlled by implementing analog voltage, it will be feasibly controlled by digital, replacing the M_1 and M_2 in Figure 3.7 with small digitally controlled switches to regulate the current and adjust timing. Such a digital to timing controller could be useful for the real applications.

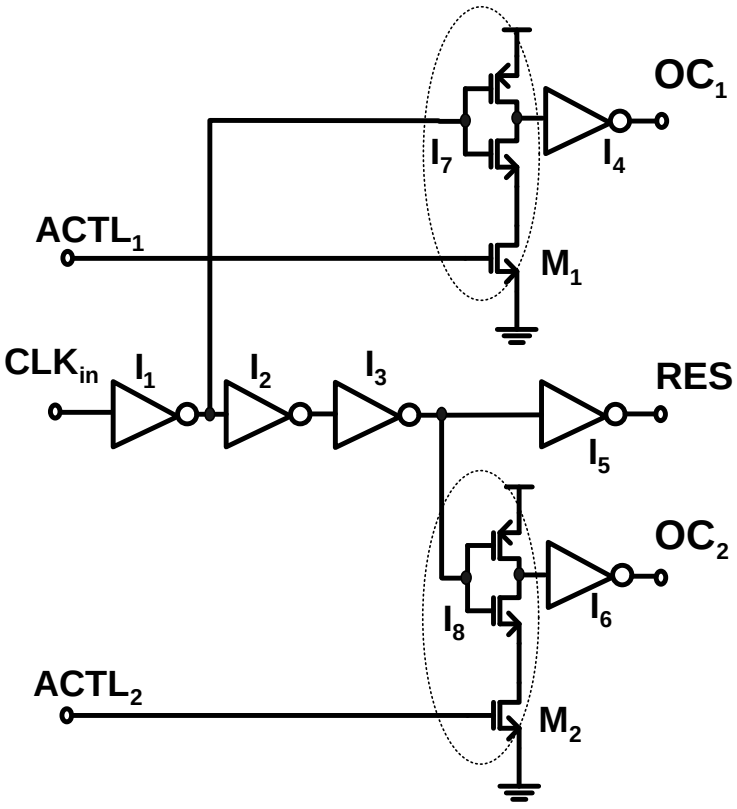


Figure 3.7 Analog-to-Timing Converter.

3.2.4 Simulation Results

Figure 3.8 shows post-layout simulated wave forms with the comparator in Figure 3.1 and the timing controller in Figure 3.7, giving 50mV of input offset to the preamplifier. Gain of the preamplifier is 3dB. $ACTL_2$ is set 550mV to ensure M_5 turns on after M_3 completely turns off. $ACTL_1$ is swept from 0.7V to 1.2V in 10mV steps. By measurement, the slew rate of the clock phase RES is around 15V/ns. The transition appears at the latch output when $ACTL_1$ changes from 860mV to 850mV.

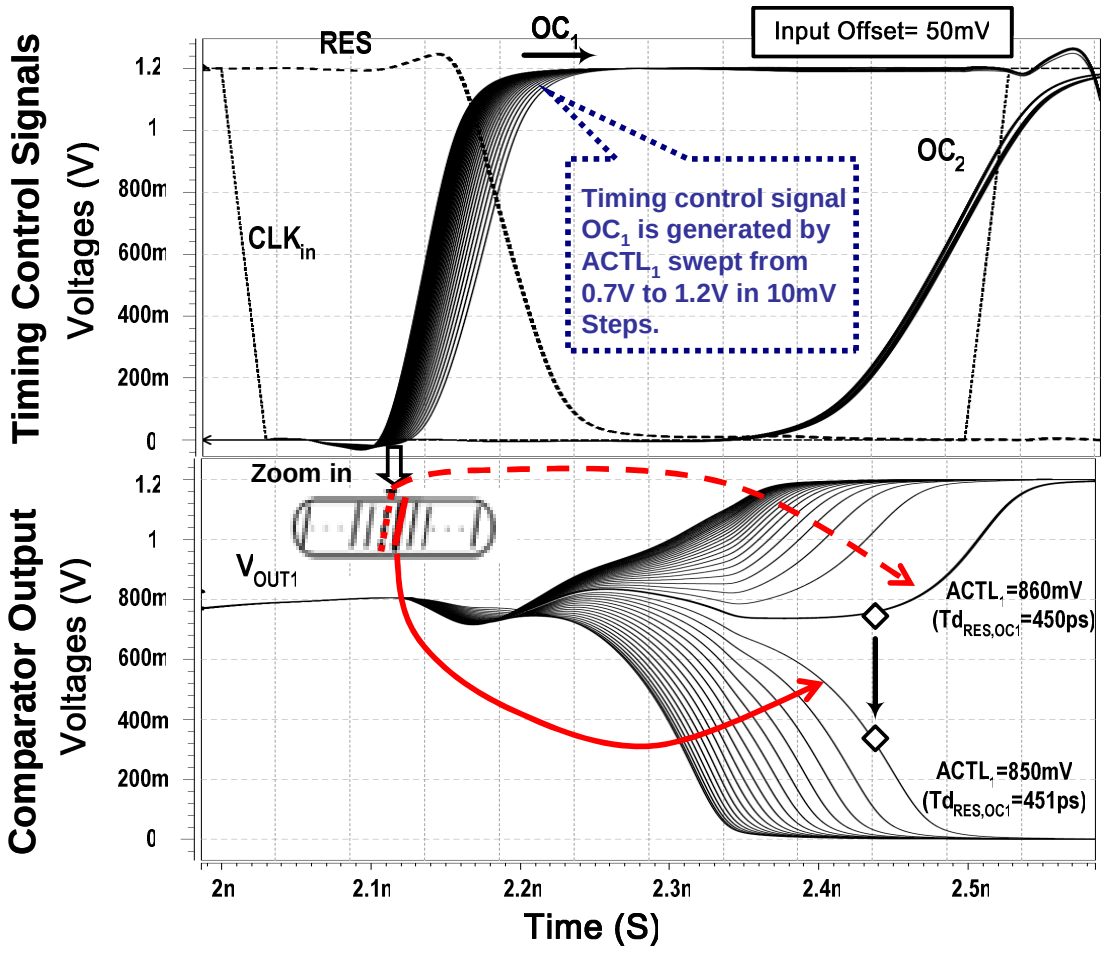


Figure 3.8 Simulation results.

Figure 3.9 shows the relationship between $ACTL_1$ and the input offset, by changing the input offset to the preamplifier. According to this simulated result, 470mV of $ACTL_1$ variation causes OC_1 delay to change by approximately 50ps and 60mV input offset is controlled. The control ratio ($\Delta V_{off}/\Delta ACTL_1$) is 0.127.

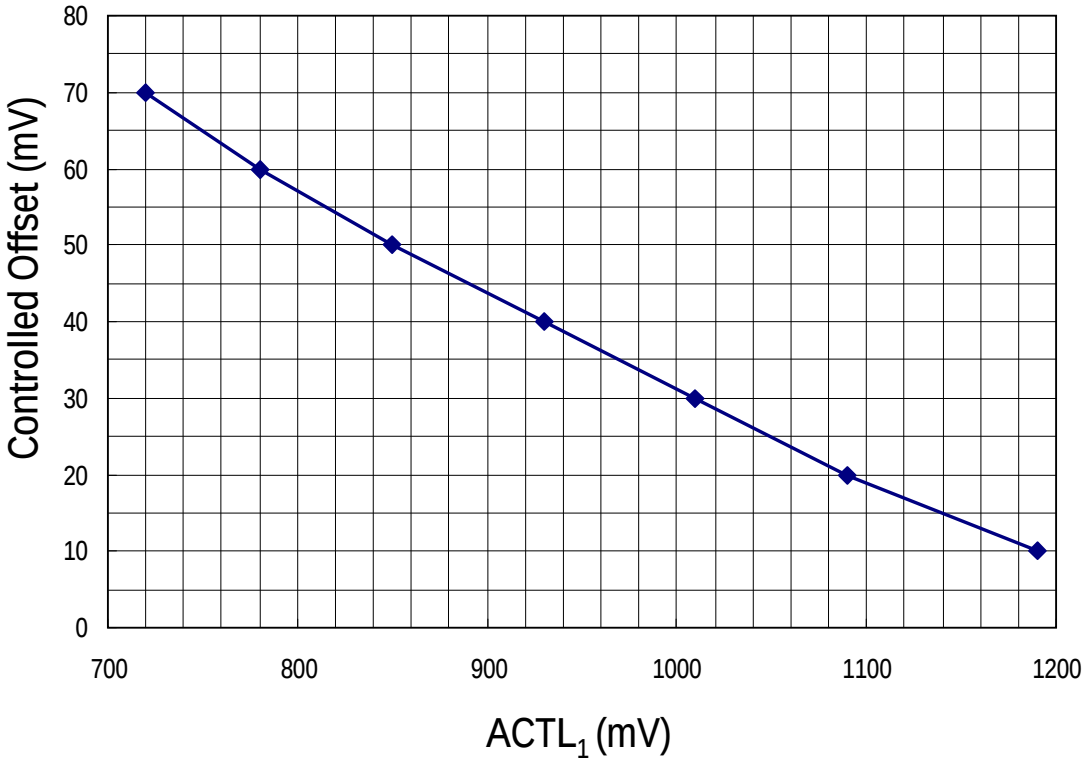


Figure 3.9 Relationship between analog control signal and input offset.

3.3 Experimental Results

Figure 3.10 is a chip photograph of the comparator, including blocks of Figure 3.1, Figure 3.8 and an output flip-flop, fabricated in a 65nm CMOS process. It occupies 25 x 65μm^2 and consumes 380μW under 1.2V power supply.

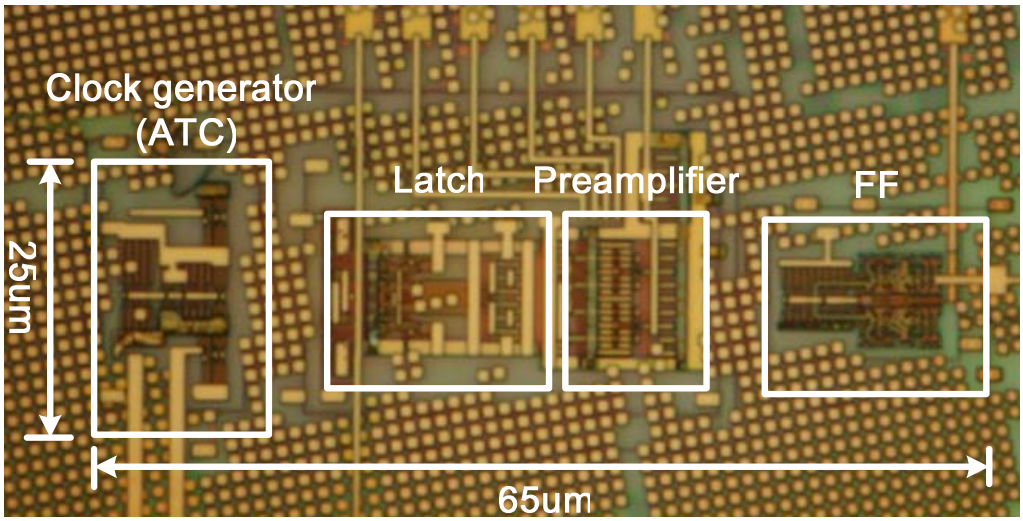
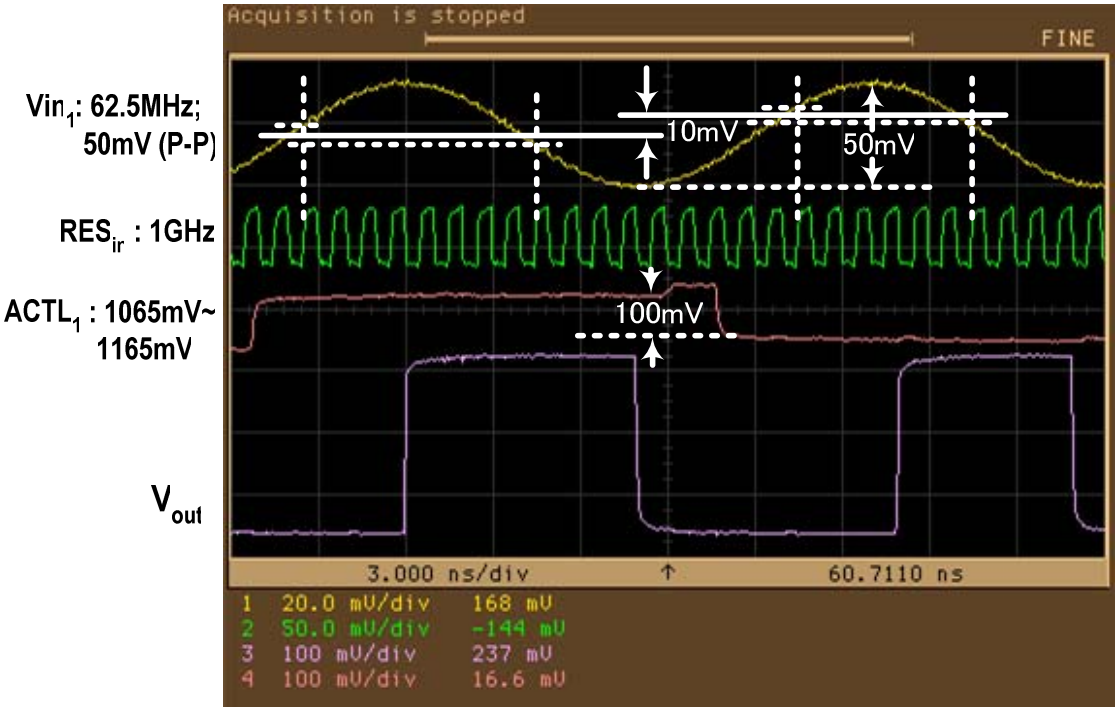


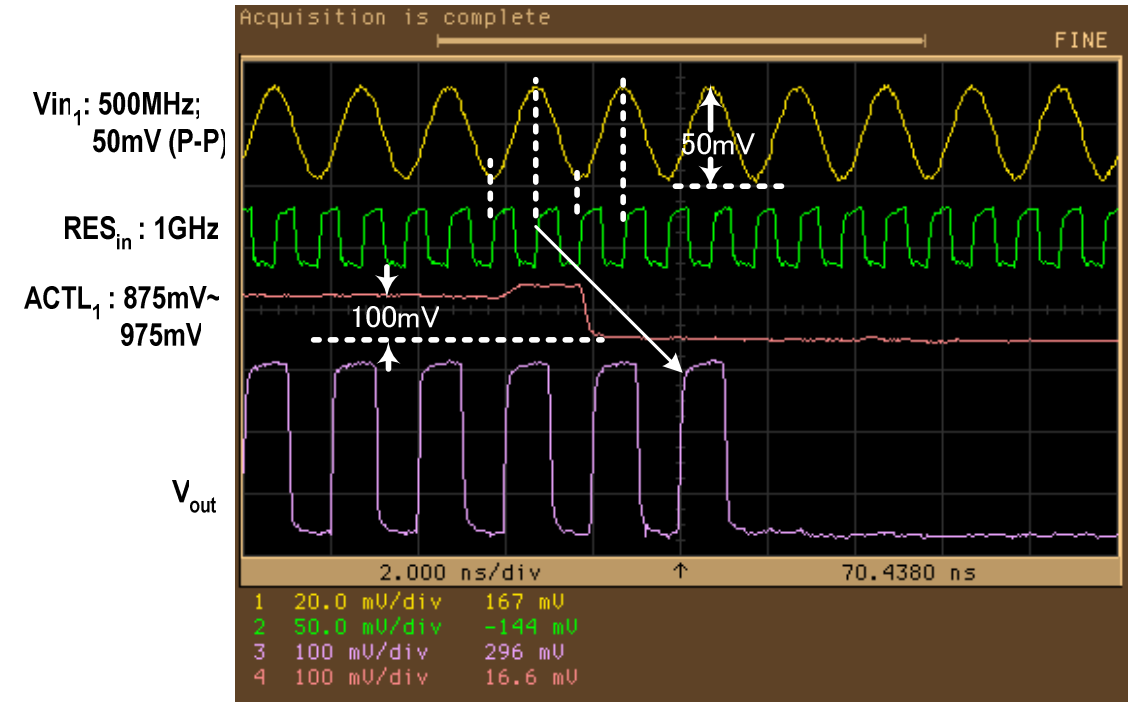
Figure 3.10 Photograph of the comparator test die.

Figure 3.11 (a) shows the threshold level of the comparator response at 1GS/s with 1.2V power supply. $ACTL_1$ is controlled with a 100mV gap. Analog signals are acquired at the rising edge of the clock. An offset of 10mV is controlled by 100mV of $ACTL_1$ variation. Figure 3.11 (b) also shows a response with a 500 MHz analog input frequency, synchronized to the 1GHz clock. The analog signal is acquired at the top and bottom voltage and their outputs are compared. 100 mV of $ACTL_1$ variation controls the threshold level of the comparator to be higher than the top of analog signal. So after the transition of $ACTL_1$ is on lower level, the comparator output is fixed to low. This means the analog signal is lower than reference revel.

Figure 3.12 shows the relationship between $ACTL_1$ and the input offset. The control ratio is 0.104 which means 1mV offset can be controlled by 10mV of $ACTL_1$. It is well balanced between the controllable range and resolution to control several tens of mV offset with mV order accuracy. There is 23% mismatching between post-layout simulation and the actual performance which is mainly caused by the decreasing of the



(a)



(b)

Figure 3.11 Oscilloscope photographs of typical waveforms for input offset control test.

slew rate of the clock signal which has been explained with Figure 3.5 in section 3.2.2. Mismatch also suffers from the process variation of the parasitic on nodes c and d, and modeling of the elements.

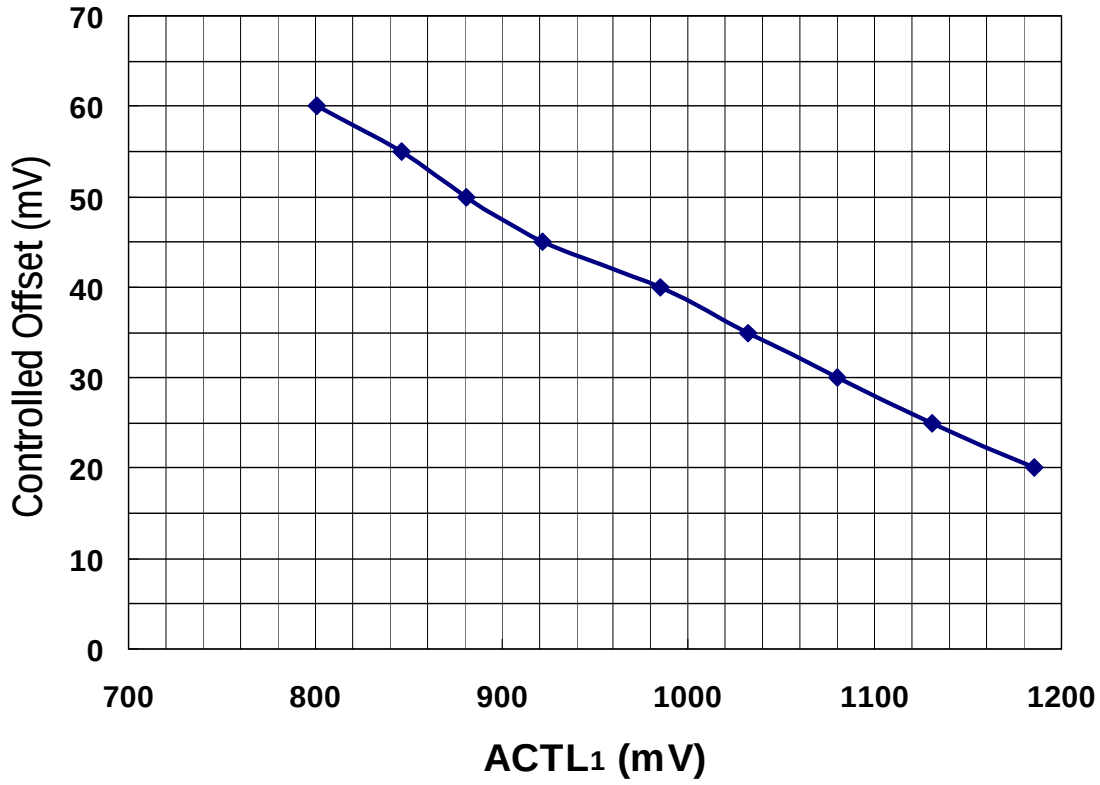


Figure 3.12 Relationship between control signal and input offset based on dc measurement results.

3.4 Conclusion

This work explores a dynamic offset control technique that employs charge compensation by timing control. The charge injection and clock feed-through by turning off the latch reset transistor are investigated. A simple method is proposed to generate offset compensation voltage by implementing two source-drain shorted

transistors on each regenerative node with timing control signals on their gates. The principle of timing based charge compensation approach for comparator offset control is described. The relationship between the offset control and slew rate of the timing control is analyzed based on simulation results. Proposed technique is confirmed by a 1GHz comparator fabricated in 65nm CMOS with 1.2V power supply. Proposed timing based dynamic offset control technique has also been utilized by designing a 9-bit 50MHz split CDAC based SAR ADC with a foreground calibration [15].

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Chapter 4 Design of A 9-bit 100MS/s SAR ADC with Digitally Assisted Background Calibration

4.1 Introduction

Charge redistribution based capacitor DAC (CDAC) is widely used for SAR ADCs because of its superior response to resister DAC (RDAC). CDAC needs to be designed large enough capacitance against thermal noise, as well as the mismatch of each unit capacitors. However, implementing large capacitor array means increased cost and large input capacitance which will decrease the conversion speed. Split CDAC is one of the solutions for both area efficiency and decreasing the input capacitance. However, the nonlinearity induced by the mismatch between MSB-side and LSB-side CDAC array limits the accuracy of a split CDAC based SAR ADC. Therefore, the calibration technique is required for most of the ADC blocks. Analog calibration techniques [1], [2] use analog components in the signal path to generate higher linearity at the expense of conversion speed. On the other hand, digitally assisted calibration techniques, which compensate for ADC mismatch, are reported [3], [4]-[7], [15]. For example, [4], [7] compensate the CDAC linearity, but they need offset free comparator. Comparator offset cancel scheme is implemented to compensate for CDAC linearity which increase the hardware complexity and reduce the calibration efficiency. [8] can correct the linearity as well as radix error, but it needs two times conversion, resulting in the conversion rate into half. The trade off between compensated performance and the costs, area, power, sacrificed performance and convergent time, needs to be considered. Therefore, low cost, high efficient calibration technique is always challenging for the industry in SAR ADC design.

In this chapter, an on chip histogram-based digitally assisted technique is proposed to compensate for CDAC mismatch with a minimum cost. The calibration is performed

using the input signal, watching the data stream to find the missing or wide code at ADC output, judge and feed back to the compensation capacitor so as to relax the nonlinearity suffer from the CDAC mismatch. The calibration does not require special input signal and extra analog hardware and offset-free comparator as well.

4.2 Architecture of ADC with Calibration

As shown in Figure 4.1, the ADC consists of a tri-level charge redistribution CDAC [5], a comparator, SAR control logic and a digital background calibration block. The DAC are implemented as split capacitor arrays (4-bit + 4-bit) for small area and input capacitance. A bridge capacitor C_B connects the top plates of the MSB-side and LSB-side capacitor arrays. The bottom plates of the differential capacitor arrays are connectable with each other so that the tri-level charge redistribution can be achieved by passive charge sharing. The tri-level technique makes it possible for the ADC to achieve 9-bit resolution with the 4-bit + 4-bit capacitor arrays. The system clock CLK defines the sampling phase. The comparator is triggered by an internal asynchronous clock ICLK, which is generated by detecting the outputs of the comparator. The bottom plate of each capacitor in CDAC array is switched by the DI control signal which is generated by the SAR logic. The mismatches between the MSB-side and LSB-side capacitor arrays due to process variation and parasitic capacitance are compensated by a tunable capacitor C_C implemented in parallel with the LSB-side array. Calibration block watches the output data stream to find the wide or missing code at ADC output, judge and feed back a controlling signal CI to the variable compensation capacitor C_C. The calibration scheme will be discussed in detail in section 4.3.

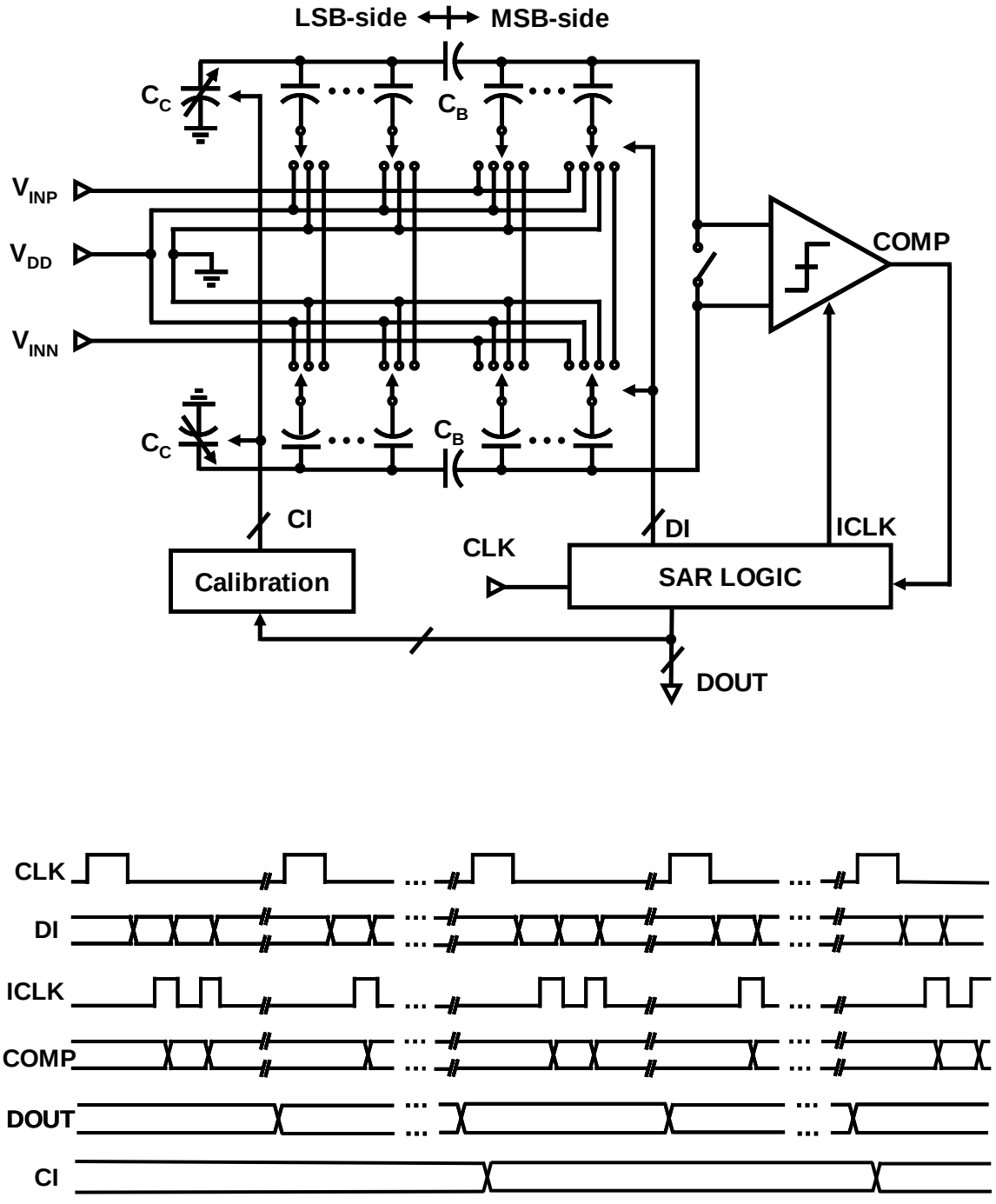


Figure 4.1 Architecture of ADC with Calibration.

4.3 Circuits Implementation

4.3.1 CDAC

A tri-level charge redistribution CDAC utilizing the passive charge sharing technique which is shown in Figure 4.1. During the sampling phase, the bottom plates of differential capacitor array (MSB-side) are disconnected from each other and connected to the input voltage V_{IN}. After the top plates become floating, the bottom plates of the two differential capacitor array (MSB-side) are disconnected from the inputs and all capacitor arrays are connected with each other through switch arrays. Then conversion starts with the most significant bit (MSB) estimation. The bottom plates charge sharing achieves voltage averaging by switching all capacitor bottom plates from V_{IN} to 1/2 V_{DD}, the middle point level of input differential pair, which is given 1/2 V_{DD}. Therefore the input is compared to the 1/2 V_{DD} and the MSB bit estimation is made. Then the bottom plate of the second bit of the capacitor array is switched from 1/2 V_{DD} to V_{DD} or Gnd based on the first bit decision, thus the input is compared to 1/4 V_{DD} or 3/4 V_{DD} and the second bit estimation is achieved. The conversion process continues on with the remaining capacitors so that the voltage on the top plate of the array, V_{TOP}, is close to the value of the offset voltage, V_{OS} (within the resolution of the ADC).

4.3.2 Histogram based digitally background calibration

The nonlinearities suffer from the mismatch of the split CDAC array will degrade the ADC performance. To simplify the analysis, single-ended tri-level charge redistribution CDAC with calibration is shown in Figure 4.2. Except for the parasitic capacitance C_{P1} and C_{P2}, all the other capacitors are considered to be ideal. A tunable capacitor C_C is

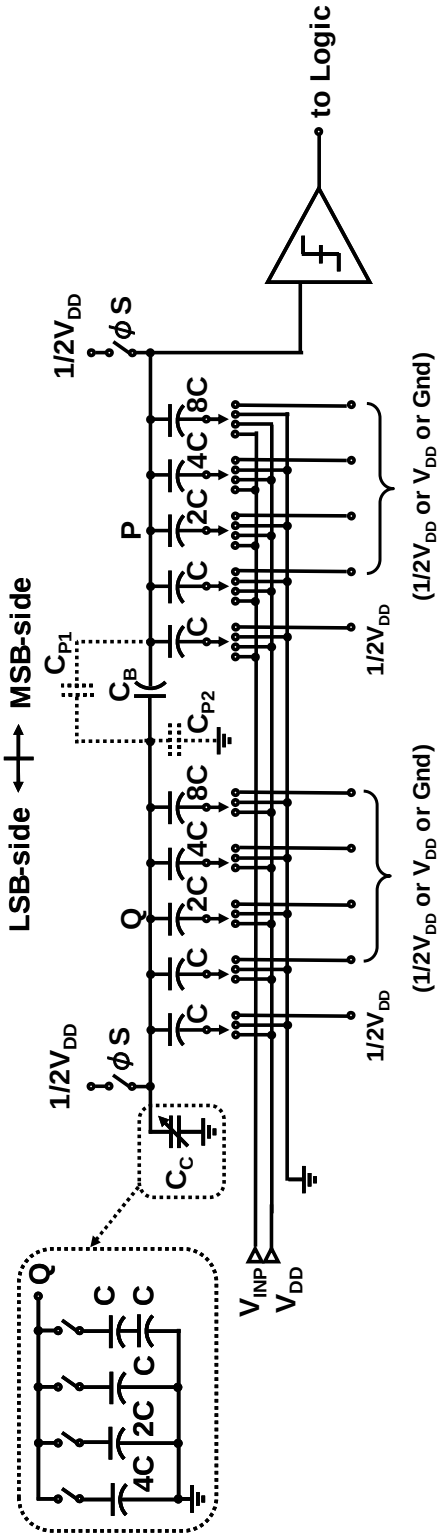


Figure 4.2 Tri-level charge redistribution CDAC (single-ended).

implemented in parallel with the LSB-side CDAC array to compensate the mismatch between MSB-side and LSB-side capacitor array. During the sampling period, since the bottom plates of MSB-side CDAC array are applied with analog inputs, and LSB-side CDAC array is biased to common mode voltage V_{CM} level, which is $1/2V_{DD}$, the charge stored on node P and Q can be expressed with Eq. (4.1) and (4.2) respectively,

$$Q_P = 16C \cdot (V_{IN} - \frac{1}{2}V_{DD}) \tag{4.1}$$

$$Q_Q = (C_C + C_{P2}) \cdot (0 - \frac{1}{2}V_{DD}) \tag{4.2}$$

After the conversion for a sample is completed, the charge is redistributed onto the capacitors with their bottom plates connected to V_{DD}, Gnd or 1/2 V_{DD}. At this moment, the voltage level of the top plate on the MSB-side array returns back to V_{CM}, and that of the LSB-side array is an uncertain voltage level V_Q. So the charges on node P and Q are expressed as,

$$\begin{aligned} Q_P' = {} & (8C \cdot D_8 + 4C \cdot D_7 + 2C \cdot D_6 + C \cdot D_5) \cdot V_{DD} - (8C + 4C + 2C + C) \cdot \frac{1}{2}V_{DD} \\ & + (C_B + C_{P1}) \cdot (V_Q - \frac{1}{2}V_{DD}) \end{aligned} \tag{4.3}$$

$$\begin{aligned} Q_Q' = {} & (8C \cdot D_4 + 4C \cdot D_3 + 2C \cdot D_2 + C \cdot D_1 + \frac{1}{2}C \cdot D_0) \cdot V_{DD} \\ & - (8C + 4C + 2C + C + C) \cdot V_Q \\ & + (C_C + C_{P2}) \cdot (0 - V_Q) + (C_B + C_{P1}) \cdot (\frac{1}{2}V_{DD} - V_Q) \end{aligned} \tag{4.4}$$

Where D_i is the binary code represents the comparator's output. Since the charges on node P and Q should keep constant respectively, that are,

$$Q_P = Q_P' \tag{4.5}$$

$$Q_Q = Q_Q' \tag{4.6}$$

Combing Eq. (4.1) ~ (4.6), and let $\varepsilon = \frac{16 \cdot (C_B + C_{P1})}{16C + C_B + C_{P1} + C_{P2} + C_C}$, V_{IN} can be simplified and written as,

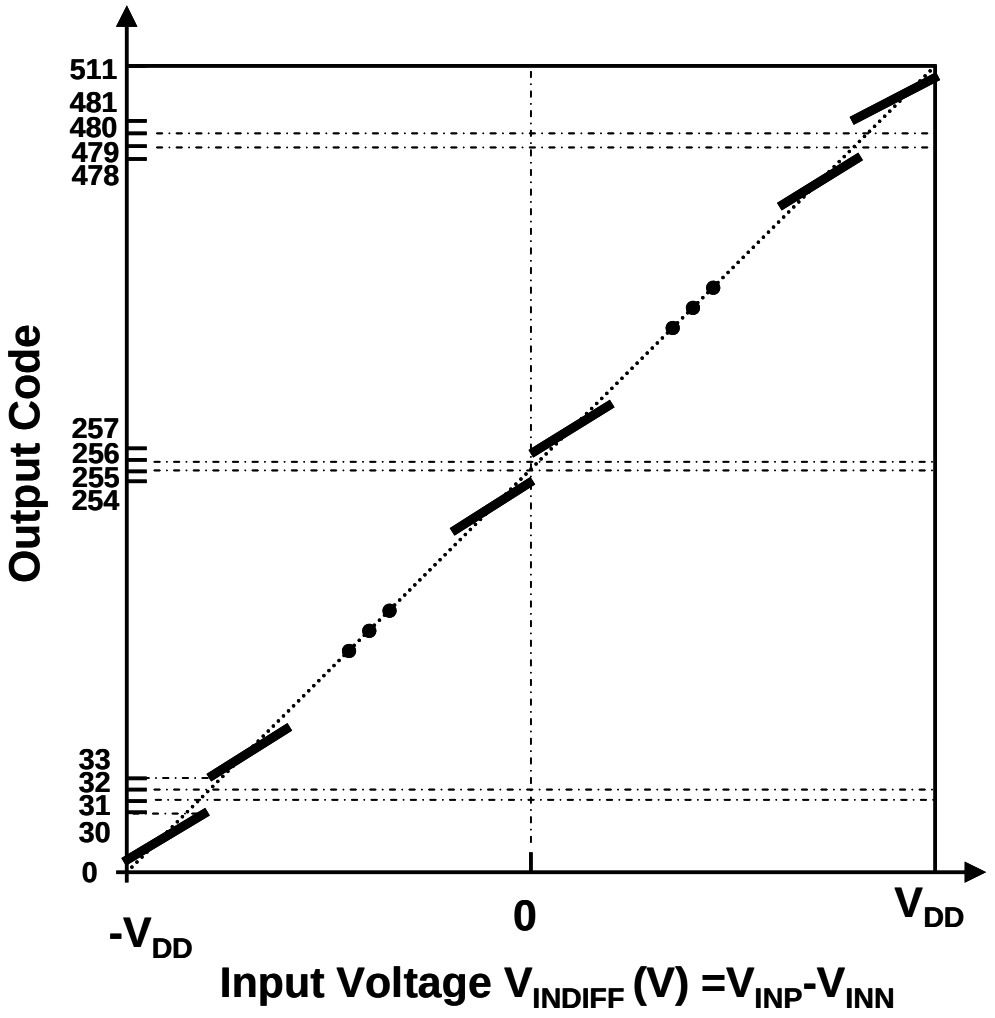
$$\begin{aligned} V_{IN} = {} & \frac{1}{2} D_8 \cdot V_{DD} + \frac{1}{2^2} D_7 \cdot V_{DD} + \frac{1}{2^3} D_6 \cdot V_{DD} + \frac{1}{2^4} D_5 \cdot V_{DD} \\ & + \varepsilon \cdot \left(\frac{1}{2^5} D_4 \cdot V_{DD} + \frac{1}{2^6} D_3 \cdot V_{DD} + \frac{1}{2^7} D_2 \cdot V_{DD} + \frac{1}{2^8} D_1 \cdot V_{DD} + \frac{1}{2^9} D_0 \cdot V_{DD} \right) \\ & + \frac{1}{32} (1 - \varepsilon) \cdot V_{DD} \end{aligned} \tag{4.7}$$

The Eq. (4.7) shows the single-ended mode and the last term in the equation would be cancelled in differential mode which is shown in Eq. (4.8).

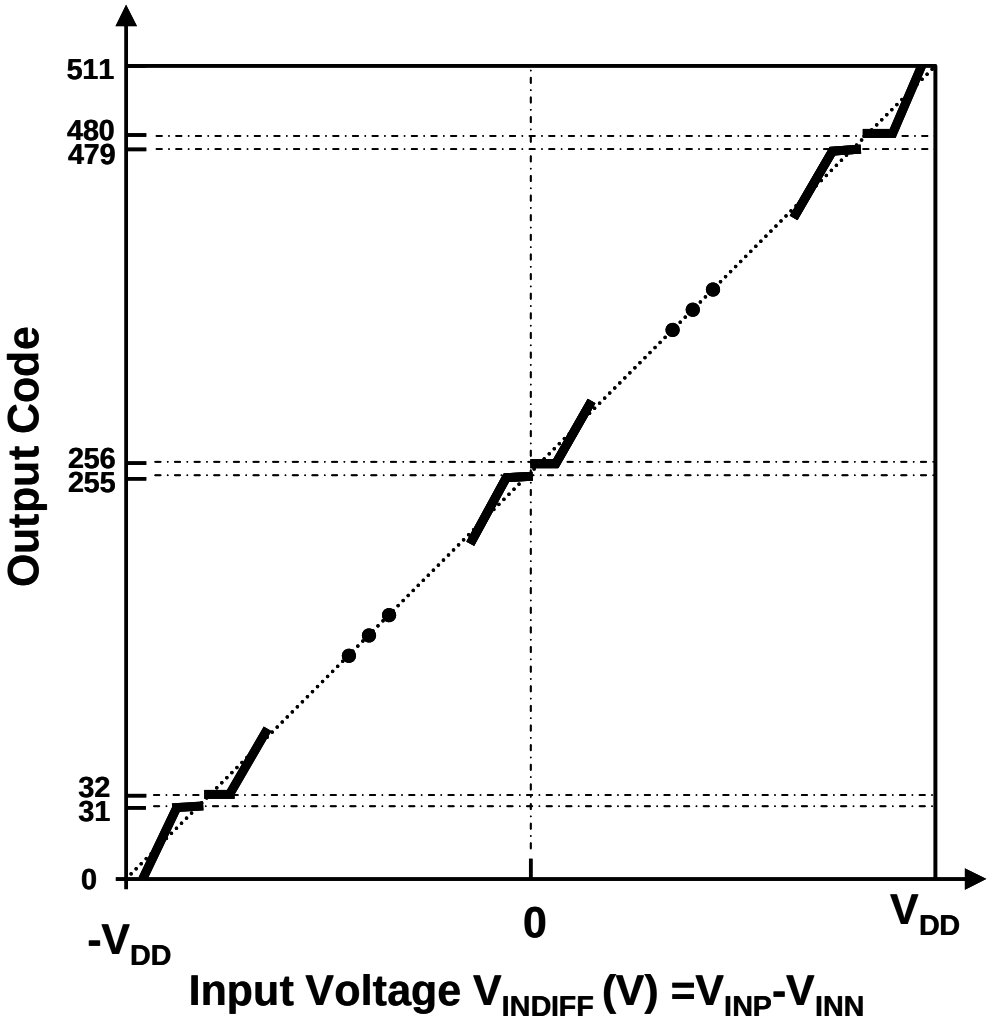
$$\begin{aligned} V_{INDIFF} = V_{INP} - V_{INN} = {} & \frac{1}{2} (D_8 - \overline{D_8}) \cdot V_{DD} + \frac{1}{2^2} (D_7 - \overline{D_7}) \cdot V_{DD} + \frac{1}{2^3} (D_6 - \overline{D_6}) \cdot V_{DD} \\ & + \frac{1}{2^4} (D_5 - \overline{D_5}) \cdot V_{DD} + \varepsilon \cdot \left[\frac{1}{2^5} (D_4 - \overline{D_4}) \cdot V_{DD} + \frac{1}{2^6} (D_3 - \overline{D_3}) \cdot V_{DD} \right. \\ & \left. + \frac{1}{2^7} (D_2 - \overline{D_2}) \cdot V_{DD} + \frac{1}{2^8} (D_1 - \overline{D}_1) \cdot V_{DD} + \frac{1}{2^9} (D_0 - \overline{D_0}) \cdot V_{DD} \right] \end{aligned} \tag{4.8}$$

The nonlinearity results from missing or wide code appears periodically in ADC transfer function when $\varepsilon \neq 1$, which is shown in Figure 4.3. Due to the differential architecture and also based on Eq. (4.8), symmetric wide codes or missing codes will appear on the waveform separated by every 32-code. The target of calibration is to remove the missing code gap or the wide code region at the bit boundary by tuning the value of compensation capacitor C_C so as to have ε equal to 1. [5] proposed a CDAC

mismatch calibration technique, however it needs an offset free comparator. Although only two missing codes appear periodically at the bit boundary as shown in Figure 4.3(a), in reality, more than two missing codes might appear if the ε is much larger than 1. Figure 4.4(a) and (b) show example of histogram collected when ε>1 and ε<1 while the input voltage V_{IN} is uniformly distributed in the missing code or wide code region near the bit decision boundary.

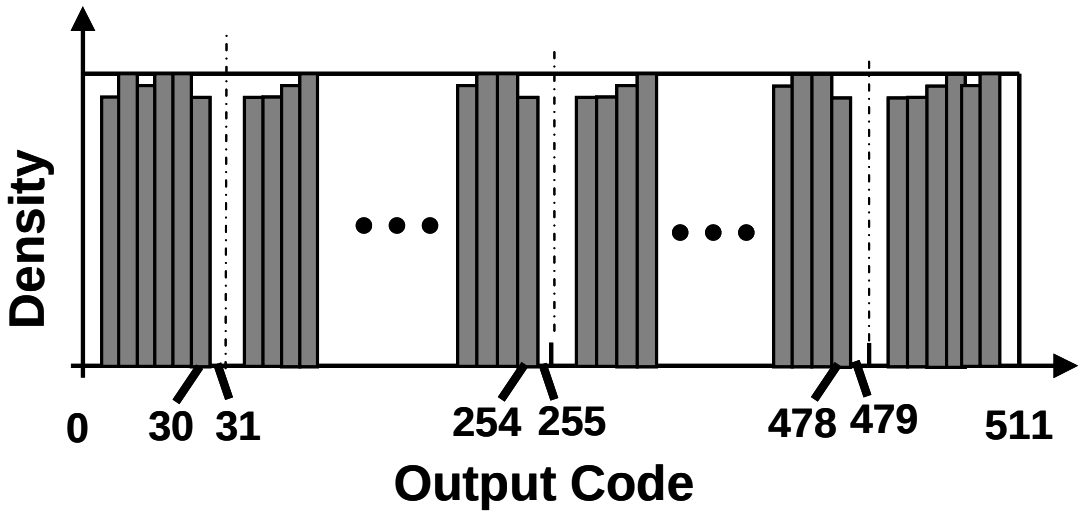


(a) Missing code error (ε>1)

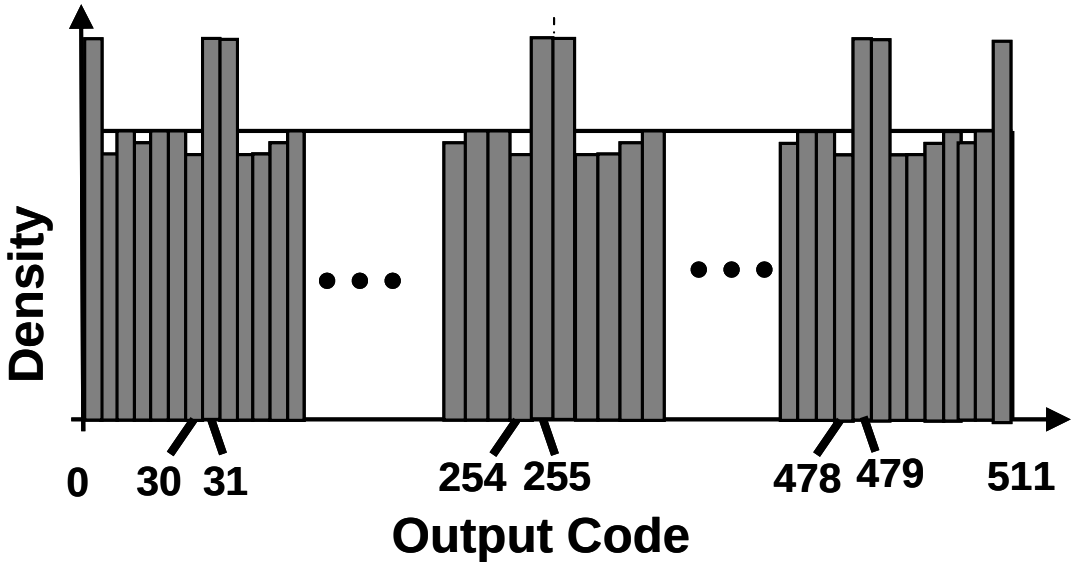


(b) Wide code error (ε<1)

Figure 4.3 ADC transfer function from mismatch of CDAC.



(a) Missing code error (ε>1)



(b) Wide code error (ε<1)

Figure 4.4 Histogram of an example data set from mismatch of CDAC.

In the case of wide code error illustrated in Figure 4.4(b), the code density of the last 5-bit of “11111” is much larger than that of “11110”. The calibration tries to

remove the difference of code density between these two neighborhoods and produce a desirable histogram with uniform code density.

The calibration scheme utilizes a simple algorithm and the procedure is described as follow:

The compensation capacitor C_C is initially set the largest value within its tunable range to make sure the wide code region will appear firstly since the total weight of the LSB-side array is initially smaller than that of the LSB of the MSB-side array.

Receive a block of N samples from ADC;

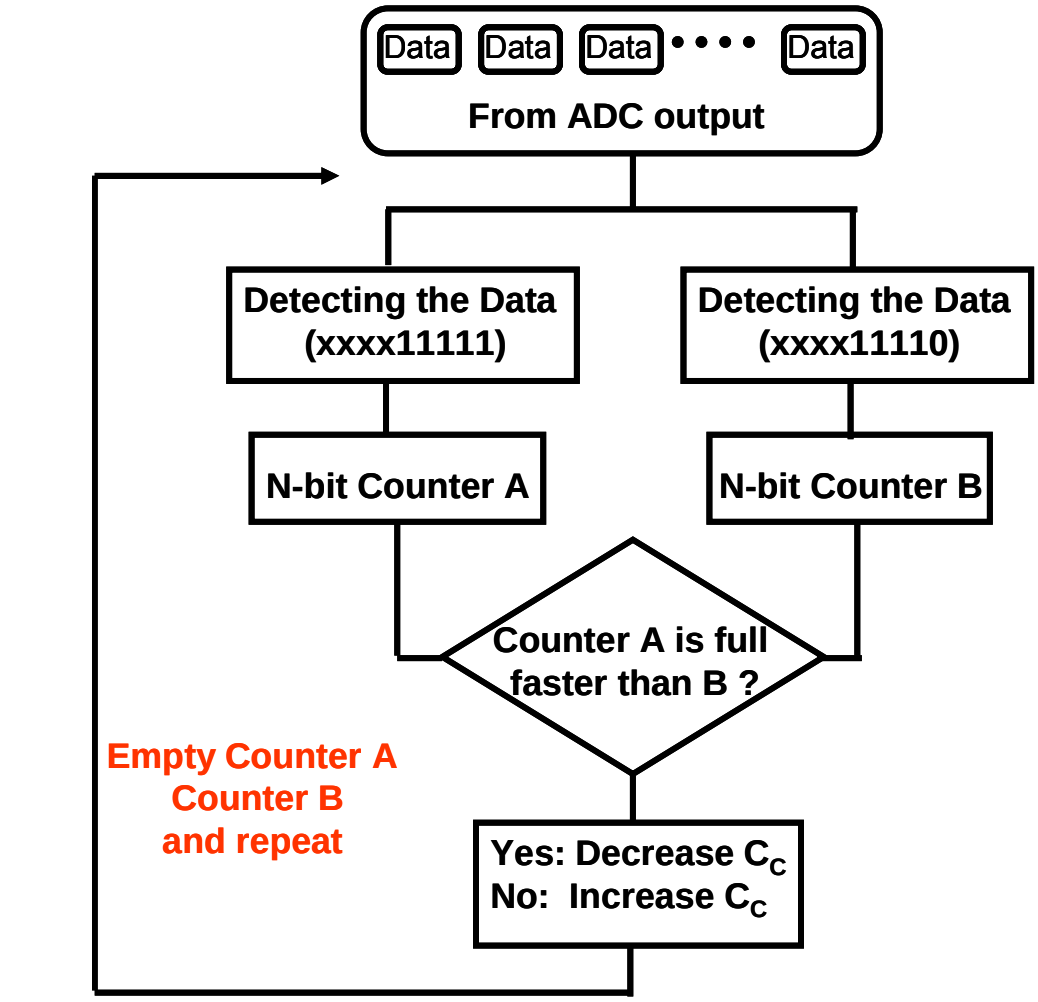
Split it into two sets X_A and X_B. X_A is the set of all samples whose last 5-bit are "11111" and X_B is the set of samples whose last 5-bit are "11110";

Fill the two different sets of examples X_A and X_B into two bins A and B with the same capacity;

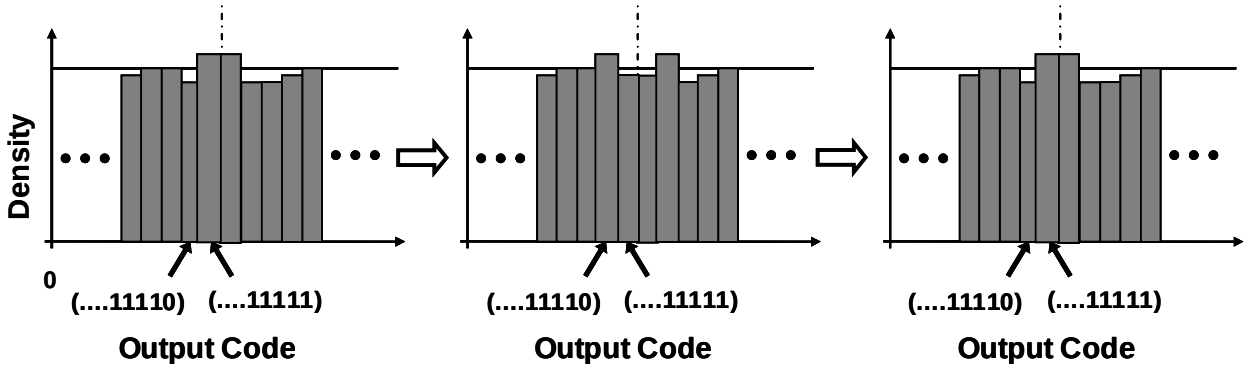
If bin A fill the full range up faster than bin B, a "count down" signal is generated and feeds back to control logic to decrease C_C so that the weight of the LSB-side array becomes larger;

Empty both bin A and B, and repeat from 2) to5).

In other words, calibration block watch the data stream at the decision boundary to find out whether the number of set of samples whose last 5-bit are "11111" is more likely lager than that of samples whose last 5-bit are "11110", which means the wide code nonlinearity caused by mismatch of CDAC need to be calibrated. Ideally, calibration process repeats until the bin A and B gets filled up simultaneously. However, in practice, the calibration ends up with a meta-stable status which can be



(a)



(b)

Figure 4.5 Calibration flow chart and histogram of an example data set after calibration (wide code calibration).

described with a sample histogram as depicted in Figure 4.5. The bin A and its neighbor bin B take turns at getting faster filled full range up with either the sample X_A (last 5-bit "11111") or the sample X_B (last 5-bit "11110"). The difference of code density between bin A and B at this meta-stable status should meet the requirement from the resolution of ADC. Qualitatively, the more likely the input signal is to exercise the codes at the decision boundary, the better this calibration performs and vice versa. How quickly the calibration converges also depends on the probability density in the region of the decision boundary which means the optimal calibration has dependence with the input signal and capacities of the bin.

On the other hand, calibration is possible to perform based on missing code error. The procedure is described as follow:

The compensation capacitor C_C is initially set the smallest value within its tunable range to make sure the missing code gap will appear firstly since the total weight of the LSB-side array is initially larger than that of the LSB of the MSB-side array.

Receive a block of N samples from ADC;

Split it into two sets X_A and X_B. X_A is the set of all samples whose last 5-bit are "11111" and X_B is the set of samples whose last 5-bit are "01111";

Fill the two different sets of examples X_A and X_B into two bins A and B with the same capacity;

If bin B fill the full range up faster than bin A, a "count up" signal is generated and feeds back to control logic to increase C_C so that the weight of the LSB-side array becomes smaller;

Empty both bin A and B, and repeat from 2) to5).

Instead of using “11110” and “11111”, missing code based calibration uses “01111” and “11111” as sets of sample. This is because missing code gap might be larger than two codes distance if the weight of the LSB-side array is much larger than that of the LSB of the MSB-side array, which is difficult to estimate before calibration. In the case of example histogram for missing code, the initial code density for samples whose last 5-bit are “11110” and “11111” are possibly being both zero. This means the calibration will not work any more if “11110” and “11111” are selected to be comparison samples. The alternative candidates are “01111” and “11111”, which have a 16-code distance. However, compared to the wide code based scheme using “11110” and its neighborhood “11111” as two comparison samples, missing code based scheme using samples with long distance of code results in less probability the input signal exercising the codes uniformly at either of the desired boundary region. This means the scheme is further dependent on the input signal which probably results the calibration inefficiency.

To achieve a successful calibration by proposed technique, careful estimation for the parameters such as bridge capacitor C_B, variable compensation capacitor C_C, and the range of ε will be needed. The value of parasitic capacitor C_{P1} and C_{P2} can be found and estimated from device parameter. The value of bridge capacitor C_B is designed to be slightly larger than the ideal fractional value (16/15) C which has been explained in reference [4]. In this work, the C_B is set to be 1.4C. Let ε=1, then the desired value for compensation capacitor C_C (center value of variable C_C) can be calculated. The adjustment range of C_C is designed to be 8C with a minimum step value of 0.5 C. Post-layout simulation is performed to confirm the estimation. The wide code and missing

code appear when the C_C varies from 8 C to 0. By calculation, the range of ε is from 0.87 to 1.15 which can cover a wide enough calibration range.

The proposed wide code based calibration scheme has an efficient implementation in either software or hardware. Figure 4.6 illustrates the circuit diagram of calibration block. Elements I_1 and I_2 are code selectors which select the samples whose last 5-bit are either "11111" or "11110" from the ADC output. I_4 and I_5 are 9-bit asynchronous counters which the clock input are connected with the outputs of I_1, I_2 and I_3 (a divided by four circuit) through a AND gate. The significant bits of I_4 and I_5 are connected with two stages of flip-flop (FF) registers and used as clock signals for a 4-bit down/up counter I_6 which is shown in Figure 4.7. I_6 is a counter that can change state in either direction, under the control of an up/down selector input. The counter I_4 or I_5 increment its value when the clock inputs fed from the outputs of AND gate transiting from 0 to 1. I_4 and I_5 are reset one clock cycle after the significant bit of their outputs D_{A8} or D_{B8} become high level. In the meanwhile, D_{A8} and D_{B8} are used to control the down/up counter I_6. The output state of the I_6 is initially set "1111". If D_{A8}=1 and D_{B8}=0, the I_6 decrements its value once; if D_{A8}=0 and D_{B8}=1, the I_6 increments once. Then the calibration code produced by I_6 feeds back to the compensation capacitor C_C to decrease or increase its value. Notice that there are more than two clock cycle duration between down/up counter I_6 and counter I_4, I_5. An error calibration code will be possibly produced if the clock inputs for I_4 and I_5 are synchronized with the same as the sample clock. A divide-by-four circuit I_3 is implemented to create quarter frequency of the sample clock to avoid such undesirable circumstance. Another issue needs considering is the case when calibration exceeds the specified range suffers from additive circuit noise and the other un-expectable noise in the analog processing path.

The desired calibration code is within the range from “1111” to “0000”, however, it is possible that the calibration code become “0000” or “1111” before achieving a successful calibration. Further increment or decrement in the down/up counter I_6 will generate a wrong calibration code. The circuits as shown with dash frame in Figure 4.7, is implemented to keep the code of “0000” or “1111” from further decrement or increment.

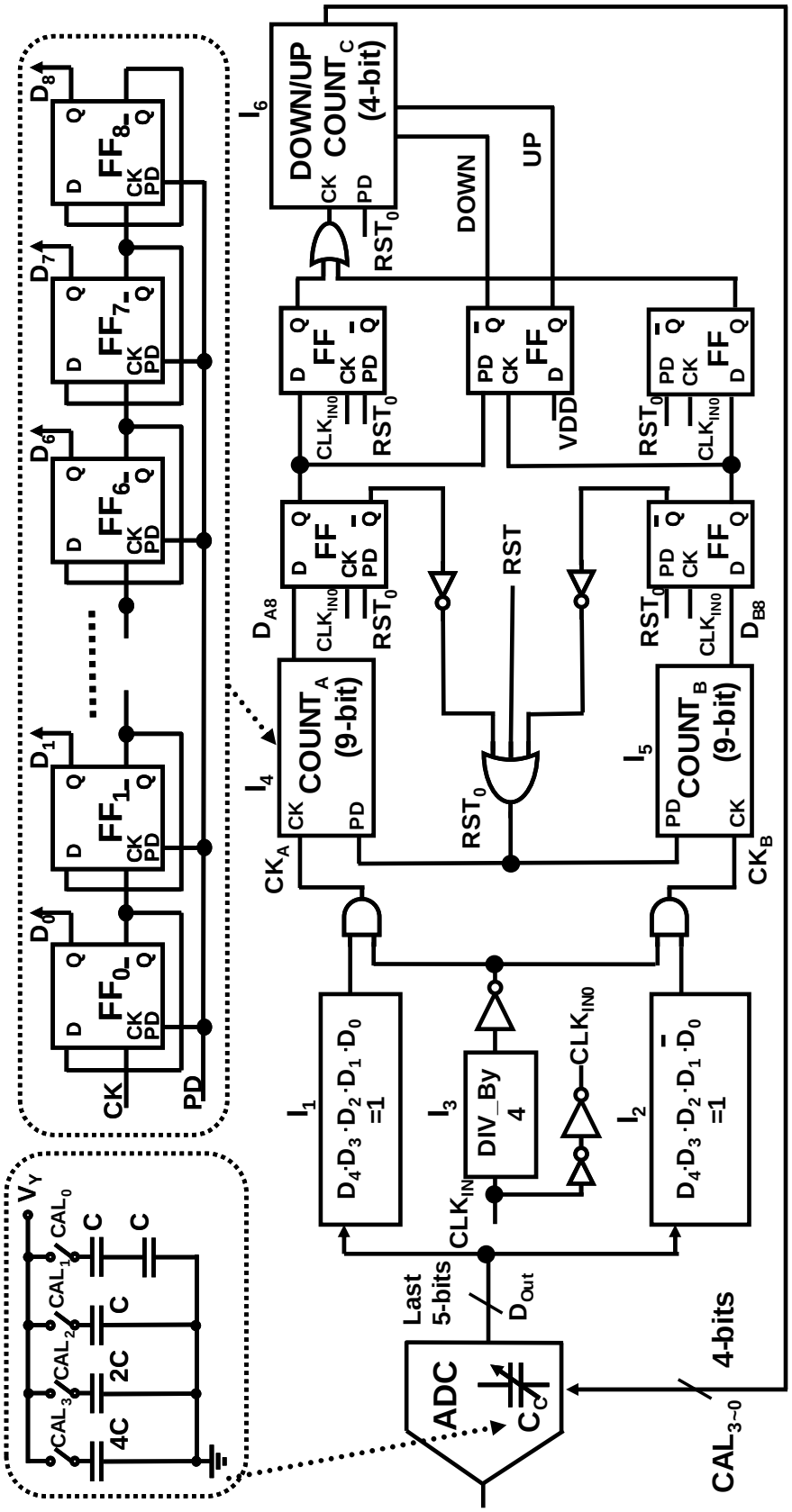


Figure 4.6 Circuits diagram of calibration block.

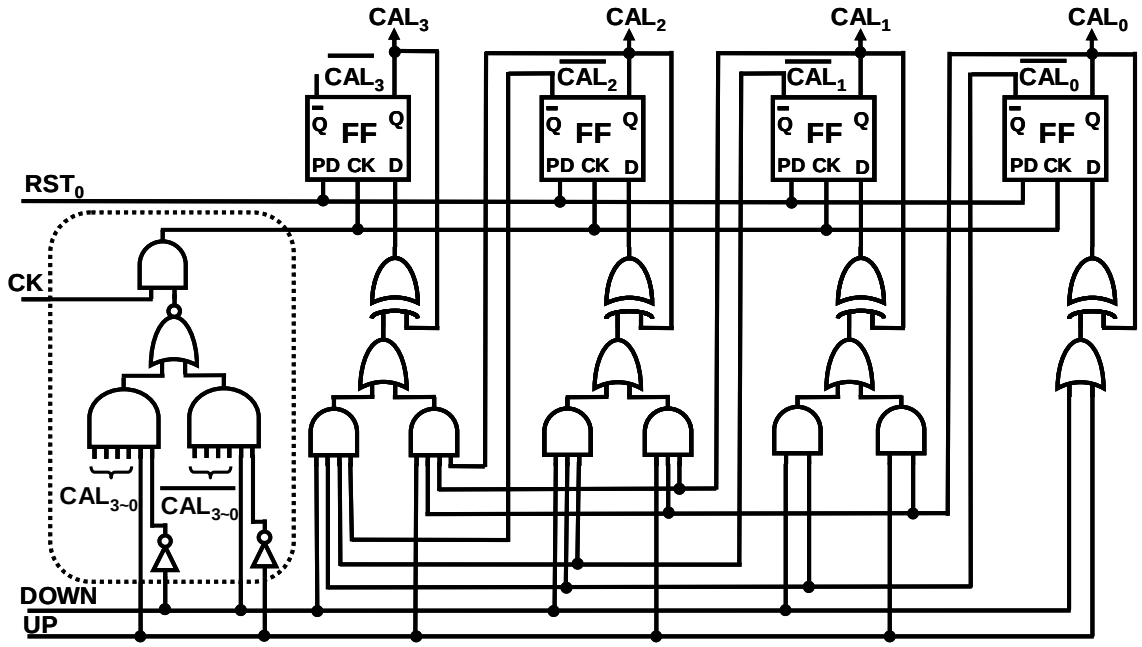


Figure 4.7 Circuits diagram of down/up counter.

4.3.3 Comparator

The schematic of a dynamic comparator is shown in Figure 4.8. A differential input pair feeds currents into a cross-coupled CMOS regenerative pair. The cross-coupled pair amplifies the differential input into near full logic levels. A reset switch in the input pair helps the comparator to recover from overdrive and avoid the kickback noise during the reset phase. The comparator outputs are connected with an SR-latch to control the successive approximation logic and also with a NAND gate to generate an internal asynchronous clock ICLK, which is also used to trigger the comparator itself. Since the CDAC calibration in this work is directly based on the data stream at the output, no calibration for comparator offset is required.

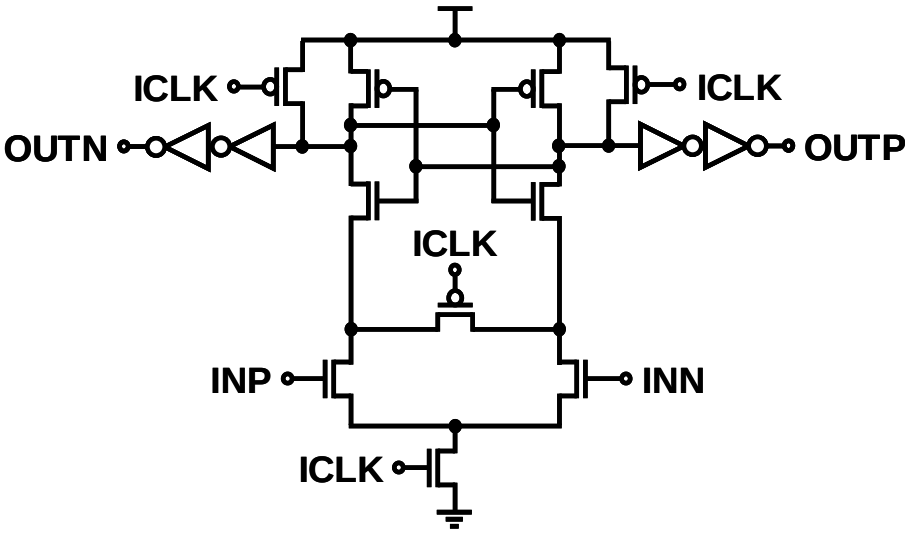


Figure 4.8 Comparator.

4.3.4 Control Logic

Based on tri-level charge redistribution technique, the SAR logic only needs to set a bit to 1 or 0 based on the comparator result in every bit decision. The logic is simplified and only requires shift registers and buffers. The shift registers in the SAR logic implement dynamic C^2MOS FFs, which have a small number of transistors and operate at high speed and low power.

4.3.5 Layout Design

The chip level layout is show in the Figure 4.9.

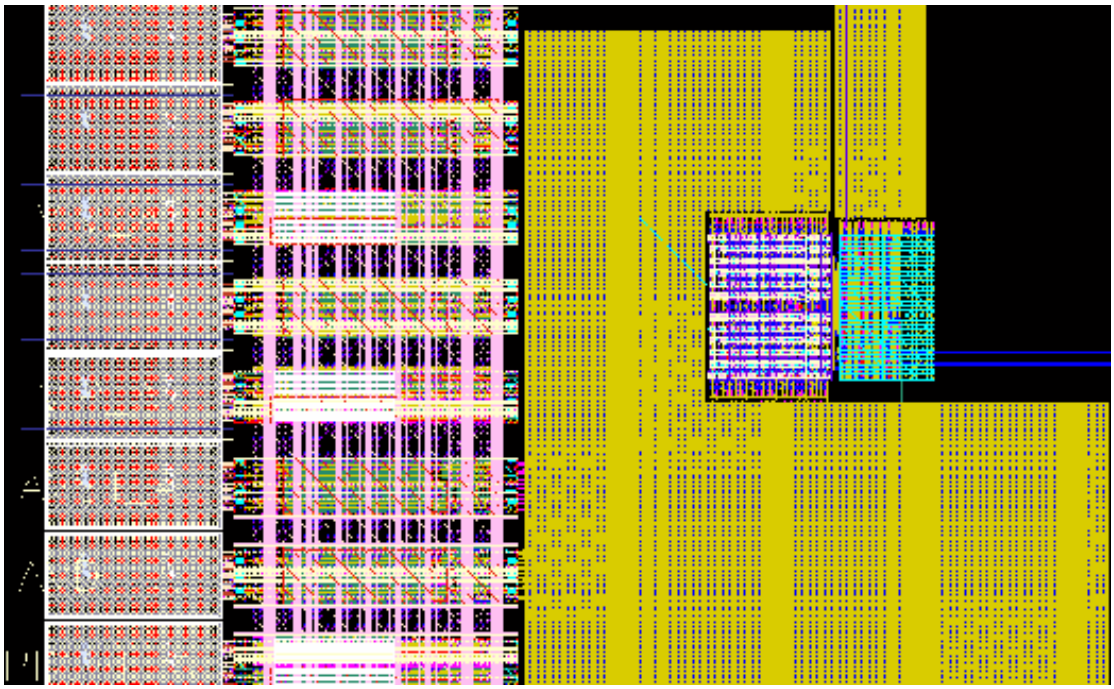


Figure 4.9 Chip level layout.

4.4 Measurement Results

The SAR ADC chip has been fabricated in a 65nm 1P7M CMOS process. Figure 9 shows the micrograph of the test chip. The active area of the ADC is 0.1mm×0.13mm.

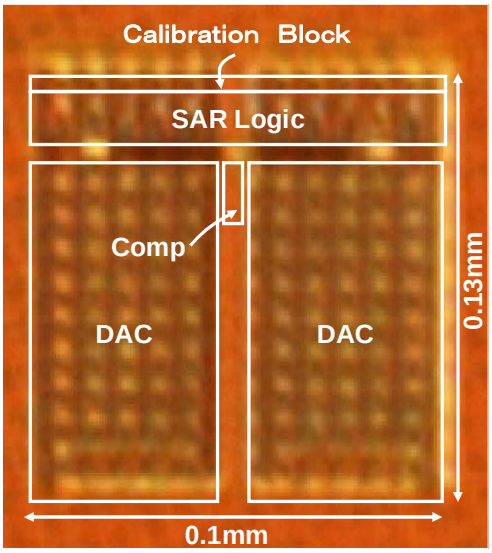


Figure 4.10 Chip photograph.

A periodic sine waveform is applied as the input analog signal and the sampling clock is produced by pulse generator. Figure 4.11 is the PCB board and measurement setup. The equipment used in the set-up and their functions are:

1) Agilent Logic Analyzer System: To capture the digital data coming from the ADC outputs;

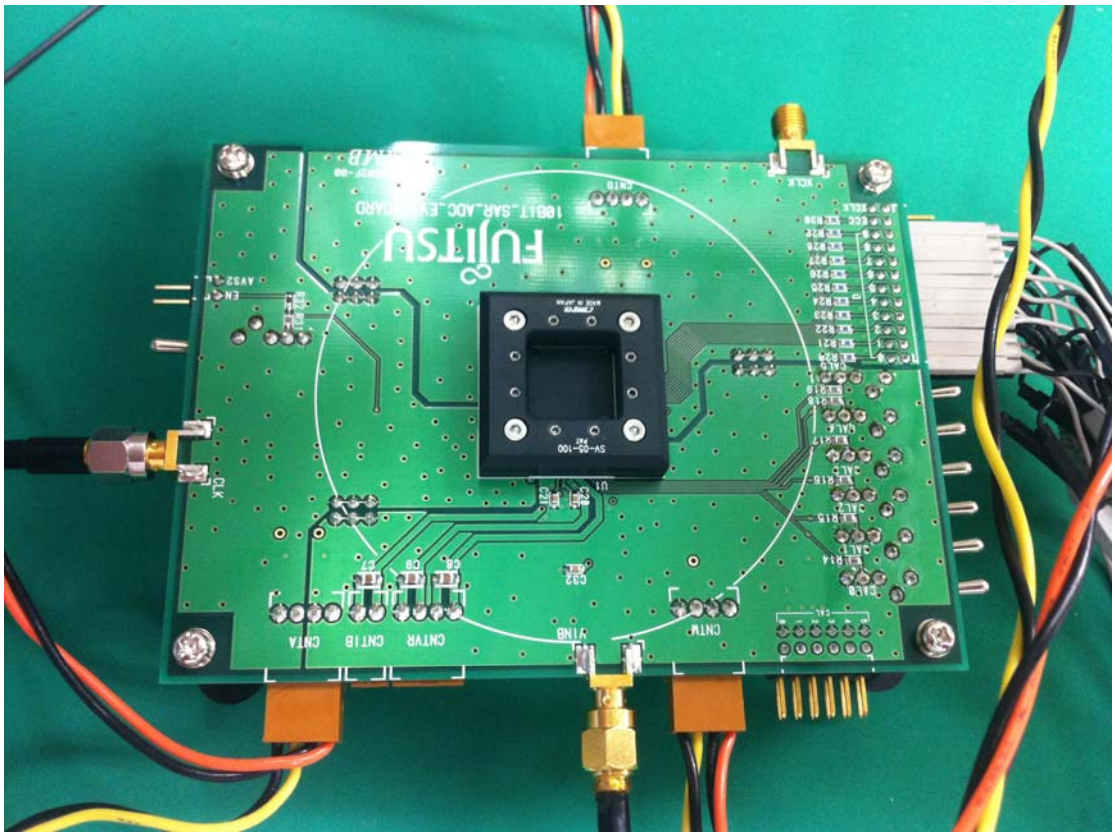
2) Agilent Signal Generator: To generate of the input signal;

3) Agilent Clock Generator: To generate the clock signal;

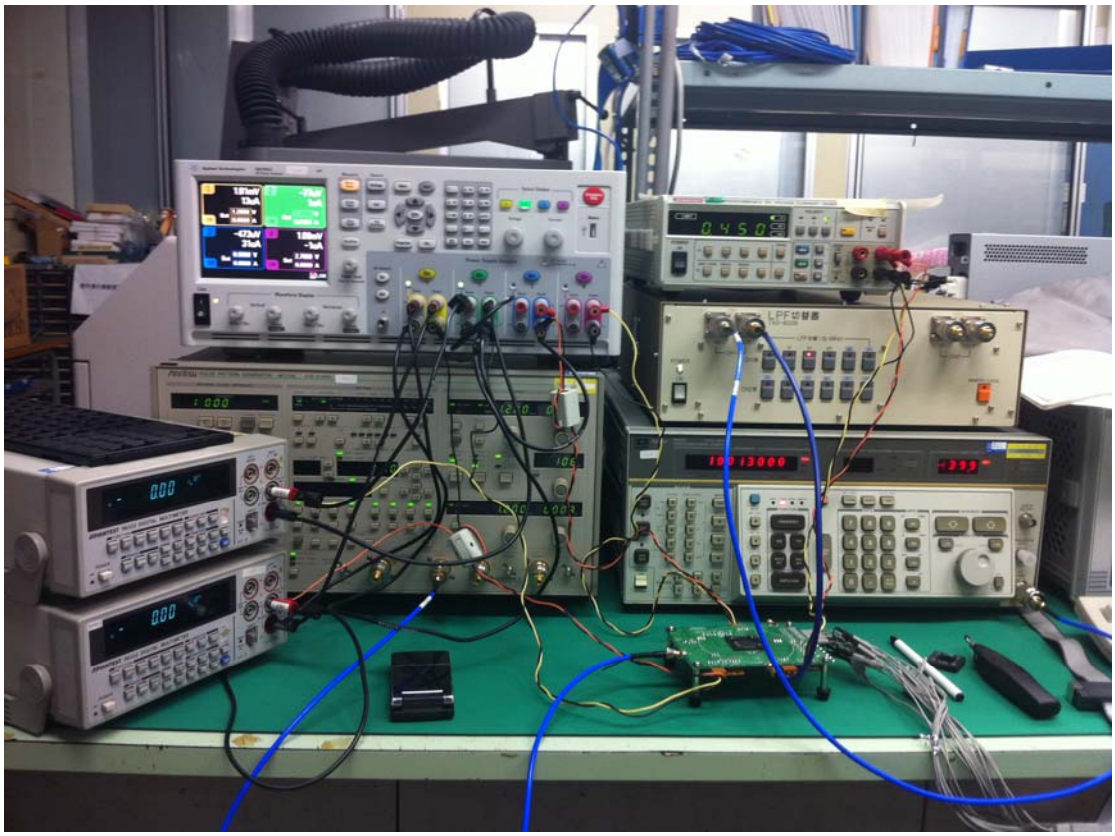
4) DC Power Supply: To generate VDD for the board. The board has discrete regulators to generate different supply voltages for the chip and only a single power supply is necessary. However, several power supplies were also kept in the test setup as any DC bias generation on the board or inside the chip can be disconnected and an external supply can be used;

5) HP Oscilloscope: For quick verification of node voltages on the board;

6) Agilent Multimeter: For quick verification of the dc voltages and the duty cycle of the chip clock (which can be measured from the DUTYOUT node).



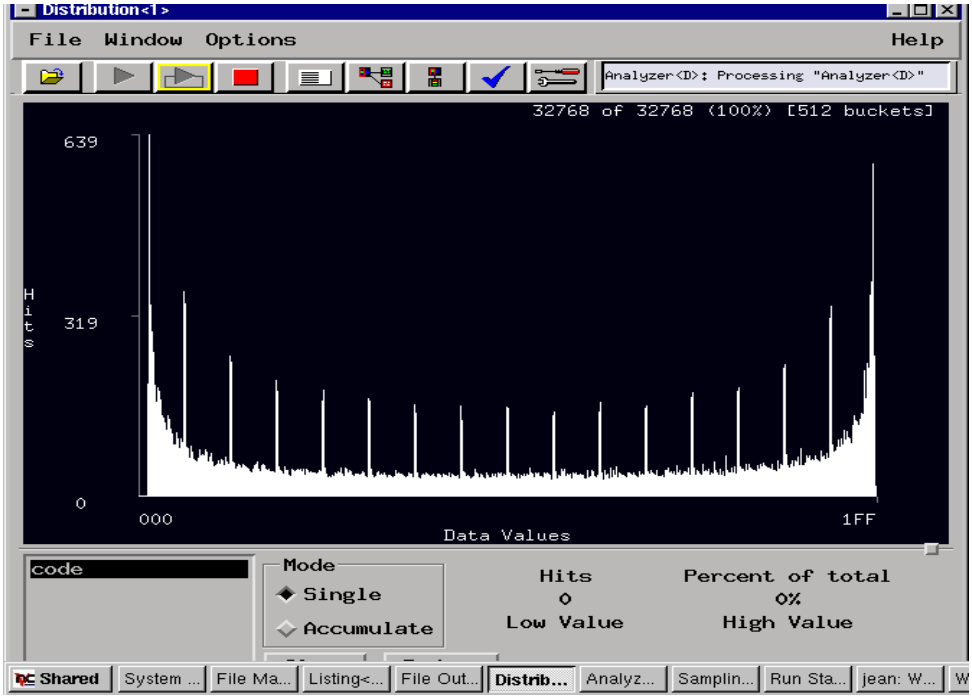
(a) PCB board.



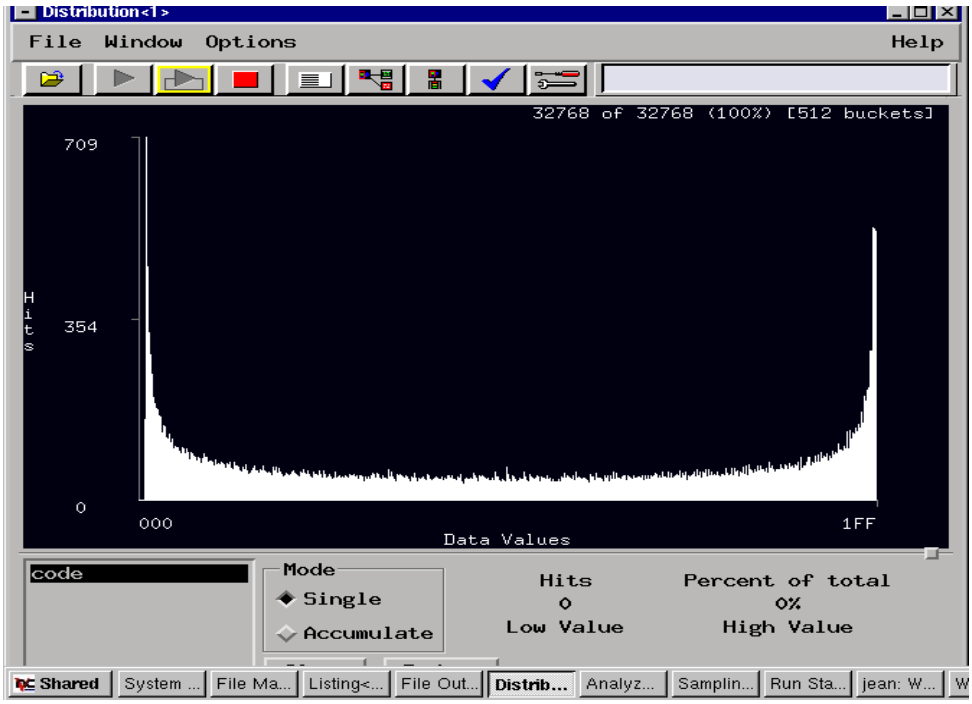
(b) Measurement setup.

Figure 4.11 PCB Board and Measurement setup.

Figure 4.12 shows the measured histogram before calibration and after calibration. The wide code error is effectively removed after calibration from the histogram. Figure 4.13 shows the measured static performance. After the calibration is performed, the DNL and INL at 100MS/s are +0.4/-0.4LSB and +0.5/-0.7LSB, respectively. Figure 4.14 shows the measured SNDR and SFDR versus sampling rate at frequency of input different signal is set 2.013MHz. Figure 4.15 plots the measured SNDR and SFDR of the ADC with respect to the frequency of input different signal at the sampling rate of 100MHz. With a 10% duty-cycle sampling clock from the pulse generator, the ADC achieves a peak SNDR of 50.89dB and SFDR of 62.06dB. Figure 4.16 shows the output FFT spectrum at near Nyquist input, which is around 47MHz.

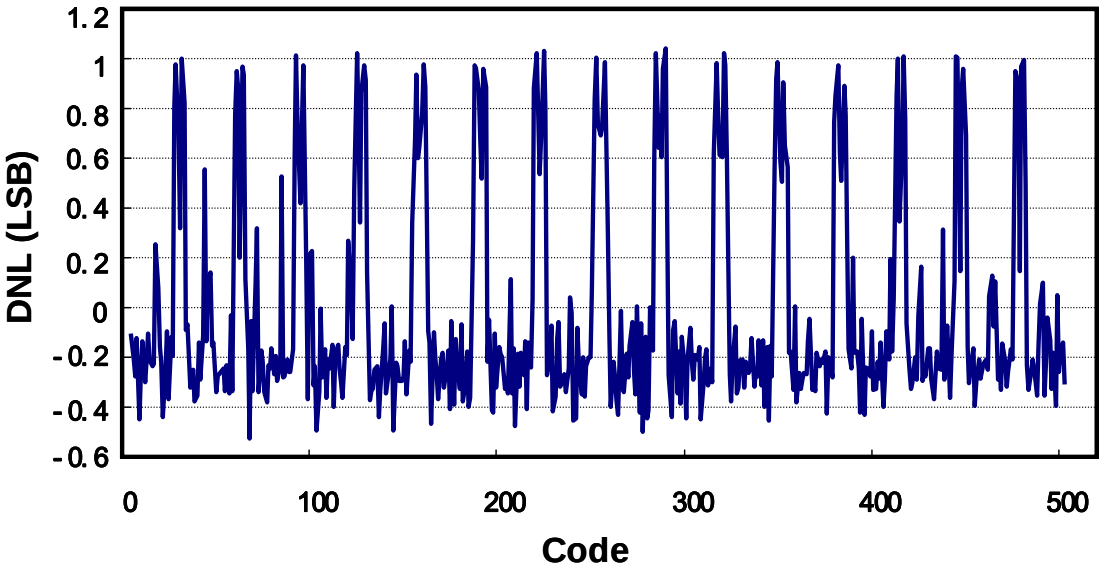


(a) Before calibration.

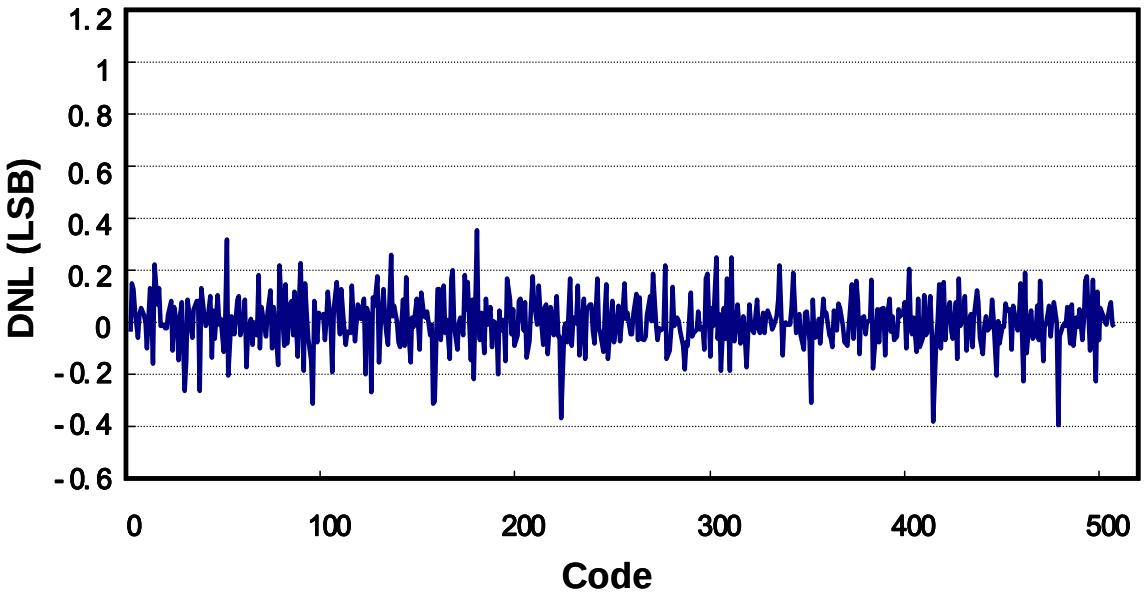


(b) After calibration.

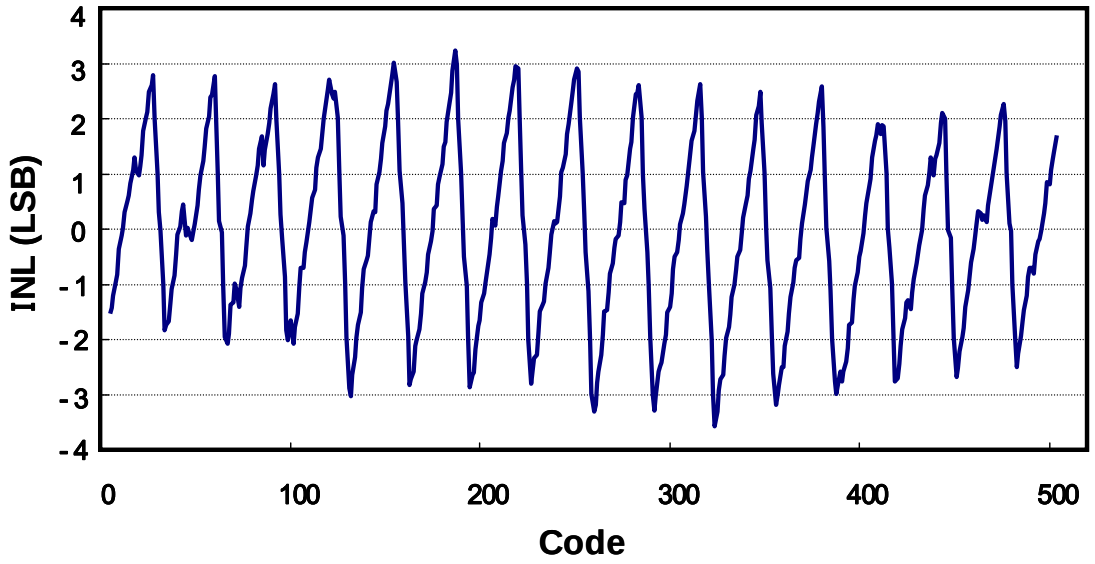
Figure 4.12 Windows of measured histogram at F_S=100MS/s.



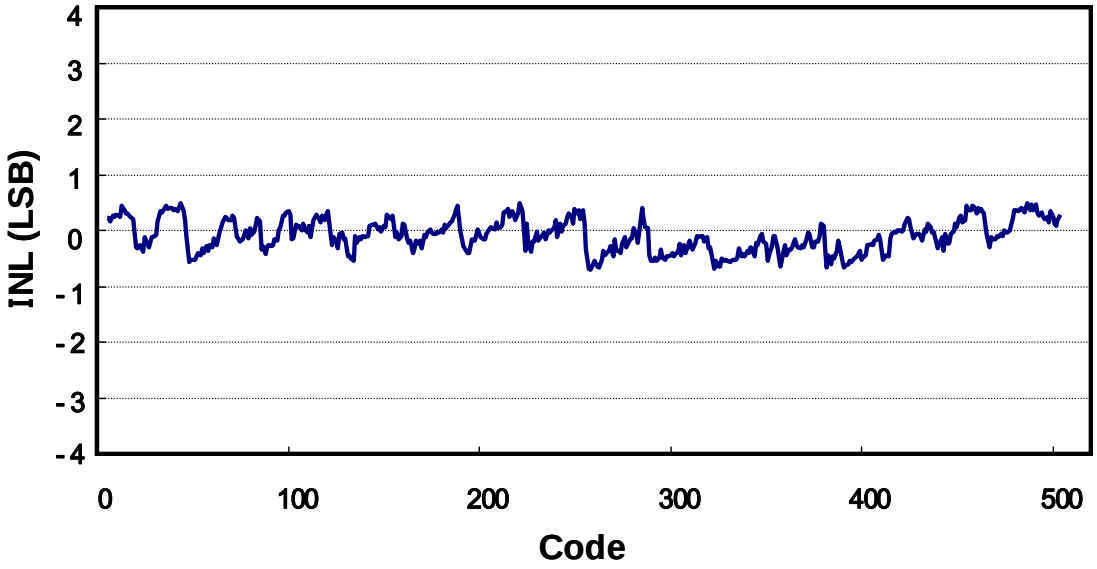
(a) DNL before calibration.



(b) DNL after calibration.



(c) INL before calibration.



(d) INL after calibration.

Figure 4.13 Measured DNL and INL at F_S=100Ms/s.

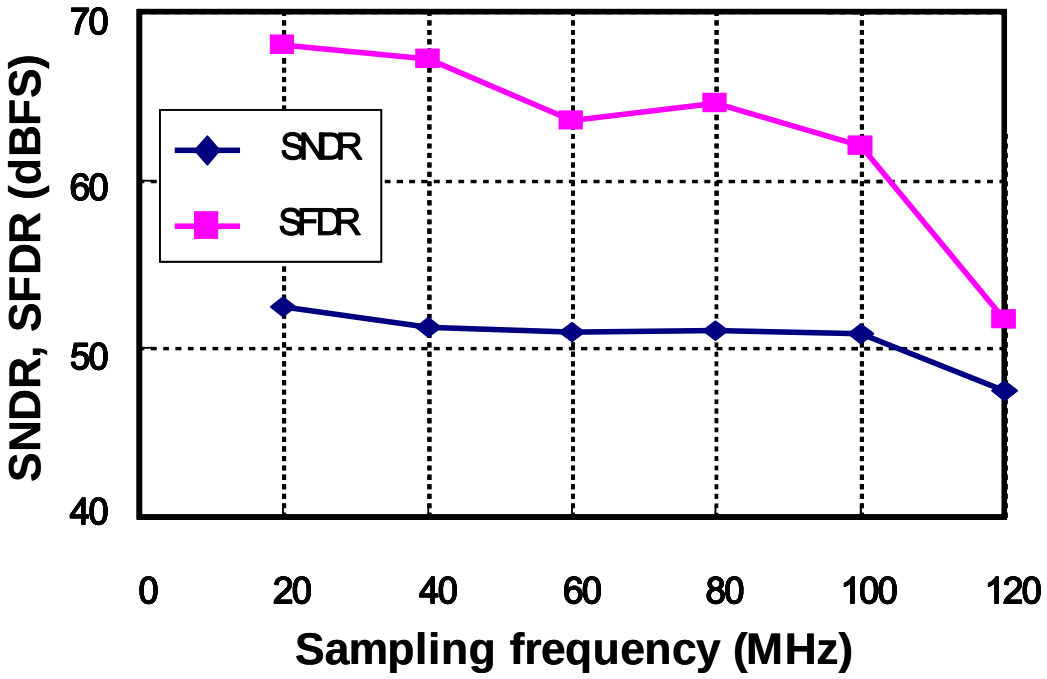


Figure 4.14 Measured SNDR and SFDR vs. sampling frequency at F_{in}=2.013MHz.

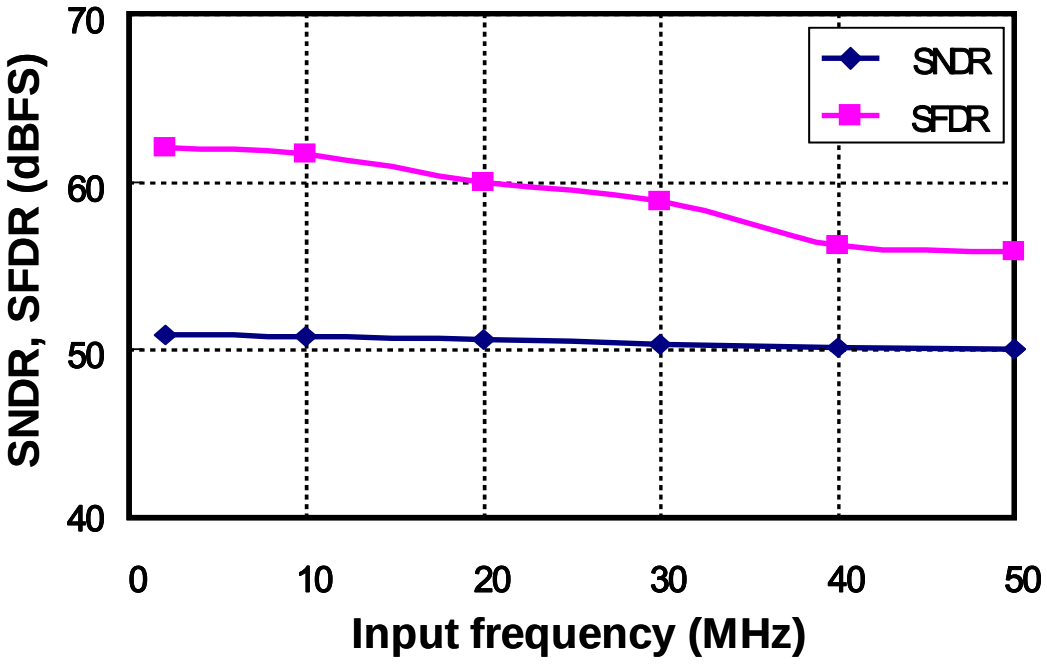


Figure 4.15 Measured SNDR and SFDR vs. input frequency at F_s=100MHz.

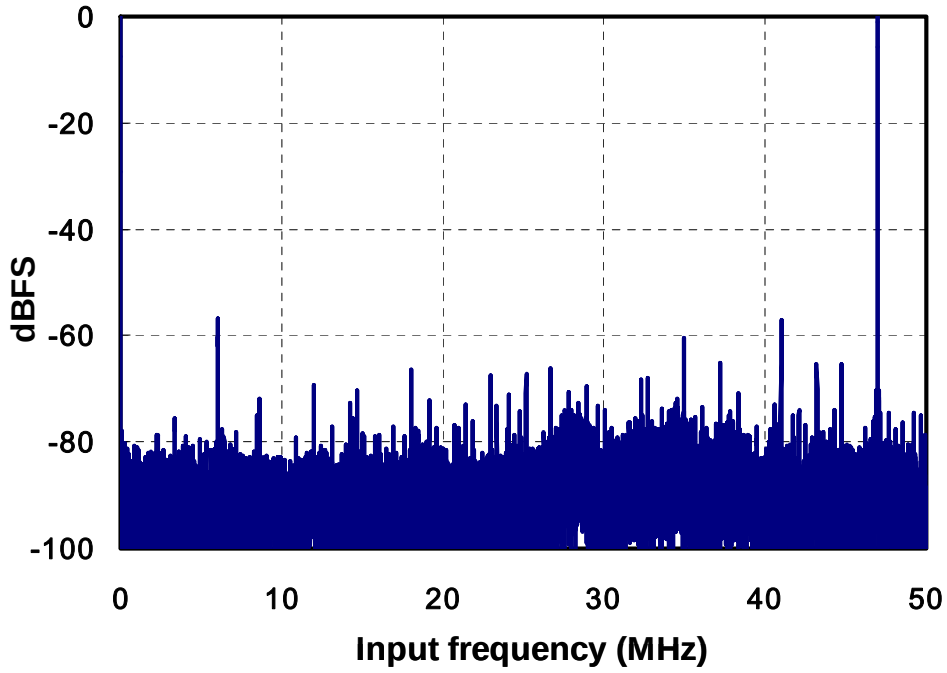


Figure 4.16 Measured output FFT spectrum.

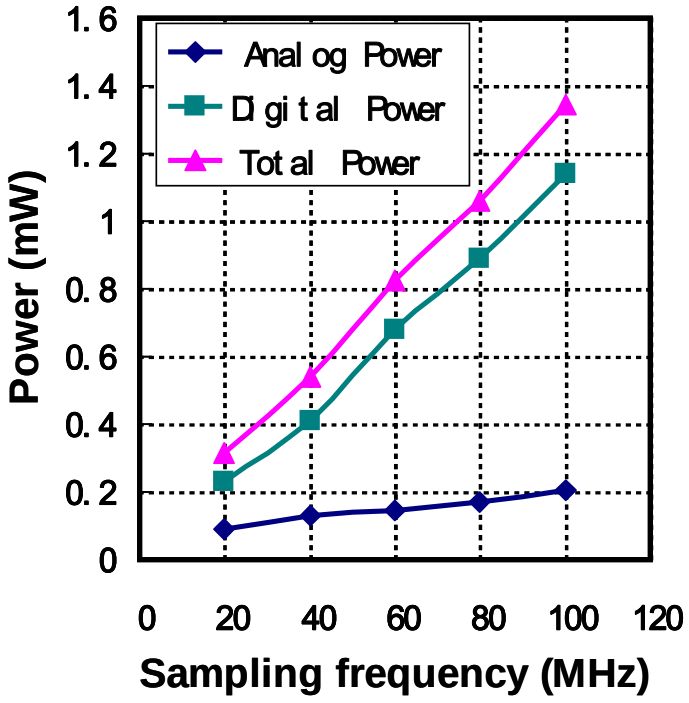


Figure 4.17 Measured power vs. sampling frequency.

The ADC consumes 1.34mW at 100MS/s sampling rate from a 1.2V supply voltage, 0.204mW for analog and 1.14mW for digital. The reference uses the 1.2V supply voltage, included in the analog power. The Figure 4.17 displays the measured power consumption under the power supply of 1.2V versus the sampling frequency. The same 2.013MHz sinusoidal stimulus is applied to the tests. The power consumption is proportional to the sampling frequency. Based on the definition of figure of merit (FOM), which is defined as $FOM=P/(f_s*2^{ENOB})$, the ADC achieves an FOM of 47fF/conversion-step. Table 4.1 summarizes the ADC performance.

4.5 Conclusion

The motivation for this work came from the observation that nonlinearities dominate the split CDAC based SAR ADC causes missing code or wide code at bit decision boundary periodically. Calibration block watches the data stream from ADC output to find the wide or missing code and feedback to the compensation capacitor so as to relax the nonlinearity caused by CDAC mismatch. There is no need for additional analog hardware, such as a redundant channels or a reference converter to calibrate against. The calibration is performed using the input signal without requiring special calibration signal so that the users do not see service interruption. Furthermore, its simplicity and being a digitally assisted scheme make it amenable to scaled CMOS implementation. The proposed scheme has a limitation since it has to some extent dependence on the input signal, for example, it is hardly to handle the DC signal. In some special cases, if the output codes do not exercise the codes uniformly at both of the desired boundary region (codes 31, 63,..., 479) or (codes 30, 62,…, 478) due to input signal, the calibration scheme might not work very well. However, in most

applications, because the analog inputs are random signals, it is feasible for calibration block to watch and process the digital codes in the specified vicinity of the decision boundaries and feed back to the CDAC. The proposed technique is confirmed by a 9-bit split CDAC based SAR ADC fabricated in 65nm CMOS with 1.2V power supply. The ADC occupies 0.1 x 0.13mm^2 and consumes 1.34mW.

Table 4.1 Performance Summary

Power supply	1.2V
Input capacitance	180fF
Sampling rate	100MS/s
Resolution	9 bits
Analog power	0.204mW
Digital power	1.14mW
Total power	1.344mW
DNL	+0.4 / -0.4 LSB
INL	+0.5 / -0.7 LSB
ENOB	8.14 at fin=10MHz 8.02 at fin=50MHz
FOM	47fJ/conversion-step
Area	0.1mm × 0.13mm
Technology	65nm 1P7M CMOS with MIM capacitor

References (4)

[1] P.Li, M. Chin, P. Gray, and R. Castello, “A ratio-independent algorithmic analog-to-digital conversion technique,” IEEE J. Solid-State Circuits, vol. SSC-29, no.6, pp. 828-836, Dec. 1984.

[2] B.S. Song, M. Tompsett, and K. Lakshmikumar, “A 12-bit 1-msample/s capacitor error-averaging A/D converter,” IEEE J. Solid-State Circuits, vol. 33, no. 6, pp. 1316-1323, Dec. 1988.

[3] H. Lee, D. Hodges and P. Gray, "A self-calibrating 15 bit CMOS A/D converter," IEEE J. Solid-State Circuits, vol. 19, no. 12 pp. 813 - 819, Dec. 1984.

[4] Y. Chen, et al., "Split Capacitor DAC Mismatch Calibration in Successive Approximation ADC," IEEE Custom Integrated Circuits Conference Dig. Tech. Papers, 2009, pp.279-282.

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[8] W. Liu, P. Huang, Y. Chiu, "A 12b 22.5/45MS/s 3.0mW 0.059mm2 CMOS SAR ADC Achieving Over 90dB SFDR," IEEE ISSCC Dig. Tech. Papers, 2010, pp. 380 - 381.

Chapter 5 Design of A 9-bit 100MS/s Tri-level Charge Redistribution SAR ADC with Asymmetric CDAC Array

5.1 Introduction

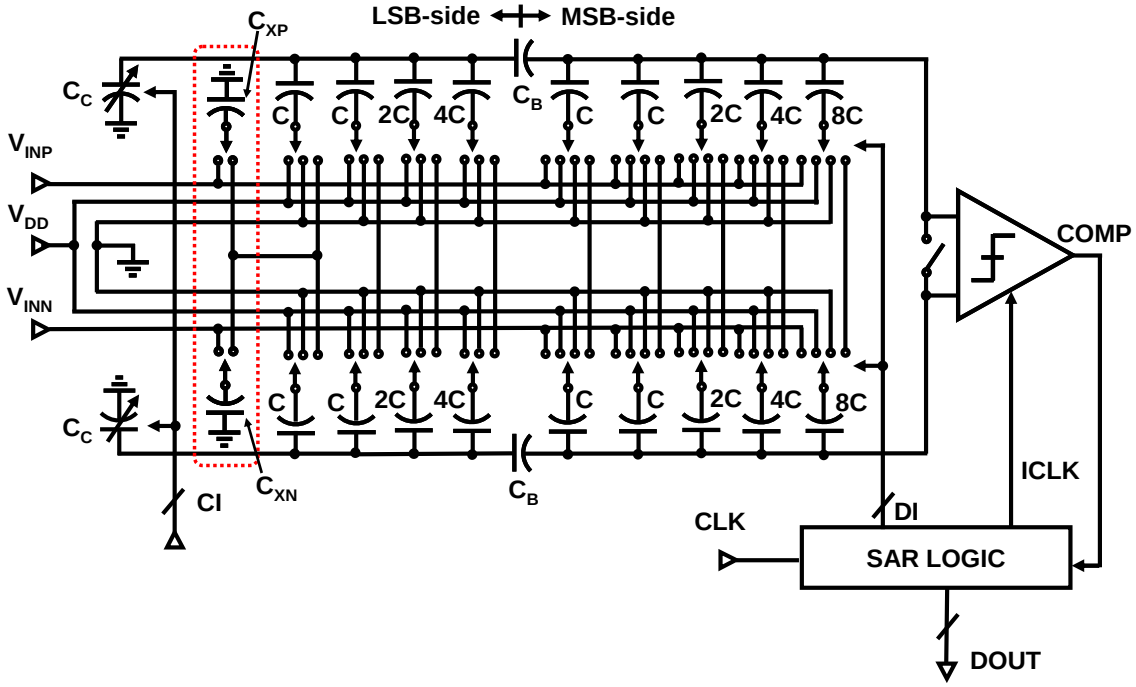
In most SAR ADC design, large capacitance required by the CDAC results in limited settling speed, increased power consumption and silicon cost [1-7]. Therefore, improvement of the area and energy efficiencies for the CDAC is one of the most important issues for SAR ADC design.

In this chapter, a partially asymmetric CDAC design technique is proposed based on the split CDAC architecture and tri-level charge redistribution technique [2]. With this technique, it is possible for a SAR ADC to achieve 9-bit resolution with 4-bit + 3-bit split capacitor arrays which saves CDAC area and the power as well. The proposed technique reduces total capacitance by 95% comparing to the conventional full binary weighted capacitor array and by 25% comparing to the symmetric tri-level split capacitor array.

5.2 Architecture

As shown in Figure 5.1, the ADC consists of an asymmetric tri-level charge redistribution CDAC, a comparator, and a SAR control logic. The DAC are implemented as split capacitor arrays (4-bit + 3-bit) for small area and input capacitance. A bridge capacitor C_B connects the top plates of the MSB-side and LSB-side capacitor arrays. An additional pair of capacitors C_{XP} and C_{X_N} with the same size as the unit capacitor is implemented in the CDAC with their top plates connecting to ground and bottom plates being connectable with each other. The tri-level charge redistribution is achieved by passive charge sharing since the bottom plates of both differential capacitor arrays are designed to be connectable with each other. The

system clock CLK defines the sampling phase. The comparator is triggered by an internal asynchronous clock ICLK, which is generated by detecting the outputs of the comparator. The mismatches between the MSB-side and LSB-side capacitor arrays due to process variation and parasitic capacitance are compensated by a tunable capacitor C_C implemented in parallel with the LSB-side array. The asymmetric CDAC architecture, the other building block and the conversion procedure will be discussed in detail in next section.



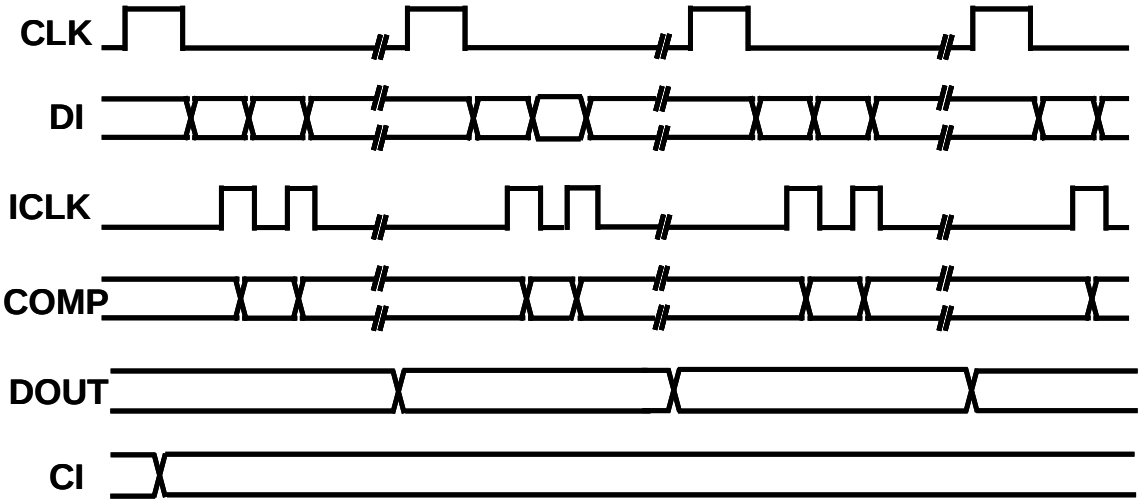


Figure 5.1 Architecture of the ADC.

5.3 Circuits Implementation

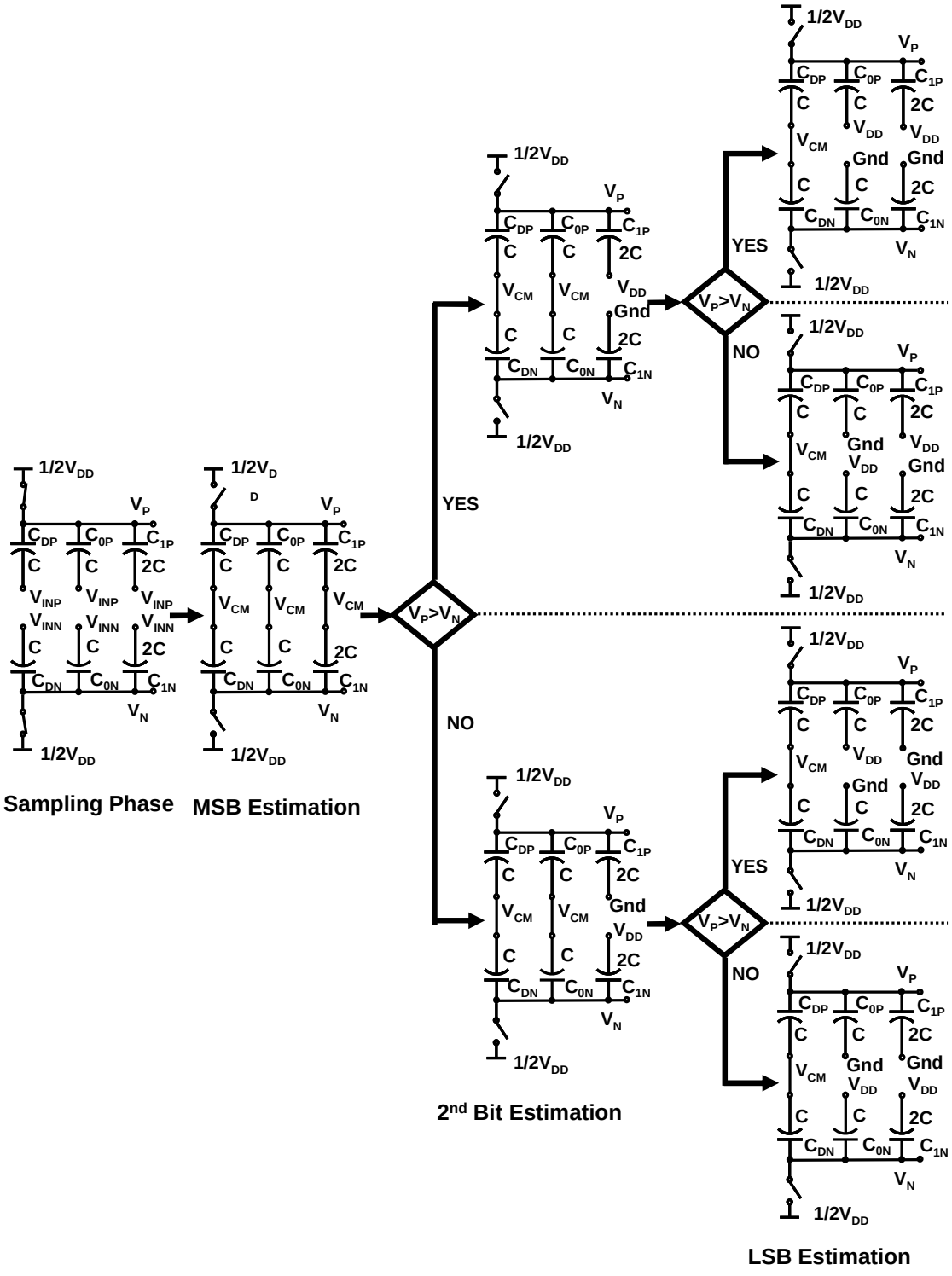
5.3.1 Asymmetric tri-level CDAC

Figure 5.2 (a) shows a tri-level CDAC [2] example with 2-bit capacitor array. During the sampling phase, the bottom plates of all capacitor arrays are connected to the differential input signals V_{INP} and V_{INN} while the top plates are connected to the common mode voltage of the comparator, which is 1/2 V_{DD}. After the top plates become floating, the bottom plates of the two different capacitor array are disconnected from the inputs and all differential capacitor pairs are connected with each other through switch arrays. The bottom plates charge sharing achieves voltage averaging which means all bottom plates of capacitor are switched from V_{IN} to V_{CM}, the common level of differential inputs. Supposing the common mode level differential inputs is also half of V_{DD}, the input is therefore compared to the $V_{DD}/2$ and the MSB bit estimation is made by the comparator. Then the bottom plates of capacitor C_{1P} and C_{1N} are switched from V_{CM} to either V_{DD} or Gnd based on the MSB decision which

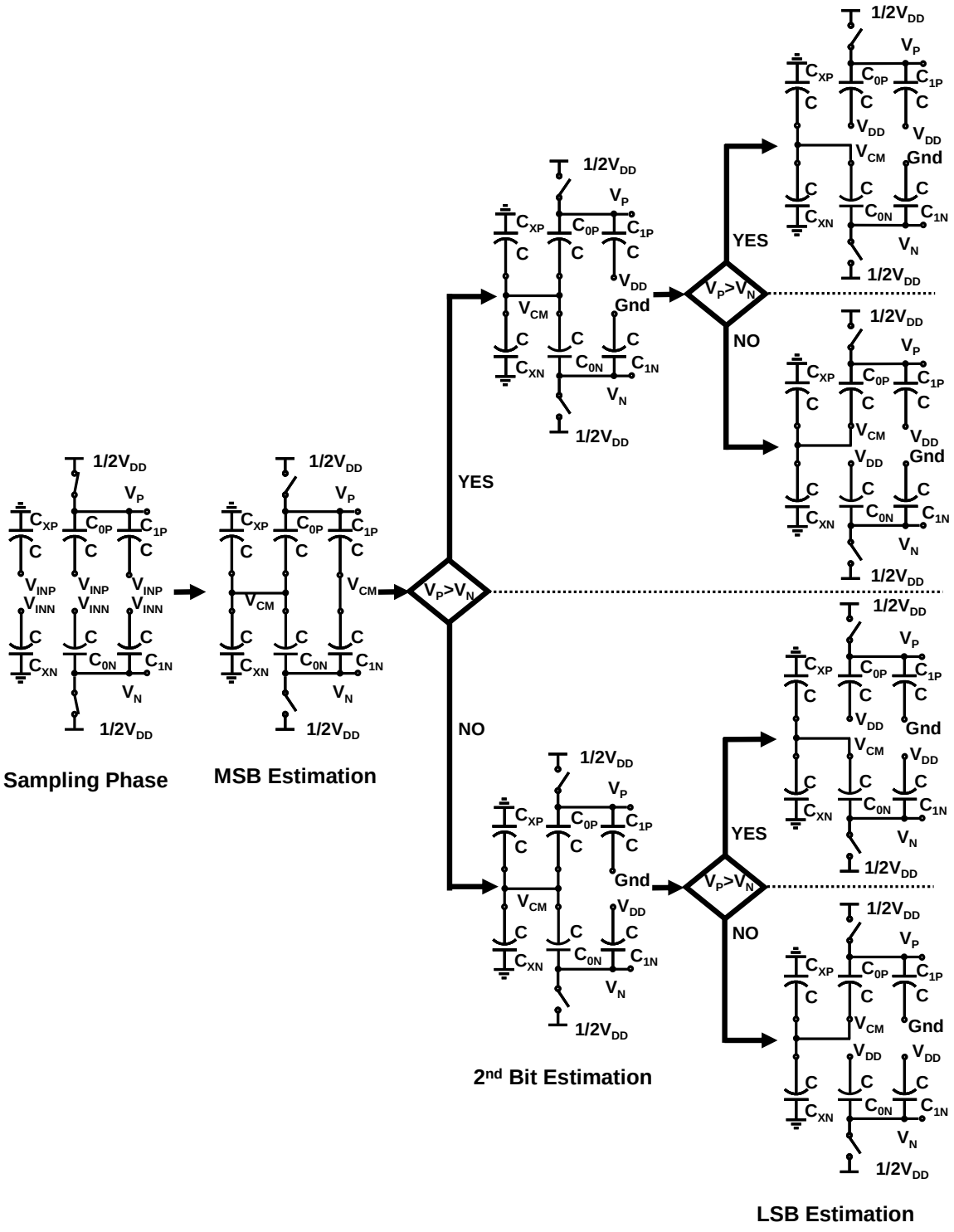
means the input is compared to 1/4 V_{DD} or 3/4 V_{DD} and therefore the second bit estimation is achieved by the comparator. Finally, the comparator resolves the LSB by the same way as switching the bottom plates of C_{0P} and C_{0N} from V_{CM} to V_{DD} or Gnd based on the second bit decision. This conversion procedure demonstrates a 2-bit capacitor array is able to achieve 3 bit conversion by using the tri-level charge redistribution technique.

The proposed asymmetric tri-level charge redistribution DAC utilizes the same passive charge sharing technique as [2]. As shown in Figure 5.2 (b), except for the differential capacitor arrays, an additional pair of capacitors C_{XP} and C_{XN} with their top plates being grounded is implemented in the CDAC. During the sampling phase, the bottom plates of all capacitor arrays and the additional pair of capacitors C_{XP}, C_{XN} are connected to the differential input signals V_{INP} and V_{INN} while the top plates are connected to the common mode voltage V_{CM}. After the top plates become floating, the bottom plates of all the capacitors including C_{XP} and C_{XN} are disconnected from the inputs and those differential capacitor pairs are connected with each other through switch arrays. In the meantime, the bottom plates of C_{XP}, C_{XN}, C_{0P} and C_{0N} are connected together. Therefore, all bottom plates of the capacitor are switched from V_{IN} to V_{CM}. So the input is compared to the common mode level of differential inputs that is also supposed to be $V_{DD}/2$ and therefore the MSB bit estimation is made by the comparator. Then the bottom plates of capacitor C_{1P} and C_{1N} are switched from V_{CM} to either V_{DD} or Gnd based on the MSB decision so as to compare the input with 1/4 V_{DD} or 3/4 V_{DD} and the comparator achieve the second bit estimation. After the second bit is determined, one of the bottom plates of capacitors C_{0P} or C_{0N} is switched from V_{CM} to V_{DD}, while the other one is kept connecting to V_{CM} level, which is like an

asymmetric connection. For example, if the comparator output of the second bit is a logic “1”, meaning $V_P>V_N$, the bottom plate of C_{0P} is switched from V_{CM} to V_{DD}, and the bottom plate of C_{0N} is kept to the V_{CM}; if the comparator output of the second bit is a logic “0”, meaning $V_P<V_N$, the bottom plate of C_{0P} is kept to the V_{CM}, and the bottom plate of C_{0N} is switched from V_{CM} to V_{DD}. The voltage on the input of the comparator is now increased or decreased 1/8 the reference as a result of this operation and then the LSB is achieved by the comparator. This conversion procedure demonstrates a 1-bit capacitor array is able to achieve 3 bit resolution by utilizing the asymmetric tri-level charge redistribution technique. An additional pair of capacitors C_{XP} and C_{XN} is required in this method which means increased silicon cost. However, in real implementation, dummy capacitors can be taken use of since the dummy capacitors are always necessary for keeping the CDAC core in symmetric in SAR ADC design. Therefore, in most cases, without any extra cost, proposed asymmetric tri-level CDAC has two more bit resolution than the conventional CDAC and one more bit resolution than the symmetric tri-level CDAC, which results in an improvement of area efficiency.



(a) Symmetric Tri-level CDAC



(b) Asymmetric Tri-level CDAC

Figure 5.2 The 3-bit charge redistribution DAC.

Since the average switching energy consumed by the CDAC in SAR ADC increases exponentially with the number of bits [3-4], CDAC area efficiency by asymmetric architecture also leads to an improvement of power efficiency. For the same resolution, asymmetric tri-level CDAC consumes only half of the power that required by the symmetric tri-level CDAC. In order to further reduce both input capacitance and area, split capacitor arrays are implemented in this design. A 4-bit + 3-bit capacitor array is designed to achieve 9-bit resolution, which is around 4.7% area of that occupied by a full binary weighted capacitor array and 75% area of that occupied by a symmetric tri-level split capacitor array. The additional pair of capacitors C_{XP} and C_{NP} does not cost extra area since the dummy capacitors are utilized.

5.3.2 Comparator

The schematic of a dynamic comparator is the same as the one that has been introduced in chapter 4. A differential input pair feeds currents into a cross-coupled CMOS regenerative pair. The cross-coupled pair amplifies the differential input into near full logic levels. A reset switch in the input pair helps to reduce the comparator recovery time during the reset phase. The comparator outputs are connected with an SR-latch to control the successive approximation logic and with a NAND gate to generate an internal asynchronous clock ICLK, which is also used to trigger the comparator itself.

5.3.3 Control Logic

The designed ADC uses an asynchronous control circuit to internally generate the clock signals to trigger the comparator, which is the same as the circuits have been discussed in chapter 4

5.3.4 Layout Design

The chip level layout is show in the Figure 5.3 which include two different cores, one is the ADC with histogram based digital calibration, another is the ADC combined with Asymmetric CDAC technique and histogram based digital calibration.

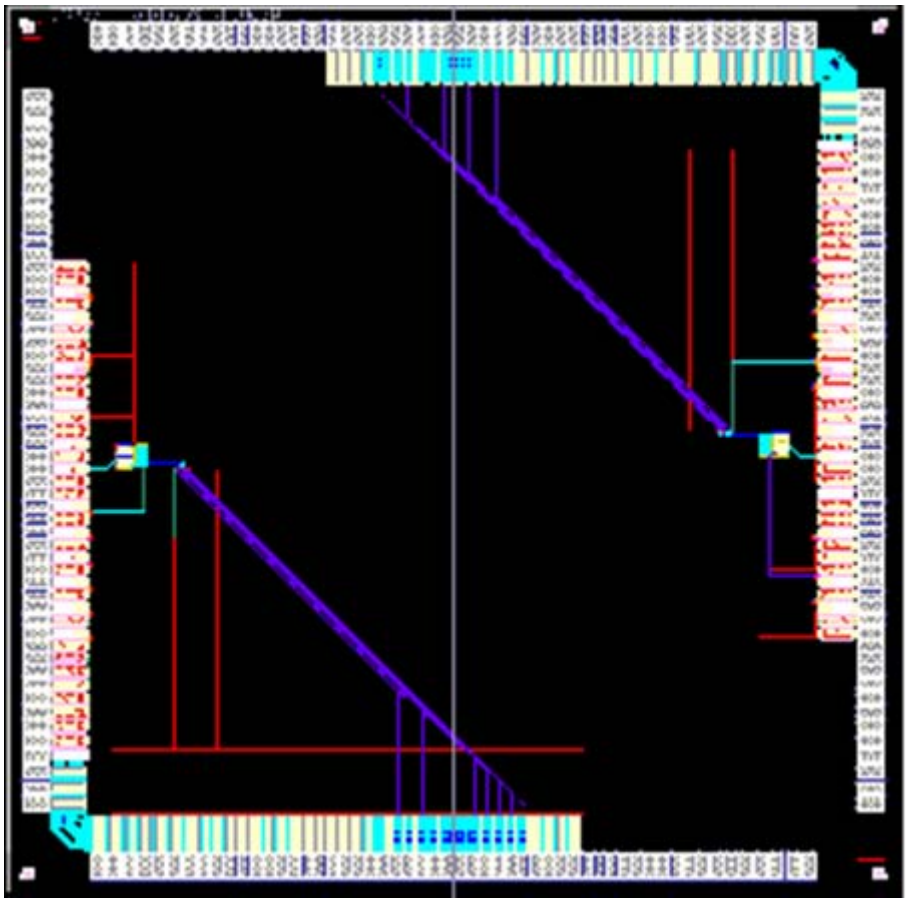


Figure 5.3 Chip level layout design

5.4 Measurement Results

The SAR ADC chip has been fabricated in a 65nm 1P7M CMOS process. Figure 5.4 shows the micrograph of the test chip. The active area of the ADC is 0.1mm×0.13mm.

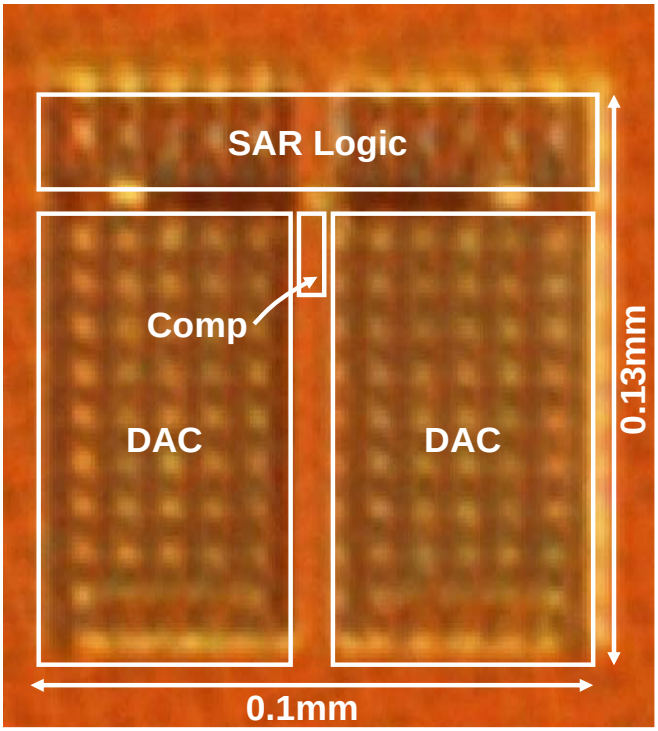
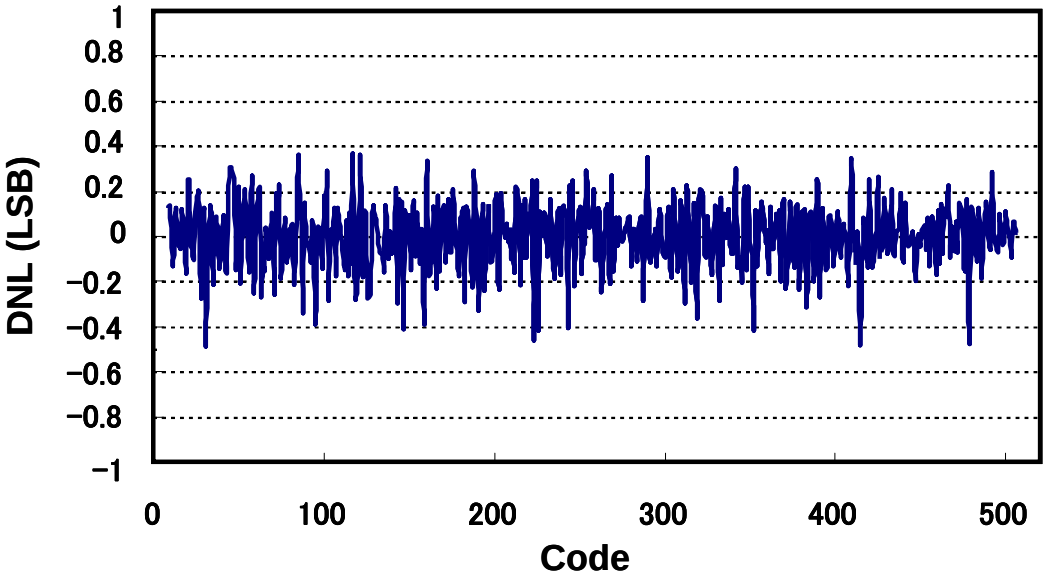
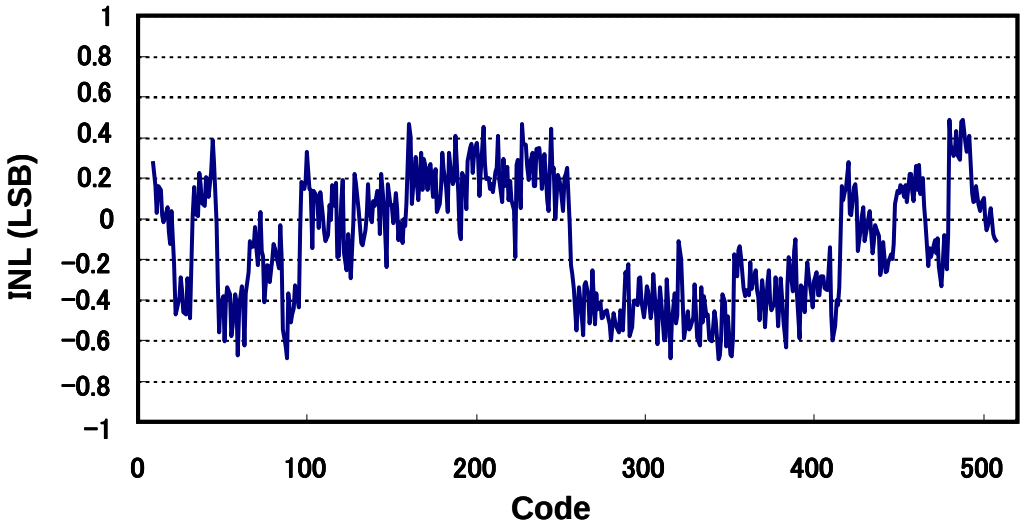


Figure 5.4 Chip photograph.

Figure 5.5 shows the measured static performance. After the calibration is performed, the DNL and INL at 100MS/s are +0.4/-0.5LSB and +0.5/-0.7LSB, respectively. Figure 5.6 shows the measured SNDR and SFDR versus sampling rate at frequency of input different signal is set 2.013MHz. With a 10% duty-cycle sampling clock, the ADC achieves a peak SNDR of 50.13dB. Figure 5.7 shows the output FFT spectrum at near Nyquist input, which is around 47MHz.



(a) DNL



INL

Figure 5.5 Measured static performance

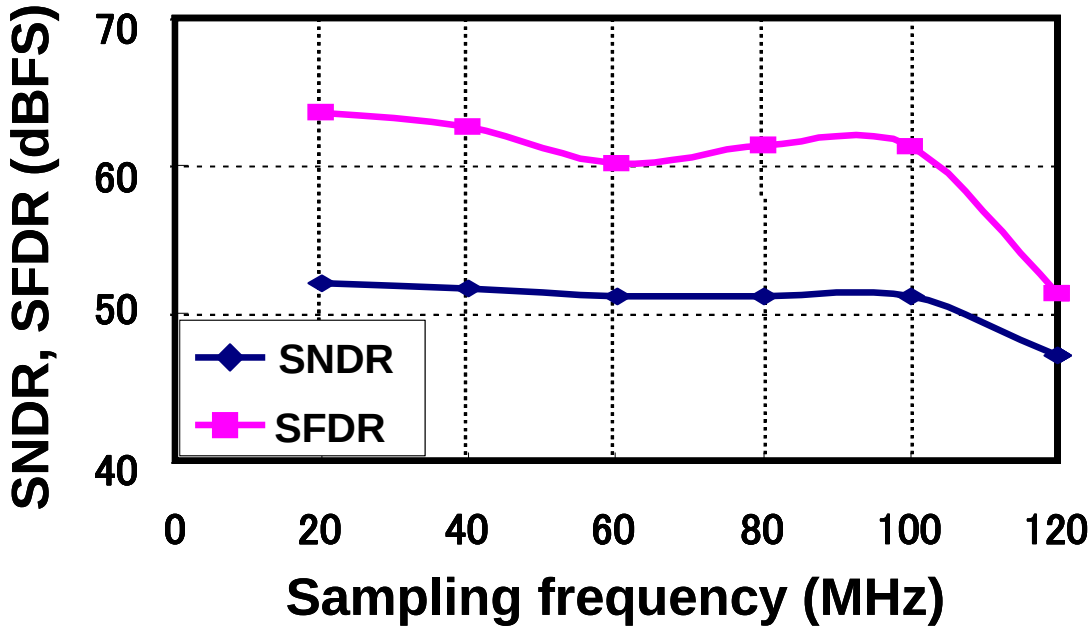


Figure 5.6 Measured F_S vs. SNDR & SFDR.

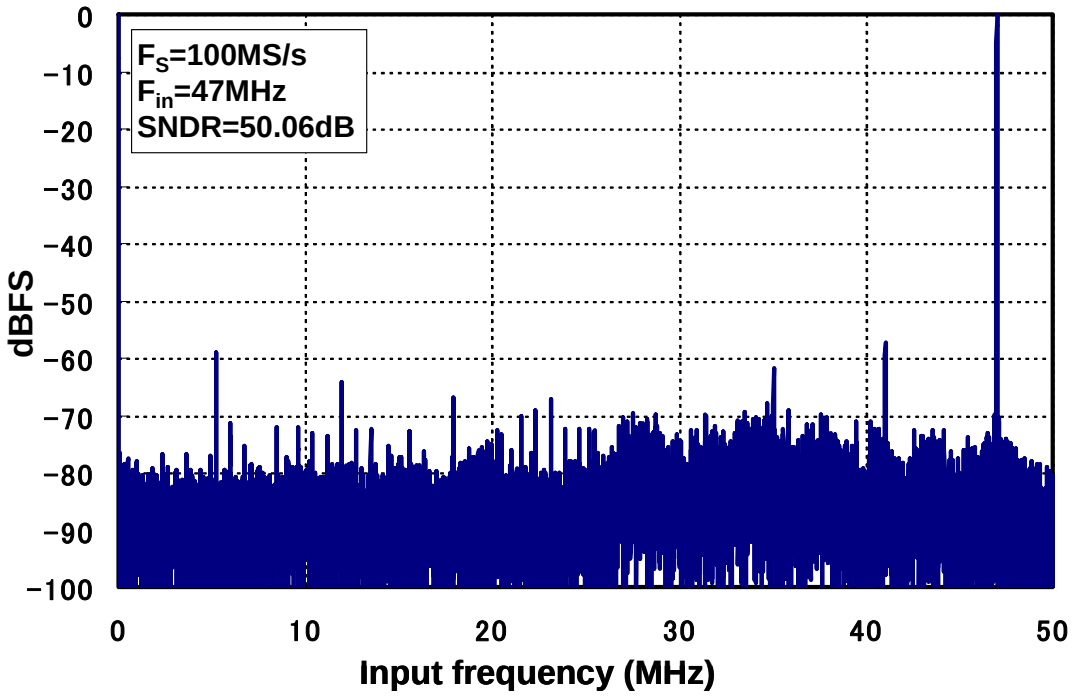


Figure 5.7 Measured FFT spectrum.

The ADC consumes 1.26mW at 100MS/s sampling rate from a 1.2V supply voltage, 0.204mW for analog and 1.14mW for digital. The reference uses the 1.2V supply voltage, included in the analog power. The Figure 5.8 displays the measured power consumption under the 1.2V supply voltage versus the sampling frequency. The same 2.013MHz sinusoidal stimulus is applied to the tests. Based on the definition of figure of merit (FOM), which is defined as FOM=P/(F_s*2^{ENOB}), the ADC achieves an FOM of 45fF/conversion-step. Table I summarizes the ADC performance.

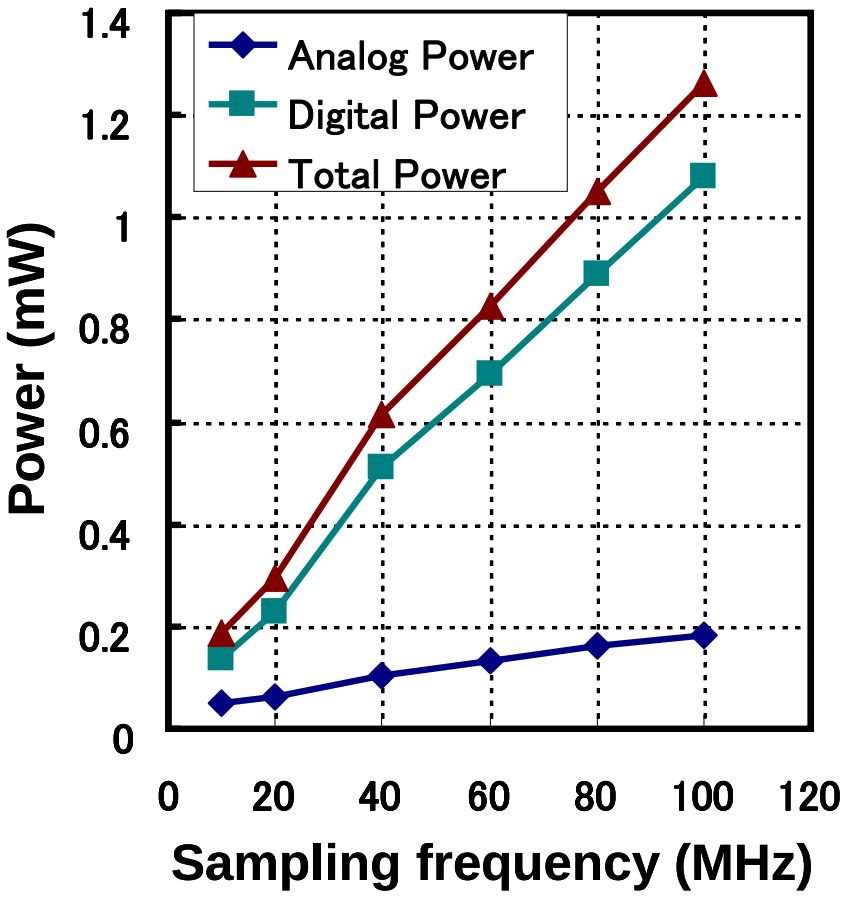


Figure 5.8 Measured F_S vs. power.

Table 5.1. Performance Summary.

Power supply	1.2V
Input capacitance	180fF
Sampling rate	100MS/s
Resolution	9 bits
Analog power	0.184mW
Digital power	1.08mW
Total power	1.26mW
DNL	+0.4 / -0.5 LSB
INL	+0.5 / -0.7 LSB
ENOB	8.13 at fin=10MHz 8.01 at fin=50MHz
FOM	45fJ/conversion-step
Area	0.1mm × 0.13mm
Technology	65nm 1P7M CMOS with MIM capacitor

5.5 Conclusion

This work explored an asymmetric split CDAC technique based on the tri-level charge redistribution. Combining the asymmetric CDAC architecture with the tri-level charge redistribution technique makes it possible for the ADC to achieve a 9-bit resolution with the 4-bit + 3-bit capacitor arrays, which feasibly reduce the silicon cost and power consumption. Since the area of a CDAC increase exponentially with the number of bits, the area efficiency is expected to be obviously improved if higher resolution bits are implemented.

Reference (5)

[1] V. Giannini, et al., "An 820μW 9b 40MS/s Noise-Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," IEEE ISSCC Dig. Tech. Papers, 2008, pp. 238-239.

[2] Y. Chen, S. Tsukamoto and T. Kuroda, "A 9b 100MS/s 1.46mW SAR ADC in 65nm CMOS," IEEE Asian Solid-State Circuits Conference Dig. Tech. Papers, 2009, pp. 145-148.

[3] B. P. Ginsburg and A. P. Chandrakasan, "An Energy-Efficient Charge Recycling Approach for a SAR Converter with Capacitive DAC," IEEE International Symposium on Circuits and System Dig. Tech. Paper, 2009, pp. 184-187.

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[6] W. Liu, P. Huang, Y. Chiu, "A 12b 22.5/45MS/s 3.0mW 0.059mm2 CMOS SAR ADC Achieving Over 90dB SFDR," IEEE ISSCC Dig. Tech. Papers, 2010, pp. 380 - 381.

[7] H. Wei, et al., "A 0.024mm2 8b 400MS/s SAR ADC with 2b/Cycle and Resistive DAC in 65nm CMOS," IEEE ISSCC Dig. Tech. Papers, 2011, pp. 187 - 188.

Chapter 6 Summary

6.1 Summary of this work

Modern portable and wireless applications are driving ADC design towards higher resolution and data rates with dramatically low power in scaled CMOS technology. Pipelined ADCs have been facing significant challenges with technology scaling since accurate residue amplification in each pipelined stage based on op-amplifier's property is required. SAR ADC can benefits from the scaled CMOS because it does not need amplifier and most of the parts, switched capacitors and comparator, are digitally operation. In the view point of power and area efficiencies, SAR ADC is better than pipelined ADC.

Comparators are crucial building blocks in most ADCs system. Mismatches due to feature scaling, process variation and input-referred supply noise cause offset that directly affects the resolution of a comparator and thus has a crucial influence on the overall performance of the ADCs. This work explores a dynamic offset control technique that employs charge compensation by timing control. The charge injection and clock feed-through by turning off the latch reset transistor are investigated. A simple method is proposed to generate offset compensation voltage by implementing two source-drain shorted transistors on each regenerative node with timing control signals on their gates. The principle of timing based charge compensation approach for comparator offset control is described. The relationship between the offset control and slew rate of the timing control is analyzed based on simulation results. Proposed technique is confirmed by a 1GHz comparator fabricated in 65nm CMOS with 1.2V power supply. The comparator occupies 25 x 65μm^2 and consumes 380μW. 40mV offset is controlled. Proposed timing based dynamic offset control technique for

regular comparators has also been utilized by designing a 9-bit 50MHz split CDAC based SAR ADC with a foreground calibration. This technique might be used in isolation or in combination with the other offset techniques in ADC design. On the other hand, the proposed technique has some limitation since is sensitive to the timing control. Carefully design efforts is needed for the timing control circuits, since timing jitter and timing mismatch caused by PVT variation will affects the offset control range, resolution and degrades the dynamic performance.

Split CDAC is widely used in SAR ADC architecture for reducing the area. However, the nonlinearity induced by the mismatch between MSB-side and LSB-side CDAC array limits the accuracy of a SAR ADC. This work proposed a novel on-chip digitally assisted calibration technique for split CDAC based SAR ADC with minimum cost. The motivation for the calibration work came from the observation that nonlinearities dominate the split CDAC based SAR ADC causes missing code or wide code at bit decision boundary periodically. Calibration block watches the data stream from ADC output to find the wide or missing code and feedback to the compensation capacitor so as to relax the nonlinearity caused by CDAC mismatch. There is no need for additional analog hardware, such as a redundant channels or a reference converter to calibrate against. The calibration is performed using the input signal without requiring special calibration signal so that the users do not see service interruption. Furthermore, its simplicity and being a digitally assisted scheme make it amenable to scaled CMOS implementation. The proposed scheme has a limitation since it has to some extent dependence on the input signal, for example, it is hardly to handle the DC signal. In some special cases, if the output codes do not exercise the codes uniformly at both of the desired boundary region (codes 31, 63,…, 479) or (codes 30, 62,…, 478)

due to input signal, the calibration scheme might not work very well. However, in most applications, because the analog inputs are random signals, it is feasible for calibration block to watch and process the digital codes in the specified vicinity of the decision boundaries and feed back to the CDAC. The proposed technique is confirmed by a 9-bit split CDAC based SAR ADC fabricated in 65nm CMOS with 1.2V power supply. The ADC occupies 0.1 x 0.13mm^2 and consumes 1.34mW.

Thirdly, energy and area efficiency for CDAC design is always challenging for the SAR ADC designers. Split and Tri-level charge redistribution based CDAC was reported for area saving in CDAC based SAR ADC. In order to further reduce the area and power as well, this work explored an asymmetric split CDAC technique based on the tri-level charge redistribution. Combining the asymmetric CDAC architecture with the tri-level charge redistribution technique makes it possible for the ADC to achieve a 9-bit resolution with the 4-bit + 3-bit capacitor arrays, which feasibly reduce the silicon cost and power consumption. Since the area of a CDAC increase exponentially with the number of bits, the area efficiency is expected to be obviously improved if higher resolution bits are implemented. Proposed technique is confirmed by a 9-bit split CDAC based SAR ADC fabricated in 65nm CMOS with 1.2V power supply. The ADC occupies 0.1 x 0.13mm^2 and consumes 1.26mW.

6.2 Scope of Future Work

Further research will focus on optimization design of real A/D converter from both the architecture and the circuit standpoints alone with the calibration techniques, interleave and interpolation techniques to achieve high linearity, high dynamic range,

and high sampling speed simultaneously under low supply voltages in deep-submicron CMOS technology with low power consumption.

From the area efficiency point of view, the area of conventional SAR ADC is mostly occupied by the C-DAC array. In order to dramatically decrease the silicon cost, a threshold configurable SAR ADC is proposed by IMEC in 2010. The comparator is able to compare the reference level by its threshold level which is digitally controlled by logic. This means the ADC does not need CDAC any more so the most area consuming building block is removed. However, this architecture has several limitations. For example, by threshold configurable technique, the ADC is hard to work at high speed. On the other hand, the nonlinearities introduced from the circuit noise are critical and on-chip calibration is not easy to be performed. Speed efficiency would be possibly improved by using Time-Interleaved technique. However, the time-interleaving technique itself has several limitations, because even with perfectly linear components, gain/offset mismatches and timing errors can cause undesired spurs in the output spectrum. Many considerations must be taken into account before turning this technique into a successful achievement. On-chip digitally calibration for such an area, speed and power efficiency architecture is very attractive. It requires smart and efficient post-processing calibration technique, careful circuit design and layout.

List of Publications

1. Articles on periodicals

[1] X. Zhu, Y. Chen, M. Kibune, Y. Tomita, T. Hamada, H. Tamura, S. Tsukamoto, and T. Kuroda, "A Dynamic Offset Control Technique for Comparator Design in Scaled CMOS Technology," *IEICE Transactions on Fundamental of Electronics, Communications and Computer Sciences,* vol. E93-A, no.12, pp. 2456-2462, Dec. 2010.

[2] X. Zhu, Y. Chen, S. Tsukamoto and T. Kuroda, "A 9-bit 100MS/s SAR ADC with Digitally Assisted Background Calibration," *IEICE Transactions on Electronics,* vol.E95-C, no.6, pp. 1026-1034, Jun. 2012.

2. Articles on international conference proceedings

[1] X. Zhu, Y. Chen, M. Kibune, Y. Tomita, T. Hamada, H. Tamura, S. Tsukamoto, and T. Kuroda, "A dynamic offset control technique for comparator design in scaled CMOS technology," in *IEEE Custom Integrated Circuits Conference (CICC)* Dig. Tech. Papers, pp.495-498, San Jose, USA, Sep. 2008.

[2] X. Zhu, S. Tsukamoto, and T. Kuroda, "A 1 GHz CMOS Comparator with Dynamic Offset Control Technique," in *14th Asia and South Pacific Design Automation Conference (ASP-DAC),* pp.103-104, Yokohama, Japan, Jan. 2009.

[3] Y. Chen, X. Zhu, H. Tamura, M. Kibune, Y. Tomita, T. Hamada, M. Yoshioka, K. Ishikawa, T. Takayama, J. Ogawa, S. Tsukamoto and T. Kuroda, "Split Capacitor DAC Mismatch Calibration in Successive Approximation ADC," in *IEEE Custom Integrated Circuits Conference (CICC)* Dig. Tech. Paper, pp. 279-282, San Jose, USA, sep. 2009.

[4] X. Zhu, Y. Chen, S. Tsukamoto, T. Kuroda, " A 9-bit 100MS/s Tri-level Charge Redistribution SAR ADC with Asymmetric CDAC Array," in *2012 International Symposium on VLSI Design, Automation and Test (2012 VLSI-DAT)*, Hsinchu, Taiwan, Apr. 2012.

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